L6390

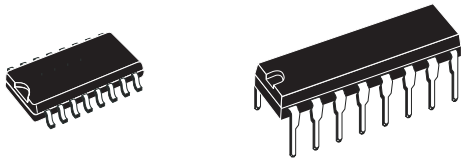
High-voltage high and low side driver

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
  - 290 mA source,
  - 430 mA sink
- Switching times 75/35 nsec rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Operational amplifier for advanced current sensing
- Comparator for fault protections
- Smart shut down function
- Adjustable dead-time
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Effective fault protection
- Flexible, easy and fast design

Applications

Motor driver for home appliances, factory automation, industrial drives. HID ballasts, power supply units.



SO-16 DIP-16

Description

The L6390 is a high-voltage device manufactured with the BCD "OFF-LINE" technology. It is a monolithic half-bridge gate driver for N-channel Power MOSFET or IGBT.

The high side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller/DSP.

The IC embeds an operational amplifier suitable for advanced current sensing in applications such as field oriented motor control.

An integrated comparator is available for protections against over-current, over-temperature, etc.

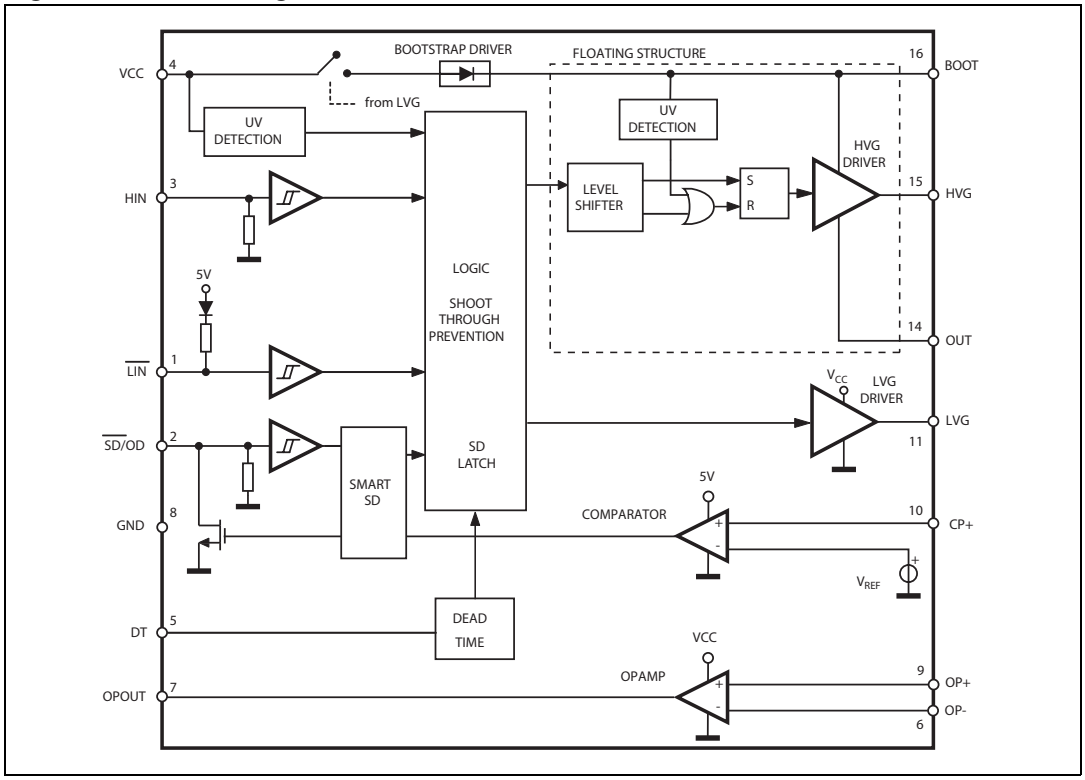
Table 1. Device summary

Order codes	Package	Packaging
L6390	DIP-16	Tube
L6390D	SO-16	Tube
L6390D013TR	SO-16	Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

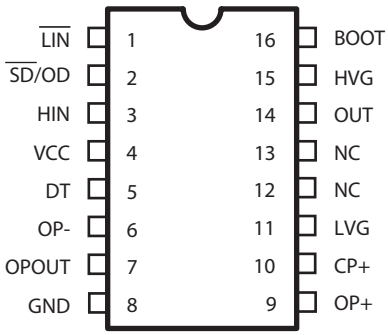


Table 2. Pin description

Pin n #	Pin name	Type	Function
1	$\overline{\text{LIN}}$	I	Low side driver logic input (active low)
2	$\overline{\text{SD}}$/OD (1)	I/O	Shut down logic input (active low)/open drain (comparator output)
3	HIN	I	High side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Dead time setting
6	OP-	I	Opamp inverting input
7	OPOUT	O	Opamp output
8	GND	P	Ground
9	OP+	I	Opamp non inverting input
10	CP+	I	Comparator input
11	LVG (1)	O	Low side driver output
12, 13	NC		Not connected
14	OUT	P	High side (Floating) common voltage
15	HVG (1)	O	High side driver output
16	BOOT	P	Bootstrap supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (@ Isink = 10 mA), with V_{CC} > 3 V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

3 Truth table

Table 3. Truth table

Input			Output	
$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
L	X	X	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

Note: X: don't care

4 Electrical data

4.1 Absolute maximum ratings

Table 4. Absolute maximum rating

Symbol	Parameter	Value		Unit
		Min	Max	
V_{cc}	Supply voltage	- 0.3	21	V
V_{out}	Output voltage	V_{boot} - 21	V_{boot} + 0.3	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{hvg}	High side gate output voltage	V_{out} - 0.3	V_{boot} + 0.3	V
V_{lvg}	Low side gate output voltage	- 0.3	V_{cc} + 0.3	V
V_{op+}	OPAMP non-inverting input	- 0.3	V_{cc} + 0.3	V
V_{op-}	OPAMP inverting input	- 0.3	V_{cc} + 0.3	V
V_{cp+}	Comparator input voltage	- 0.3	V_{cc} + 0.3	V
V_i	Logic input voltage	- 0.3	15	V
V_{od}	Open drain voltage	- 0.3	15	V
dV_{out}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	SO-16	DIP-16	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	155	100	°C/W

4.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Max	Unit
V_{cc}	4	Supply voltage		12.5	20	V
V_{BO} (1)	16-14	Floating supply voltage		12.4	20	V
V_{out}	14	DC output voltage		- 9 (2)	580	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{boot} - V_{out}$
2. LVG off. Vcc=12.5 V
   Logic is operational if $V_{boot} > 5$ V
   Refer to AN2378 for more details

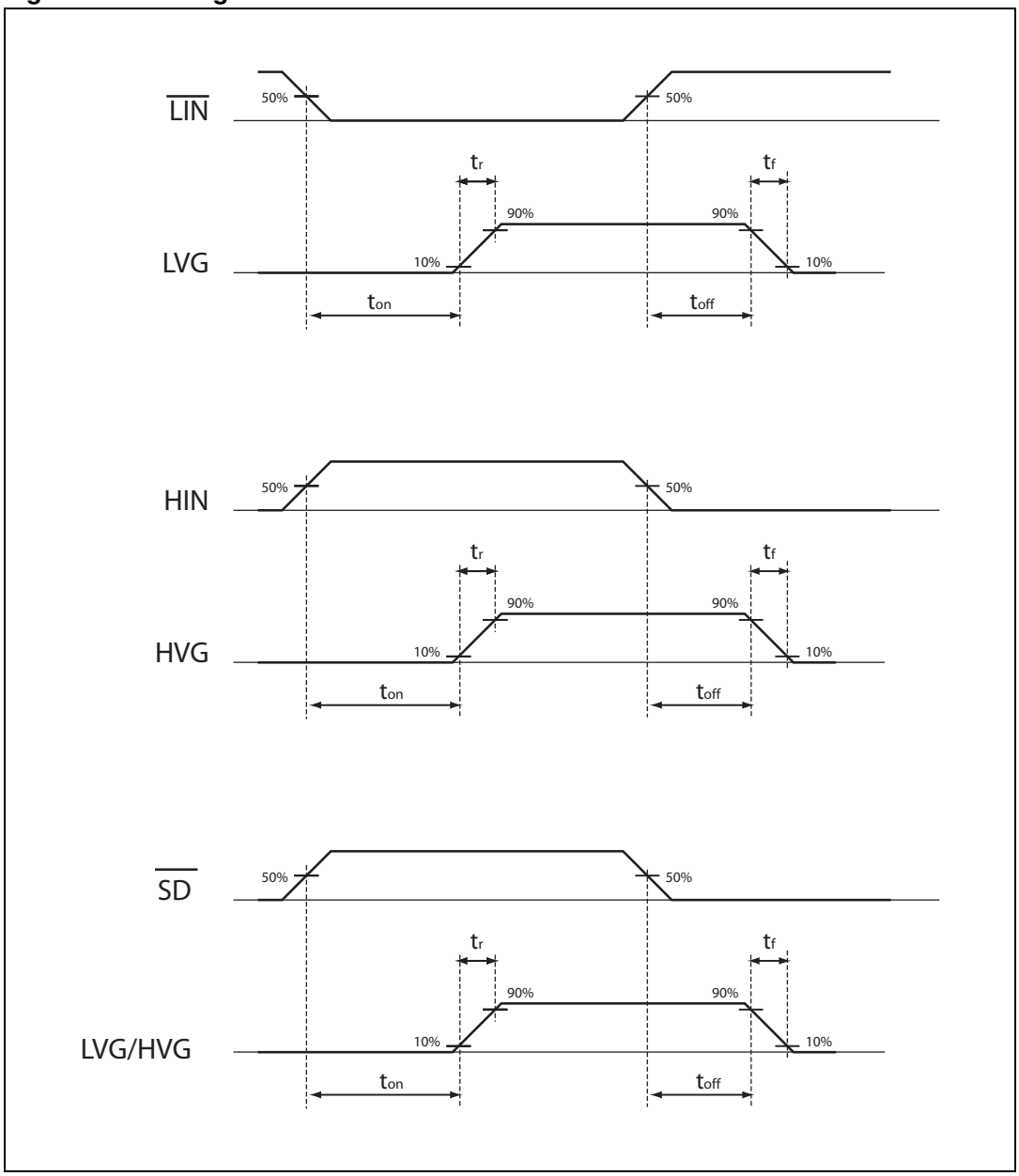
5 Electrical characteristics

5.1 AC operation

Table 7. AC operation electrical characteristics (V_{CC} = 15 V; T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
t_{on}	1 vs 11 3 vs 15	High/low side driver turn-on propagation delay	V_{out} = 0 V V_{boot} = V_{cc} C_L = 1 nF V_i = 0 to 3.3 V See *Figure 3.*		125	200	ns
t_{off}		High/low side driver turn-off propagation delay			125	200	ns
t_{sd}	2 vs 11, 15	Shut down to high/low side driver propagation delay			125	200	ns
t_{isd}		Comparator triggering to high/low side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CP+.		200	250	ns
MT		Delay matching, HS and LS turn-on/off				40	ns
dt	5	Dead time setting range	R_{dt} = 0, C_L = 1 nF, C_{DT} = 100 nF	0.1	0.18	0.25	µs
			R_{dt} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF	0.48	0.6	0.72	µs
			R_{dt} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF	1.35	1.6	1.85	µs
			R_{dt} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF	2.6	3.0	3.4	µs
MDT		Matching dead time	R_{dt} = 0, C_L = 1 nF, C_{DT} = 100 nF			60	ns
			R_{dt} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF			100	ns
			R_{dt} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF			240	ns
			R_{dt} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF			350	ns
t_r	11, 15	Rise time	C_L = 1 nF		75	120	ns
t_f		Fall time	C_L = 1 nF		35	70	ns

Figure 3. Timing



5.2 DC operation

Table 8. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Low supply voltage section							
V_{cc_hys}	4	V_{cc} UV hysteresis		1200	1500	1800	mV
V_{cc_thON}		V_{cc} UV turn ON threshold		11.5	12	12.5	V
V_{cc_thOFF}		V_{cc} UV turn OFF threshold		10	10.5	11	V
I_{qccu}		Undervoltage quiescent supply current	V_{cc} = 10 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = GND; R_{DT} = 0 Ω; CP+=OP+=GND; OP-=5 V		120	150	µA
I_{qcc}		Quiescent current	V_{cc} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = GND; R_{DT} = 0 Ω; CP+=OP+=GND; OP-=5 V		720	1000	µA
V_{ref}		Internal reference voltage		500	540	580	mV
Bootstrapped supply voltage section (1)							
V_{BO_hys}	16	V_{BO} UV hysteresis		1200	1500	1800	mV
V_{BO_thON}		V_{BO} UV turn ON threshold		10.6	11.5	12.4	V
V_{BO_thOFF}		V_{BO} UV turn OFF threshold		9.1	10	10.9	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	V_{BO} = 9 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+=OP+=GND; OP-=5 V		70	110	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+=OP+=GND; OP-=5 V		150	210	µA
I_{LK}		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot}$ = 600 V			10	µA
$R_{DS(on)}$		Bootstrap driver on resistance (2)	LVG ON		120		Ω
Driving buffers section							
I_{so}	11, 15	High/low side source short circuit current	$V_{IN} = V_{ih}$ (t_p<10 µs)	200	290		mA
I_{si}		High/low side sink short circuit current	$V_{IN} = V_{il}$ (tp<10 µs)	250	430		mA

Table 8. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C) (continued)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Logic inputs							
V_{il}	1, 2, 3	Low logic level voltage				0.8	V
V_{ih}		High logic level voltage		2.25			V
I_{HINh}	3	HIN logic “1” input bias current	HIN = 15 V		175	260	µA
I_{HINl}		HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	1	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 0 V		6	20	µA
I_{LINh}		$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	2	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 15 V		40	100	µA
I_{SDl}		$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 0 V			1	µA

1. $V_{BO} = V_{boot} - V_{out}$
2. R_{DSON} is tested in the following way:
   $R_{DSON} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I_1(V_{CC},V_{CBOOT1}) - I_2(V_{CC},V_{CBOOT2})]$
   where I_1 is pin 16 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

Table 9. OPAMP characteristics (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
I_{ib}	6, 9	Input bias current (1)			100	200	nA
V_{icm}		Input common mode voltage range		0			V
V_{OL}	7	Low level output voltage	V_{id} = ± 1 V, R_L = 10 kΩ to V_{CC}		75		mV
V_{OH}		High level output voltage	V_{id} = ± 1 V, R_L = 10 kΩ to GND		14.7		V
I_o		Output short circuit current	Source, V_{id} = ± 1; V_o = 0 V	16	30		mA
			Sink, V_{id} = ± 1; V_o = V_{CC}	50	80		mA
SR		Slew rate	V_i = 1 ÷ 4 V; R_L = 2 kΩ; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP		Gain bandwidth product	V_o = 7.5 V; R_L = 2 kΩ		12		MHz
A_{vd}		Large signal voltage gain		75	85		dB
SVR		Supply voltage rejection ratio		60	70		dB
CMRR		Common mode rejection ratio			70		dB

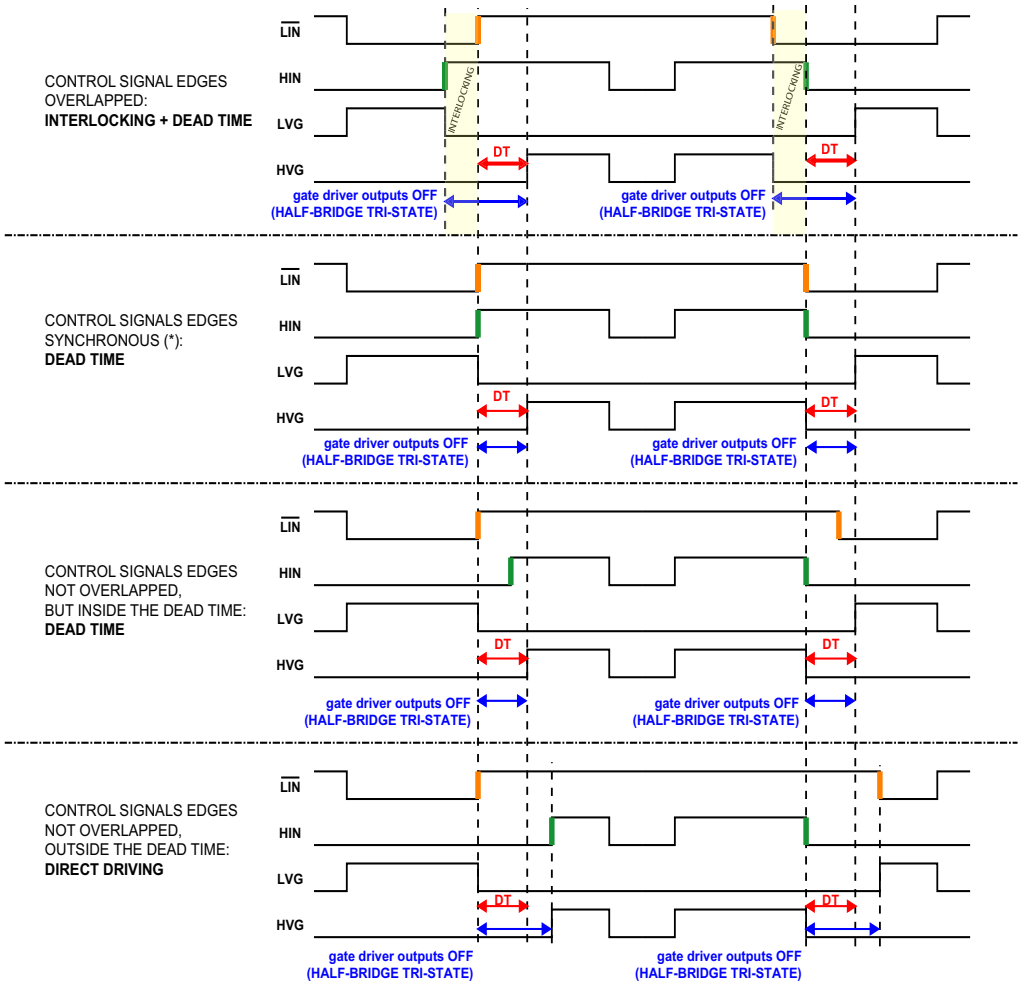
1. The direction of input current is out of the IC.

Table 10. Sense comparator characteristics (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test conditions	Min	Typ	Max	Unit
I_{io}	10	Input bias current	V_{CP+} = 1 V			1	µA
V_{ol}	2	Open drain low level output voltage	I_{od} = - 3 mA			0.5	V
t_{d_comp}		Comparator delay	$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor		90	130	ns
SR	2	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ		60		V/µsec

6 Waveforms definitions

Figure 4. Dead time and interlocking waveforms definitions

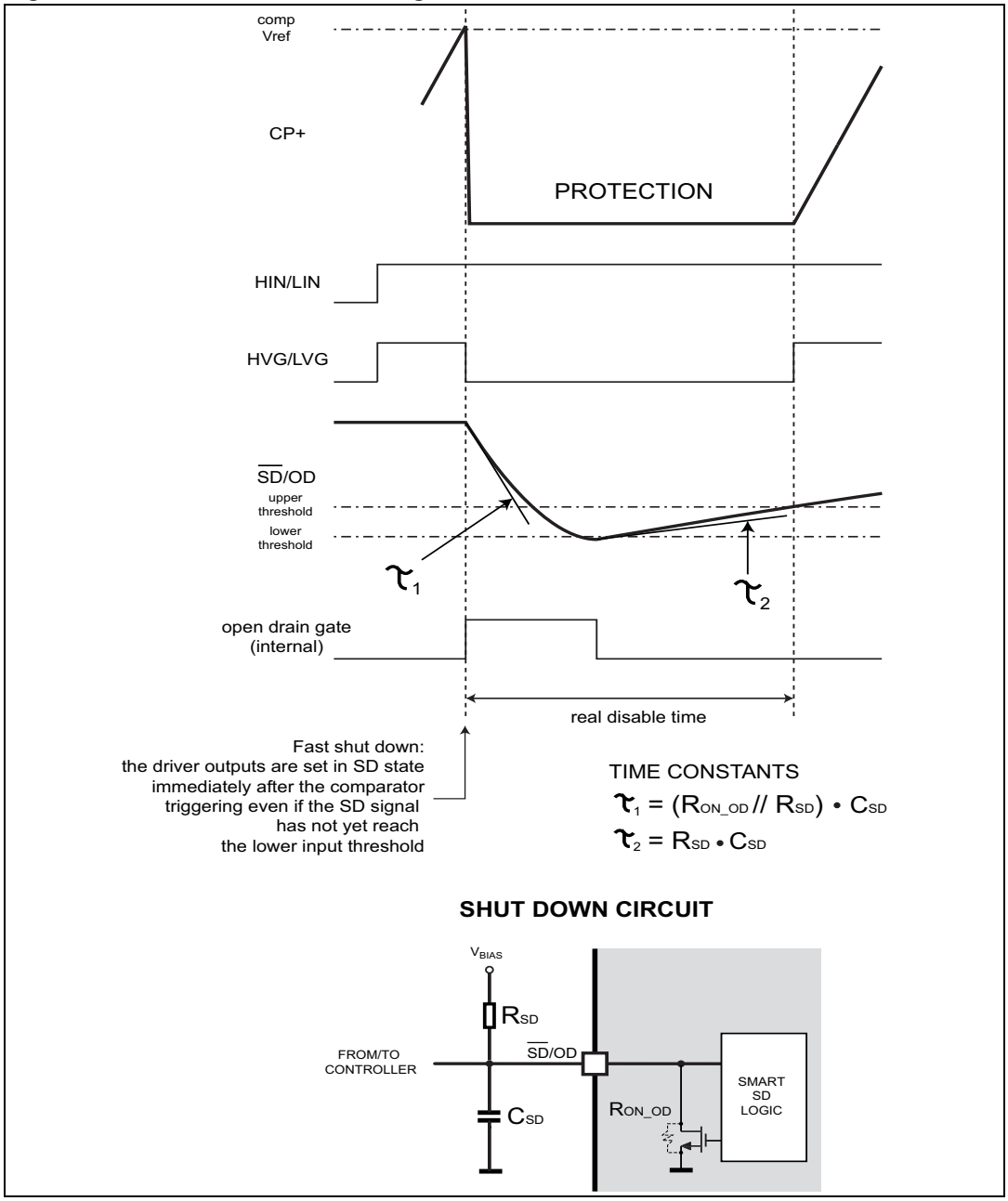


(*) HIN and $\overline{LIN}$ can be connected togheter and driven by just one control signal

7 Smart shut down function

L6390 integrates a comparator committed to the fault sensing function. The comparator has an internal voltage reference V_{ref} connected to the inverting input, while the non-inverting input is available on pin 10. The comparator input can be connected to an external shunt resistor in order to implement a simple over-current detection function. The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on pin 2, shared with the $\overline{SD}$ input. When the comparator triggers, the device is set in shut down state and both its outputs are set to low level leaving the half-bridge in tri-state.

Figure 5. Smart shut down timing waveforms

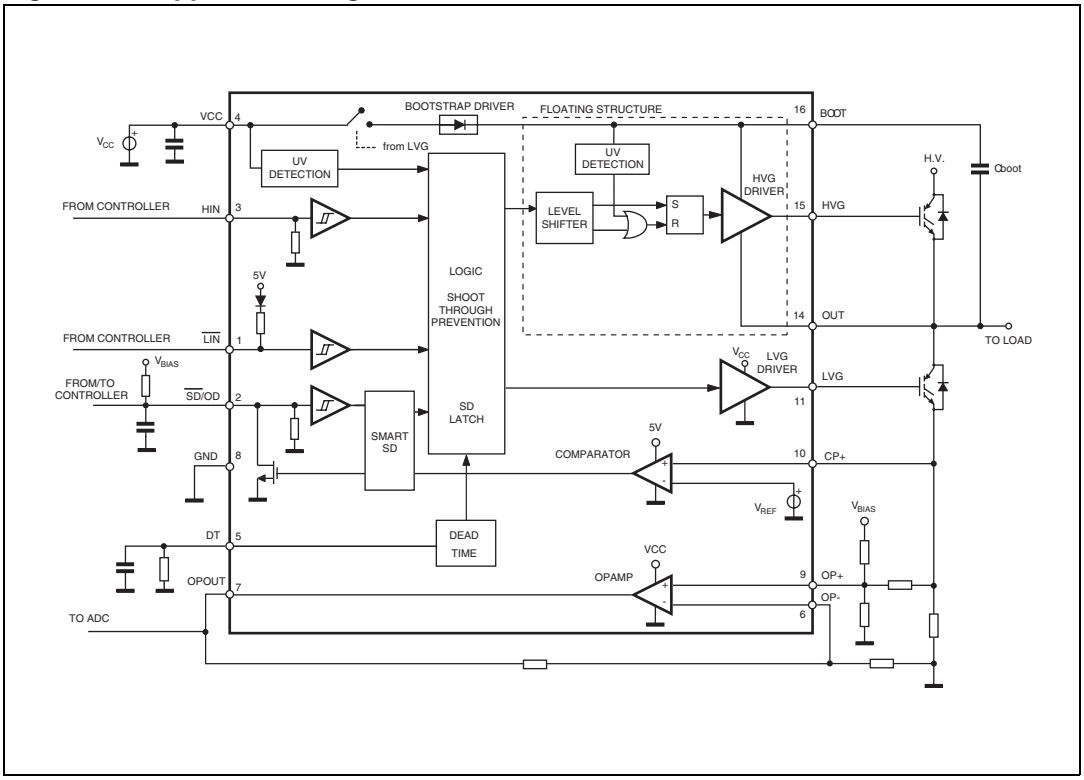


In common over-current protection architectures the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$/OD line in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Differently from the common fault detection systems, L6390 Smart shut down architecture allows to immediately turn-off the outputs gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual outputs switch-off. In fact the time delay between the fault and the outputs turn off is no more dependent on the RC value of the external network connected to the pin.In the Smart shut down circuitry, the fault signal has a preferential path which directly switch off the outputs after the comparator triggering. At the same time the internal logic turns on the open drain output and holds it on until the $\overline{SD}$ voltage goes below the $\overline{SD}$ logic input lower threshold. The Smart shut down system provides the possibility to increase the time constant of the external RC network (that is the disable time after the fault event) up to very large values without increasing the delay time of the protection.

Any external signal provided to the $\overline{SD}$ pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the $\overline{SD}$ input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice versa.

8 Typical application diagram

Figure 6. Application diagram



9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 7*.a). In the L6390 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with diode in series, as shown in *Figure 7*.b.
An internal charge pump (*Figure 7*.b) provides the DMOS driving voltage.

9.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

e.g.: HVG steady state consumption is lower than 200 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

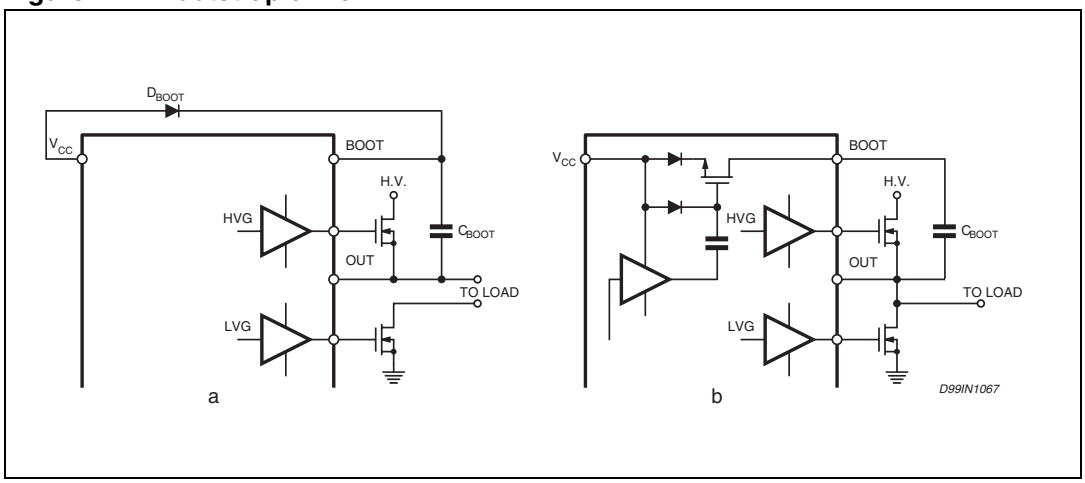
For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the T_{charge} is 5µs. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.7V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 7. Bootstrap driver



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 8. DIP-16 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

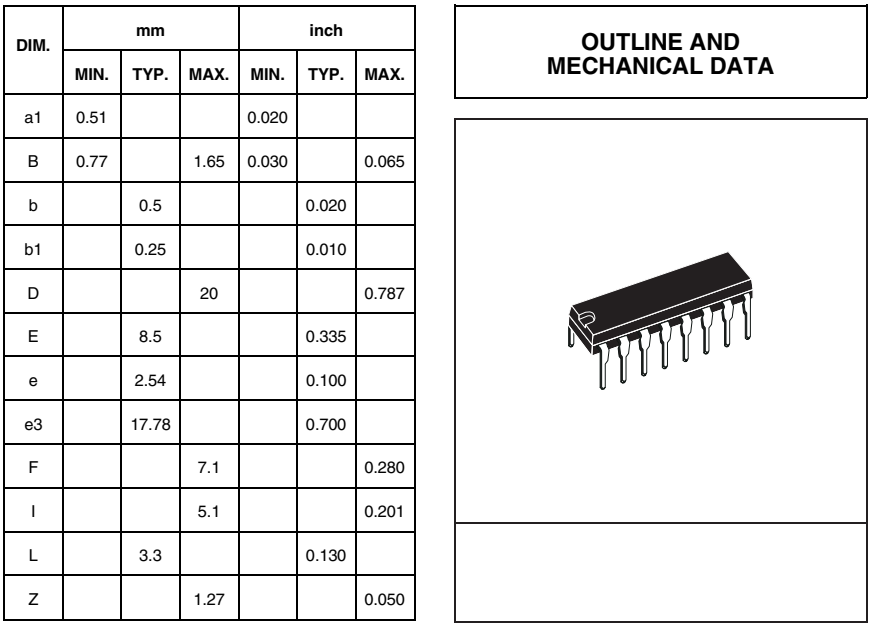
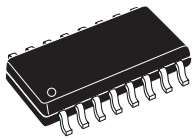


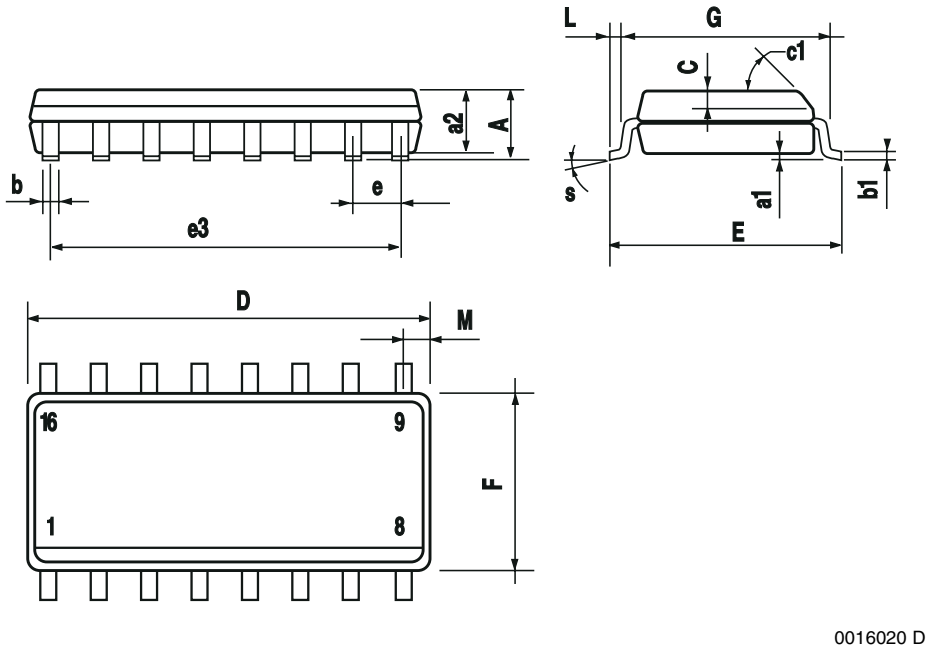
Figure 9. SO-16 narrow mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

OUTLINE AND MECHANICAL DATA





0016020 D

11 Revision history

Table 11. Document revision history

Date	Revision	Changes
29-Feb-2008	1	First release
09-Jul-2008	2	Updated: Cover page, *Table 2 on page 4*, *Table 3 on page 5*, *Section 4 on page 6*, *Section 5 on page 8*, *Section 9.1 on page 17*
17-Jul-2008	3	Updated test condition values on *Table 8* and *Table 9*

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