Enpirion® Power Datasheet

EV1380QI 8A PowerSoC
Highly Integrated Synchronous DC-DC
DDR2/3/4/QDR™ Memory Termination

Description

The EV1380QI is a Power System on a Chip (PowerSoC) DC to DC converter in a 68 pin QFN that is optimized for DDR2, DDR3, and QDR™ VTT applications. It requires a power supply (AVIN) for the controller and operates from an input supply (VDDQ). It provides a tightly regulated and very stable output voltage (VTT) which tracks VDDQ while sinking and sourcing up to 8A of output current. Altera Enpirion's integrated inductor technology significantly helps to reduce noise, and offers a high efficiency solution for VTT applications with a very low external component count.

Advanced circuit techniques, optimized switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements.

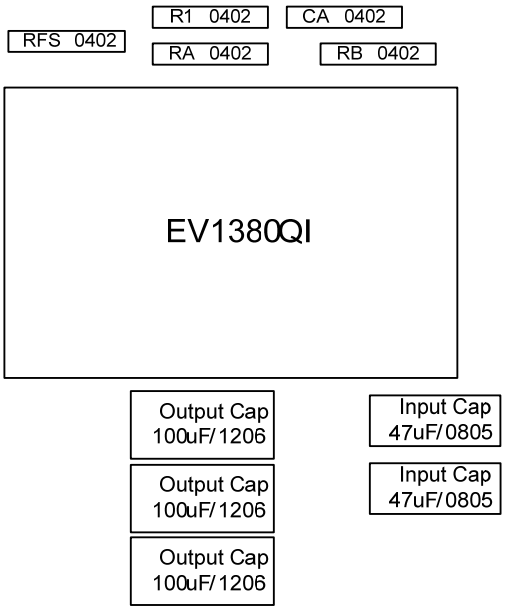


Figure 1: EV1380QI Total Solution Size ~200mm² (not to scale). Does not show back-side components.

Features

- High efficiency, up to 94%.
- Output voltage tracks VDDQ +/- 1%
- Nominal 1.5MHz operating frequency with ability to synchronize to an external clock source or serve as the primary source.
- Programmable soft-start time. Soft Shutdown.
- Master/slave configuration for parallel operation.
- Thermal shutdown, over current, short circuit, and under-voltage protection.
- RoHS compliant, MSL level 3, 260C reflow.

Application

- Bus Termination: DDR2, DDR3, DDR4 & QDR™ memory

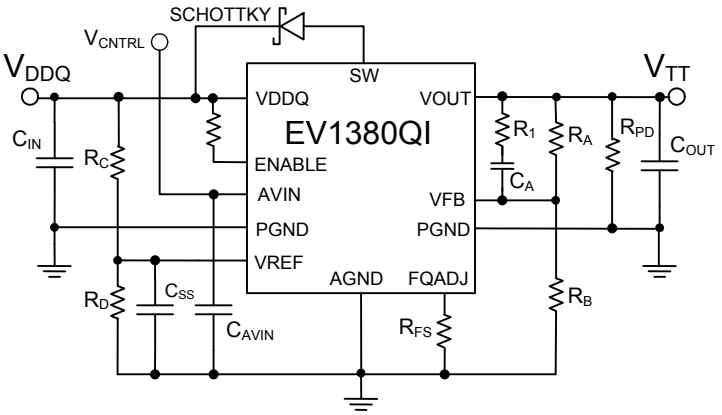


Figure 2: Typical Application Schematic (V_{DDQ} is the memory core voltage; V_{TT} is memory termination voltage that tracks V_{DDQ})

Ordering Information

Part Number	Temp Rating (°C)	Package
EV1380QI	-40 to +85	68-pin QFN T&R
EVB-EV1380QI	QFN Evaluation Board	

Pin Assignments (Top View)

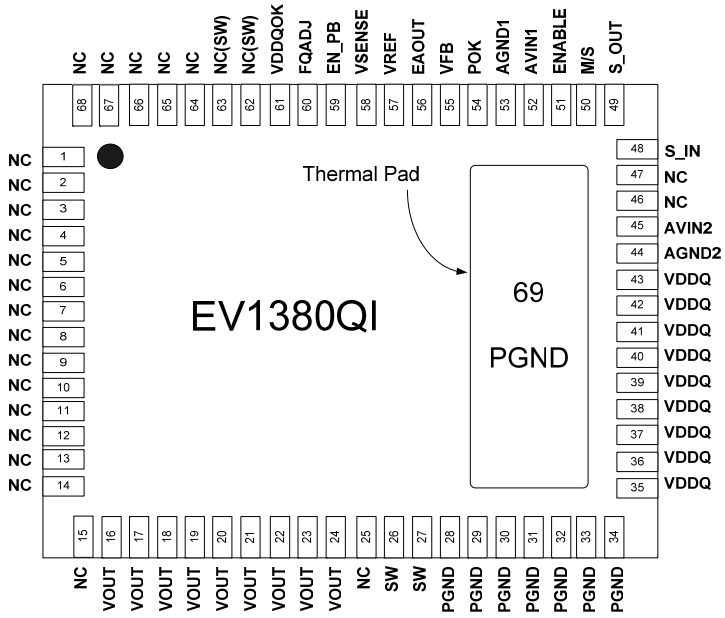


Figure 3: Pin Out Diagram (Top View)

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

Pin Description

PIN	NAME	FUNCTION
1-15, 25, 46-47, 64-68	NC	NO CONNECT: These pins must be soldered to PCB but not be electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
16-24	VOUT	Regulated converter output. Connect to the load, and place output filter capacitor(s) between these pins and PGND pins 28-31.
26-27	SW	These pins are internally connected to the common switching node of the internal MOSFETs. The anode of a schottky diode needs to be connected to these pins. The cathode of the diode needs to be connected to VDDQ.
28-34	PGND	Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN descriptions for more details.
35-43	VDDQ	In DDR applications the input to this pin is the DDR core voltage. This is the input power supply to the power train which will be divided by two to create an output voltage that tracks with the input voltage applied to this pin. Place input filter capacitor(s) between these pins and PGND pins 32-34.
44	AGND2	Ground for the gate driver supply. Connect to the ground plane with a via.
45, 52	AVIN2, AVIN1	Analog input voltage for the controller circuits. Each of these pins needs to be separately connected to the 3.3V input supply. Decouple with a capacitor to AGND1.
48	S_IN	Digital Input. Depending on the M/S pin, this pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another Altera Enpirion device. Leave this pin floating if it is not used.

PIN	NAME	FUNCTION
49	S_OUT	Digital Output. Depending on the M/S pin, either a clock signal synchronous with the internal switching frequency or the PWM signal is output on this pin. Leave this pin floating if it is not used.
50	M/S	This is a Ternary Input put. Floating the pin disables parallel operation. A low level configures the device as Master and a High level configures the device as a slave.
51	ENABLE	This is the Device Enable pin. Tie this pin to VDDQ with a 10kΩ resistor.
53	AGND	This is the quiet ground for the control circuits. Connect to the ground plane with a via.
54	POK	POK is a logical AND of VDDQOK and the internally generated POK of the EV1380QI. POK is an open drain logic output that requires an external pull-up resistor. POK is logic high when VOUT is within -10% to +10% of VOUT nominal. This pin guarantees a logic low even when the EV1380QI is completely un-powered. This pin can sink a maximum 4mA. The pull-up resistor may be connected to a power supply other than AVIN or VDDQ but the voltage should be <3.6Volts.
55	VFB	This is the External Feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. (A feed-forward capacitor is required across the upper resistor.) The output voltage regulates so as to make the VFB node voltage = VREF.
56	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
57	VREF	External voltage reference input. A resistor divider connects from VDDQ to AGND. The mid-point of the resistor divider is connected to VREF. The resistor divider has to be chosen to make the voltage applied to this pin ~0.4*VDDQ. An optional capacitor (for soft start) may be connected from VREF to AGND.
58	VSENSE	Connect this pin to VOUT.
59	EN_PB	This is the Enable Pre-Bias Input. When this pin is pulled high, the Device will support start-up under a pre-biased load. This pin is pulled high internally.
60	FQADJ	Tie this pin to AGND through a 13kΩ resistor.
61	VDDQOK	This is an active high input pin that indicates the externally supplied VDDQ has reached its POK level. This pin should be tied to the VDDQ regulator POK output, or let float if unused.
62-63	NC(SW)	NO CONNECT: These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
69	PGND	Device thermal pad to be connected to the system GND plane for heatsinking purposes. See Layout Recommendations section.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage: AVIN1, AVIN2	V_{IN}	-0.5	4.0	V
Voltages on: EN, EN_PB, VDDQOK		-0.5	V_{IN}	V
Voltages on: VFB, VREF, EAOUT, M_S, S_IN, S_OUT, VDDQ, VOUT, VSENSE, FQADJ		-0.5	2.7	V
Voltage on: POK			3.6	V
Voltage on: SW		-0.5	VDDQ+0.5	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model) – VREF pin			1500	V
ESD Rating (based on Human Body Model) – All other pins			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range: AVIN1, AVIN2		3.07	3.53	V
Input Voltage Range: VDDQ		1.16	1.65*	V
Input Voltage Range: VREF	V_{EXTREF}	0.5	0.5	V
EN_PB, VDDQOK, M/S, S_IN, EN		0	AVIN	V
Operating Ambient Temperature	T_A	- 40	+85	°C
Operating Junction Temperature	T_J	- 40	+125	°C

***: For DDR2 applications with VDDQ=1.8V, contact Power Applications support.**

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (**Note 1**)	θ_{JA}	16	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1.5	°C/W
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	20	°C

Note 1: Based on a 2oz. copper board and proper thermal design in line with JEDEC EIJ/JESD 51 Standards.

Electrical Characteristics

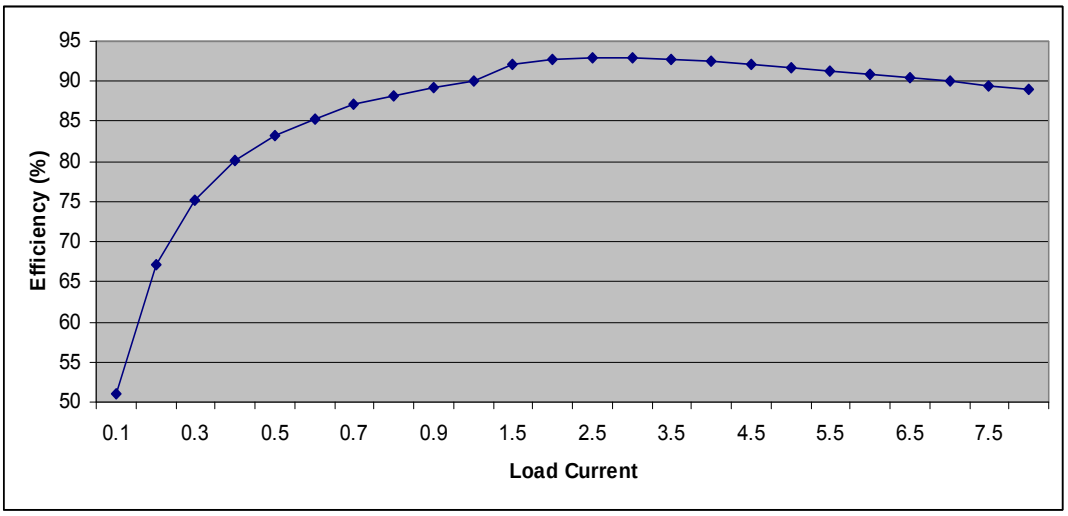
NOTE: AVIN1, AVIN2 = 3.3V, over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Power Supply Voltage	VDDQ		1.16		1.65	V
Controller Supply Voltage	AVIN		3.07	3.3	3.53	V
Controller Supply Current	I_{AVIN}	AVIN = 3.3V		18	25	mA
Output Voltage Accuracy – Initial	ΔV_{OUT}	V_{OUT} =1/2 VDDQ (e.g. @ VDDQ = 1.500V), 0.1% input and output resistor dividers)	0.740		0.760	V
VFB Pin Voltage	V_{VFB}	3.07V ≤ AVIN ≤ 3.53V, VDDQ = 1.5V, 0A ≤ ILOAD ≤ 8A	591	600	609	mV
VFB Pin Input Leakage Current	I_{VFB}	VFB pin input leakage current	-5		5	nA
Shut-Down Supply Current	I_S	Power Supply current with Enable=0		450		µA
Under Voltage Lock-out – AVIN Rising	V_{UVLOR}	Voltage above which UVLO is not asserted		2.2		V
Under Voltage Lock-out – AVIN Falling	V_{UVLOF}	Voltage below which UVLO is asserted		2.05		V
Peak-to-Peak Ripple	R_{PP}	VDDQ = 1.5V, V_{OUT} = 0.75V, I_{OUT} = 8A, C_{OUT} = 3x100 µF (1206)		<10		mV
Maximum Continuous Output Sourcing Current	$I_{OUT\_Max\_SRC}$	Maximum load current. See Note 1.	8			A
Maximum Continuous Output Sinking Current	$I_{OUT\_Max\_SNK}$	Maximum load current. See Note 1.	8			A
Over Current Trip Level	I_{OCPH}	Sourcing. VDDQ = 1.5V		18		A
Switching Frequency	F_{SW}	R_{FQADJ} = 13kOhms		1.5		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	SYNC clock input frequency range R_{FQADJ} = 13kOhms	1.25		1.75	MHz
S_IN Clock Amplitude – Low	$V_{S\_IN\_LO}$	SYNC Clock Logic Level			0.4	V
S_IN Clock Amplitude – High	$V_{S\_IN\_HI}$	SYNC Clock Logic Level	1.8		2.5	V
S_IN Clock Duty Cycle (PLL)	DC_{S_INPLL}	M_S Pin Float or Low	20		80	%
S_IN Clock Duty Cycle (PWM)	DC_{S_INPWM}	M_S Pin High		50		%
Pre-Bias Level	V_{PB}	Allowable pre-bias as a fraction of programmed output voltage.	0		40	%
V_{OUT} Range for P_{OK} = High	VDDQ rising	Range of output voltage as a fraction of programmed value when P_{OK} is asserted	92±3		110±3	%
V_{OUT} Range for P_{OK} = High	VDDQ falling	Range of output voltage as a fraction of programmed value when P_{OK} is asserted		90±3		%
P_{OK} Deglitch Delay		Falling edge deglitch delay after output crossing 90% level		64		Clock cycles

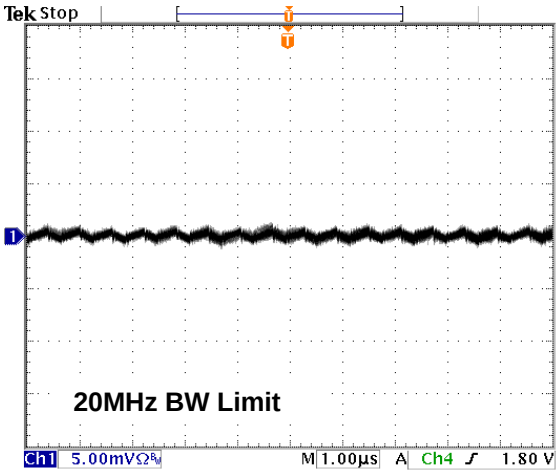
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{POK} Logic Low level		With 4mA current sink into P_{OK} pin		0.7	1	V
V_{POK} Logic high level				AVIN		V
POK Current Sink Capability		3.07V ≤ AVIN ≤ 3.53V		4		mA
VTT Tracking VDDQ	VDDQ – 2*VTT	VDDQ > 1V, VDDQ Rate of change at 1V/ms	-25		+25	mV
Enable Pin Current	I_{EN}	Tied to VDDQ through a 10kΩ		50		µA
Logic Low Threshold	V_{B-LOW}	ENABLE, S_IN, VDDQOK			0.4	V
Logic High Threshold	V_{B-HIGH}	ENABLE, S_IN, VDDQOK	1.8			V
S_OUT Low Level	$V_{S\_OUT\_LOW}$				0.4	V
S_OUT High Level	$V_{S\_OUT\_HIGH}$		2.0			V
M/S Pin Logic Low Threshold	V_{T-LOW}	Threshold voltage for Logic Low			0.4	V
M/S Pin Logic High Threshold	V_{T-HIGH}	Threshold voltage for Logic High (internally pulled high; can be left floating to achieve logic high)	2.0		2.7	V
M/S Pin Input Current	I_{ITERN}	The ternary pin has 100kΩ to AGND and another 100kΩ to an internal 2.5V supply. If connecting to AVIN recommend using a series resistor. See Figure 7.		See Figure 7.		µA
Current Balance	ΔI_{OUT}	With 2 converters in parallel, the difference between any two parts. AVIN<50mV, R_{TRACE}< 2 mΩ		+/-10		%

Note 1: Maximum output current may need to be de-rated, based on operating condition, to meet TJ requirements.

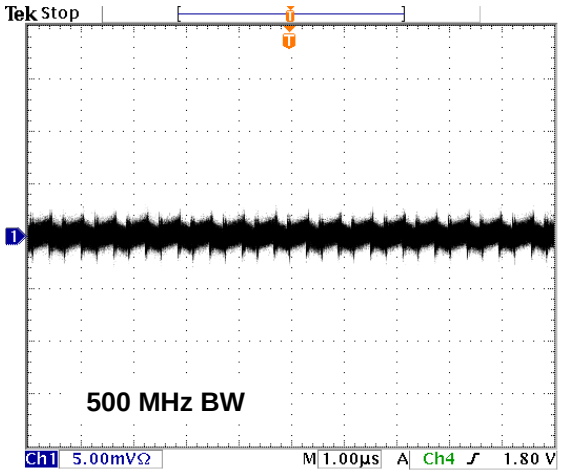
Typical Performance Characteristics



Efficiency AVIN = 3.3V, VDDQ = 1.5V V_{OUT} = VDDQ * 0.5



Output Ripple: AVIN = 3.3V, VDDQ = 1.16V, VOUT = VDDQ*0.5, Iout = 8A, C_{IN} = 2x47µF (0805), C_{OUT} = 4x100µF (1206)



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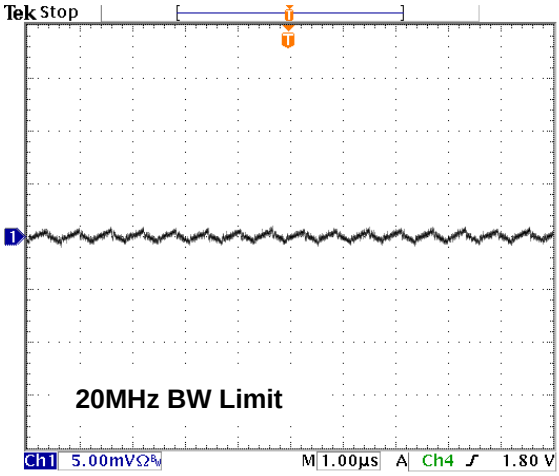
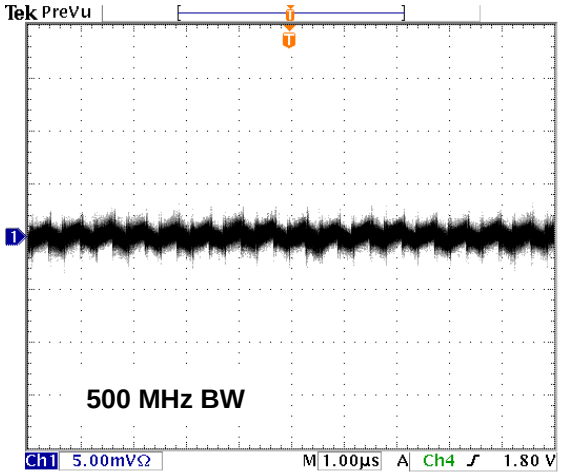


Output Ripple: AVIN = 3.3V, VDDQ = 1.5V, VOUT = VDDQ*0.5, Iout = 8A, C_{IN} = 2x47µF (0805), C_{OUT} = 4x100µF (1206)



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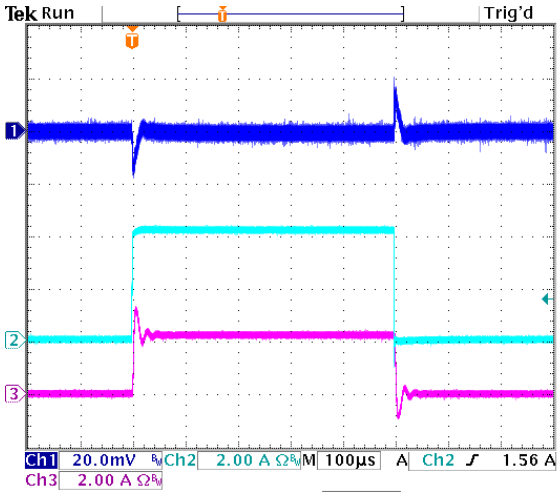
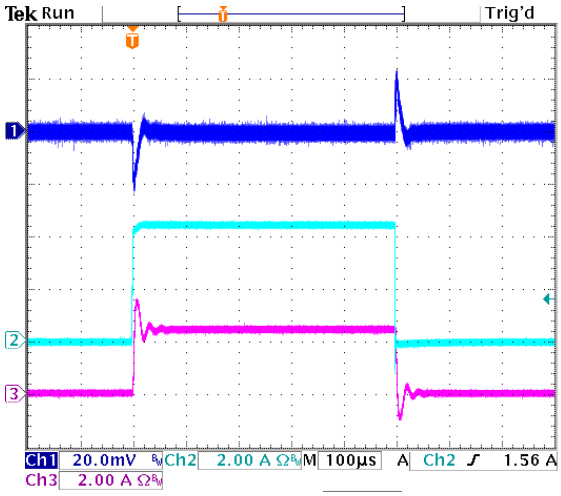
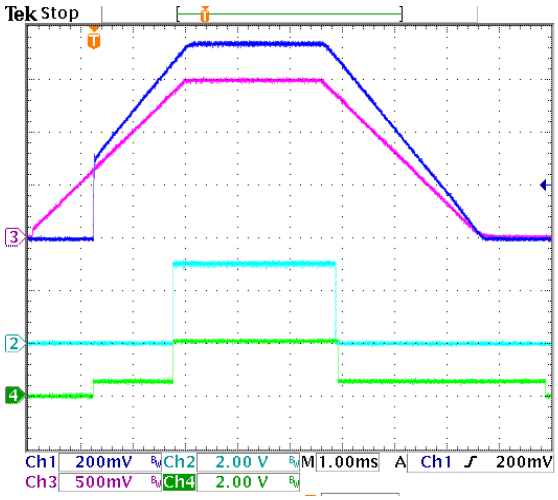


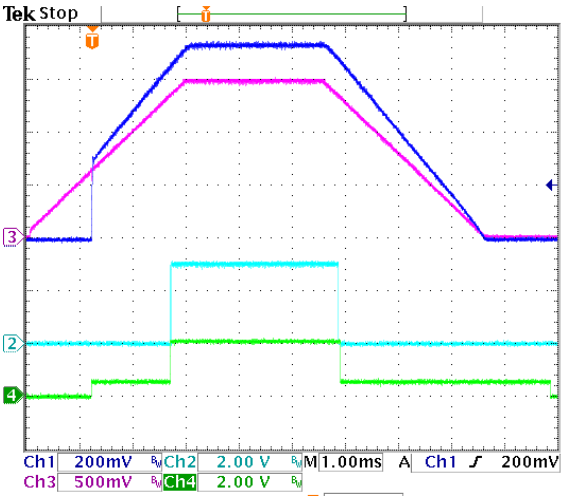
Load Transient Response: AVIN = 3.3V, VDDQ = 1.5V, VOUT = VDDQ*0.5, Ch.1: V_{OUT}, Ch.2: I_{LOAD} 0↔~4A, Ch.3: I_{VDDQ} C_{IN} = 2x47µF (0805), C_{OUT} = 4x100µF (1206)



Load Transient Response: AVIN = 3.3V, VDDQ = 1.215V, VOUT = VDDQ*0.5, Ch.1: V_{OUT}, Ch.2: I_{LOAD} 0↔~4A, Ch.3: I_{VDDQ} C_{IN} = 2x47µF (0805), C_{OUT} = 4x100µF (1206)



Power Up/Down at No Load: AVIN = 3.3V, VDDQ = 1.5V, VOUT = VDDQ*0.5, Ch.1: V_{OUT}, Ch.2: VDDQOK, Ch.3: VDDQ, Ch. 4: POK C_{IN} = 2x47µF (0805), C_{OUT} = 4x100µF (1206)



Power Up/Down into a ~94mΩ Load: AVIN = 3.3V, VDDQ = 1.5V, VOUT = VDDQ*0.5, Ch.1: V_{OUT}, Ch.2: VDDQOK, Ch.3: VDDQ, Ch. 4: POK C_{IN} = 2x47µF (0805), C_{OUT} = 4x100µF (1206)

Functional Block Diagram

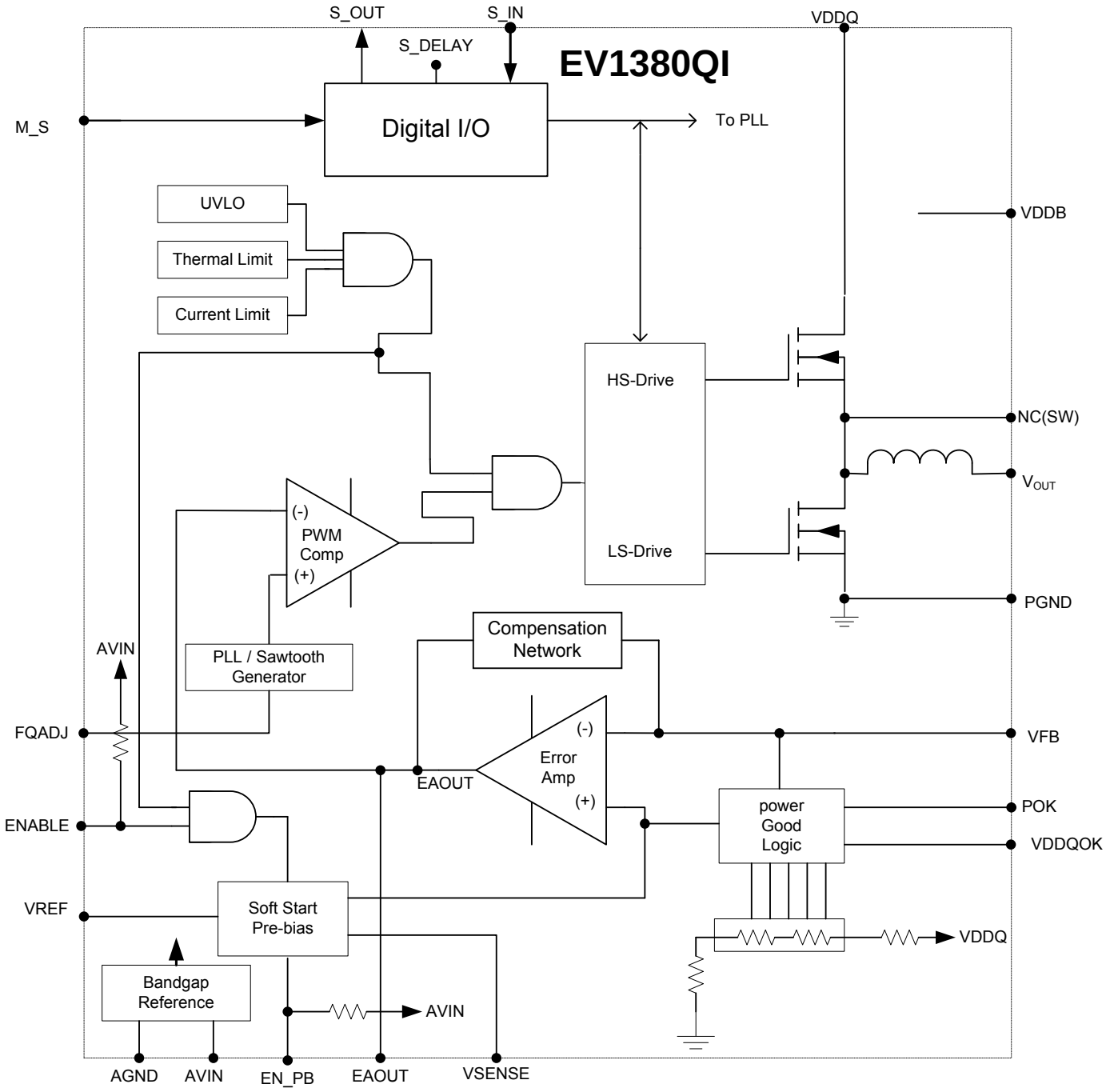


Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EV1380QI is a synchronous, programmable Buck power supply with integrated power MOSFET switches and integrated inductor. The switching supply uses voltage mode control and a low noise PWM topology. Typically two power sources are required to operate this device. The first power source (AVIN) is for the controller with a nominal input voltage range of 3.07-3.53V. The second supply (VDDQ) is the supply that is tracked - the recommended operating range is 1.16 to 1.65V. With the right choice of input

and output dividers, the output voltage of the EV1380QI will produce an Output Voltage which tracks to ½ VDDQ. The EV1380QI can continuously source or sink currents up to 8A. The 1.5MHz nominal switching frequency enables small-size input and output capacitors.

Soft-Start and Soft-Shutdown

The EV1380QI is expected to operate with the controller power supply (AVIN) ON, VDDQ ramped up and down at a relatively slow rate (~1V/mS), and ENABLE tied to VDDQ through a 10kΩ resistor. It is also acceptable for VDDQ to be dynamically scaled within a small voltage range. If, however, VDDQ should ramp up at a high rate, a capacitor connected between VREF and AGND provides the soft-start function to limit in-rush current. The soft-start time constant is determined by the input voltage divider and the soft-start capacitor. See figure 5.

Pre-Bias Start-up

The EV1380QI supports start up into a pre-biased load. Allowable pre-bias is in the range of 0% to 40% of the programmed output voltage. The Pre-Bias feature is controlled by the EN_PB pin. For the pre-Bias feature to function properly, VDDQ must be stable; Enable must be toggled; and a pre-bias must be present at the output.

Phase-Lock Operation:

With M_S pin floating or at a logical '0,' the internal switching clock of the DC/DC converter can be phase-locked to a clock signal applied to S_IN. When a clock signal is present at S_IN, an activity detector recognizes the presence of the clock signal and the internal oscillator phase locks to the external clock. The external clock could be the system clock or the output of another EV1380QI. A delayed version of the phase locked clock is output at S_OUT. The clock frequency should be within 1.25MHz to 1.75MHz for guaranteed phase-lock. Two EV1380QI devices on a system board may be daisy chained with appropriate phase delays to reduce or eliminate input ripple as well as avoid beat frequency components.

Master / Slave (Parallel) Operation:

Up to two EV1380QI devices may be connected in a Master / Slave configuration to handle larger load currents. The Master device's switching clock may be phase-locked to an external clock source or another EV1380QI. The device is placed in Master mode by pulling the M_S pin low or in Slave mode by pulling M_S pin high. When this pin is in Float state, parallel operation is not possible. In Master mode, the internal PWM signal is output on the S_OUT pin. The PWM signal at S_OUT is delayed relative to the Master device's internal PWM signal. This PWM signal from the Master is fed to the Slave device at its S_IN input. The Slave device acts like an extension of the power FETs in the Master. The inductor in the slave prevents crow-bar currents from Master to slave due to timing delays. Altera does not recommend paralleling more than 2 EV1380QI's.

POK Operation

The internal POK signal is asserted when VDDQ > 0.3V and 0.45*VDDQ < VOUT < 0.55*VDDQ, indicating VOUT is tracking VDDQ. This assertion range assumes typical VDDQ slew rates associated with VDDQ POL regulators. For typical VDDQ POL regulators, the VDDQ ramp rate will range from 0.5 V/mSec to 2 V/mSec. Within this range of slew rates, the speed of the POK circuit, the loop bandwidth, and the delay caused by the soft-start capacitor on the VREF pin will not significantly affect the measured POK threshold. For much faster VDDQ ramp rates, hot-plug slew rates for example, the speed and latency of the elements will cause the measured VOUT voltage where POK is valid to be higher than the actual threshold.

The internal EV1380QI POK is AND'ed with the VDDQOK input. The VDDQOK input is driven by the upstream VDDQ regulator's POK output. Normally the VDDQOK input indicates that VDDQ has settled to the required level. If VDDQ is dynamically switched, VDDQOK is expected to mask the EV1380QI POK during the voltage transition. POK is not guaranteed to be valid when VDDQ < 300mV. The POK

signal is asserted high when rising VOUT voltage crosses 46% (nominal) of VDDQ. POK is de-asserted low ~64 clock cycles after the falling VOUT voltage crosses 45% (nominal) of VDDQ. POK is also de-asserted if VOUT exceeds 55% (nominal) of VDDQ. For proper POK thresholds, the input voltage divider must generate VREF = ~0.4*VDDQ.

Over Current Protection

The current limit function is achieved by sensing the current flowing in the hi-Side FET. The OCP trip point is nominally set to 225% of maximum rated load at VDDQ=1.5V. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition lasts only a few switching cycles, normal PWM operation is resumed. If the over-current condition persists, the circuit will continue to protect the load by entering a hiccup mode. In the hiccup mode, the output is disabled for approximately 20ms and then it goes through a soft-start. The output will no longer track the input voltage briefly as a result of the fault condition. This cycle can continue indefinitely as long as the over current condition persists.

Thermal Overload Protection

Temperature sensing circuits in the controller will disable operation when the Junction temperature exceeds approximately 150ºC. When the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start cycle.

Input Under-Voltage Lock-Out

When the controller voltage AVIN is below a required voltage level (V_{UVLOR}) for normal operation, converter switching is inhibited. The lock-out threshold has hysteresis to prevent chatter. When the device is operating normally, the input voltage must fall below the lower threshold (V_{UVLOF}) for the device to stop switching.

Application Information / Layout Recommendation

Soft-start Capacitor Selection

A soft-start capacitor is recommended on the EV1380QI's VREF pin. The soft start capacitor serves as both a noise filter for noise on VDDQ as well as a slew rate limiter for fast VDDQ input ramps. The soft start time constant is determined by the value of this capacitor and the input divider resistors R_C and R_D. See figure 5. For most applications, Altera recommends a 0.1µF capacitor on this node.

Output Voltage Programming and loop Compensation

The output voltage of EV1380QIQI is determined by the two voltage dividers as shown in the simplified application diagram of Figure 5.

The VDDQ voltage divider consisting of R_C and R_D should be selected to make VREF = ~0.4 * VDDQ for proper POK operation. Altera recommends R_C = 3.01kΩ and R_D = 2kΩ. This requirement ensures proper POK operation.

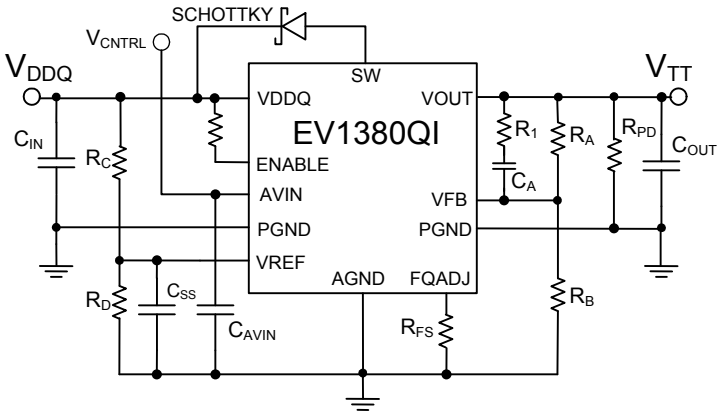


Figure 5: Typical Application Schematic

In steady state, VREF = VFB, and VOUT = 0.5 *VDDQ with proper selection of R_A and R_B.

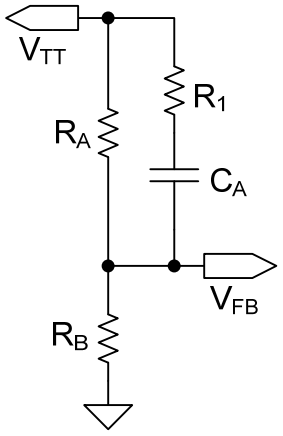
R_A and R_B are calculated using the equations in Figure 6. For best voltage accuracy 0.1% resistors are recommended for R_A–R_D. For example, for VDDQ = 1.5V, R_A = 60.4kΩ,

R_B = 240kΩ.

Although the EV1380QI integrates most of the compensation network, a phase lead capacitor and a resistor are required in parallel with the upper resistor R_a of the external feedback network as shown in Figure 6. For the 1.5V VDDQ example stated above, C_A = 120pF.

The compensation is optimized for use with 3x100µF or 4x100µF 1206, X5R ceramic output capacitors.

In exceptional cases, modifications to the compensation might be required. The EV1380QI's compensation can be modified for specific applications. For more information, contact Power Applications support.



$R_A = 40{,}000 \cdot VDDQ$ (value in Ω)

$C_A = \frac{8 \times 10^{-6}}{R_A}$ (C_A/R_A in F/Ω)

Round C_A down to closest standard value lower than calculated value.

$R_B = 4 \cdot R_A$ (V_{FB} is 0.6V nominal)

$R_1 = 3k\Omega$

Figure 6: External Feedback and Compensation Network

Enable Operation

The ENABLE pin should be tied to VDDQ through an 0201 resistor. With the device input power applied, the device automatically starts to operate with a soft-start, provided the AVIN voltage is above the upper UVLO high threshold of ~2.2 volts.

Input Capacitor Selection

The EV1380QI requires between 80uF and 100uF of input capacitance. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used because these dielectrics lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors maybe needed in parallel with the larger capacitors in order to provide high frequency decoupling.

Recommended Input Capacitors

Description	MFG	P/N
47uF, 10V, X5R, 1206	Taiyo Yuden	LMK316BJ476ML-T
47uF, 4V, X5R, 0805	Murata	GRM21BR60G476M
100uF, 6.3V, X5R, 1206	Murata	GRM31CR60J107M

Output Capacitor Selection

The EV1380QI has been optimized for use with an output capacitance of 300–400µF. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Recommended Output Capacitors

Description	MFG	P/N
47uF, 10V, X5R, 1206	Taiyo Yuden	LMK316BJ476ML-T
47uF, 6.3V, X5R, 1206	Taiyo Yuden Murata	JMK316BJ476ML-T GRM31CR60J476ME19L
100uF, 6.3V, X5R, 1206	Murata	GRM31CR60J107M

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. At the 1.5MHz switching frequency output impedance, denoted as Z, is comprised mainly of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing multiple capacitors in parallel reduces the impedance and hence will result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Typical Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p) VDDQ = 1.5V, V_{OUT} = 0.75V
3 x 100 uF	<10mV

Ternary Pins

M_S is a Ternary pin. This pin can assume three states – A low state, a high state and a float state. Device operation is controlled by the state of the pin. The pins may be pulled to ground or left floating without any special care. However when pulling high, it is recommended that this pin is tied to VIN with a series resistor. Using the equations in Figure 7, the resistor value may be optimized to reduce the current drawn by the pin.

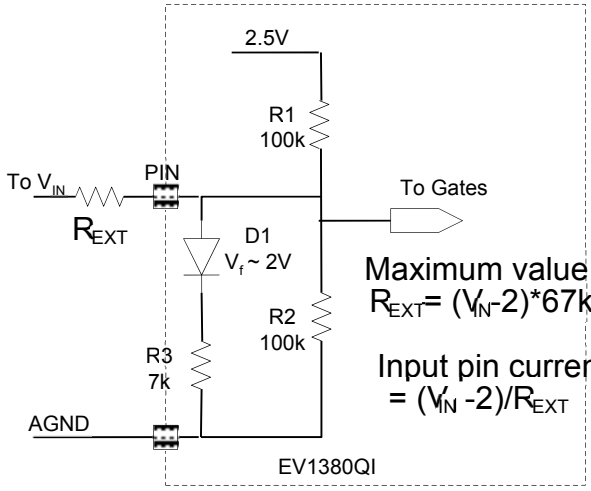


Figure 7: Selection of R_{EXT} to Connect Ternary Pins to V_{IN}

M_S (Master/Slave) Pin States

M_S Pin	Function
Low	This is Master mode. Switching phase locked to S_IN external clock. S_OUT outputs a delayed version of internal PWM signal
Float	Parallel operation is disabled. Switching phase locked to S_IN external clock. S_OUT outputs a delayed version of switching clock
High	This is Slave mode. The S_IN signal directly drives the power FETs. S_OUT outputs a delayed version of S_IN

NOTE: Power Applications support can be contacted for additional information on the Parallel operation of up to two EV1380QIs for high output current.

Layout Recommendations

Figure 8 and Figure 9 shows critical components along with top and bottom traces of a recommended minimum footprint of the EV1380QI layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files at www.altera.com/enpirion for exact dimensions and other layers. Please refer to Figures 8 and 9 while reading the layout recommendations in this section.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EV1380QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EV1380QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: There are a total of seven PGND pins dedicated to the input and output circuits. The input and output ground currents should be separated with a slit until they reach the seven PGND pins to help minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files at www.altera.com/enpirion.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible.

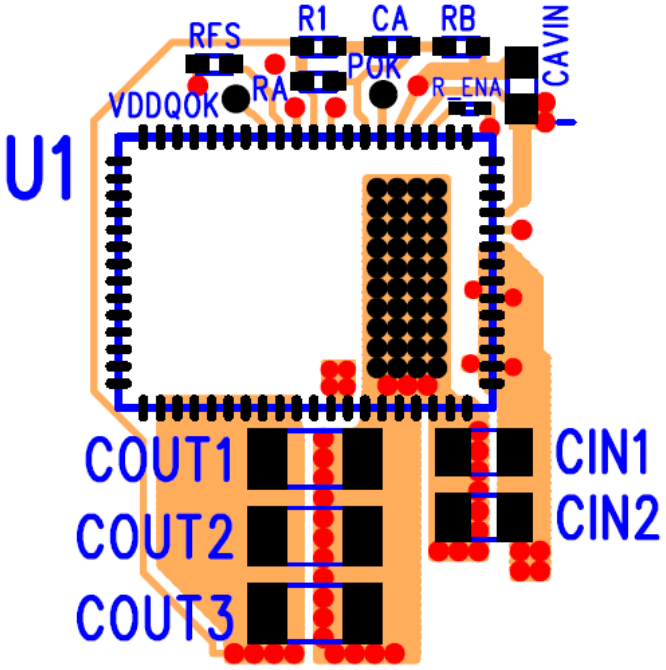


Figure 8: Top PCB Layer with Critical Components and Copper for Minimum Footprint (Top View)

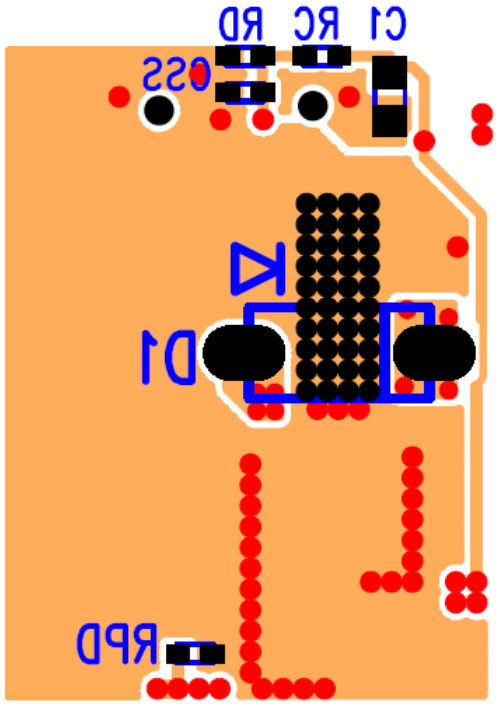


Figure 9: Bottom PCB Layer with Critical Components and Copper for Minimum Footprint (Top View)

The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figures 8, 9, 10, and 11.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 8 and Figure 9. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN1 and AVIN2 are the power supplies for the internal small-signal control circuits. AVIN1 and AVIN2 should be powered by an external supply. In Figure 8, the filter capacitor C_{AVIN} is connected closely from the AVIN1 and AVIN2 pins to AGND for proper filtering of the control circuit.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 8. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense trace to R_A should come just after the last output filter capacitor COUT2. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 9: Keep R_A, C_A, R1 and R_B close to the VFB pin (see Figure 8). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Recommendation 10: Connect AGND to the ground plane through a single via as close to the AGND pin as possible. This establishes the connection between AGND and PGND.

Recommendation 11: The VREF pin sets the reference voltage for VOUT and should be as clean as possible. The connection from VDDQ to VREF should begin from the CIN input capacitor to VREF through a resistor voltage divider (R_C, R_D). The soft-start capacitor C_{SS}, R_C, and R_D form a low-pass RC filter for the VREF pin. A bypass capacitor C1 should be placed close to the R_C resistor for additional filtering. The long trace from VDDQ to C1 forms a low-pass LC filter with C1 and helps further reduce noise coupling to VREF.

Recommendation 12: The Schottky diode D1 should be connected with anode to SW and cathode to VDDQ with very low inductance traces. Place D1 directly under the device as shown in Figure 9. Vias near SW and VDDQ connect these pins to the D1 terminals. The recommended diode for this layout is ST Microelectronics TMBYV10-40FILM. Contact Power Applications support for alternate options for this diode.

Recommendation 13: Altera provides schematic and layout reviews for all customer designs. It is highly recommended for all customers to take advantage of this service. Please send pdf schematic files and Gerber layout files of the power section to your local sales contact or to Power Applications support.

Design Considerations

Exposed Metal on Bottom of Package

Package lead frames offer advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. They do, however, require some special considerations.

In the assembly process, lead-frame construction requires-for mechanical support-that some of the lead-frame cantilevers be exposed at the point where wire-bonds or internal passives are attached. Because of this lead frame requirement, several small pads are exposed on the bottom of the package. Only the large thermal pad and the perimeter pads should be mechanically or electrically connected to the PC board. The PCB top layer under the EV1380QI should be clear of any metal except for the large thermal pad. The "grayed-out" area in Figure 10 represents the area that should be clear of all metal (traces, vias, or planes) on the top layer of the PCB.

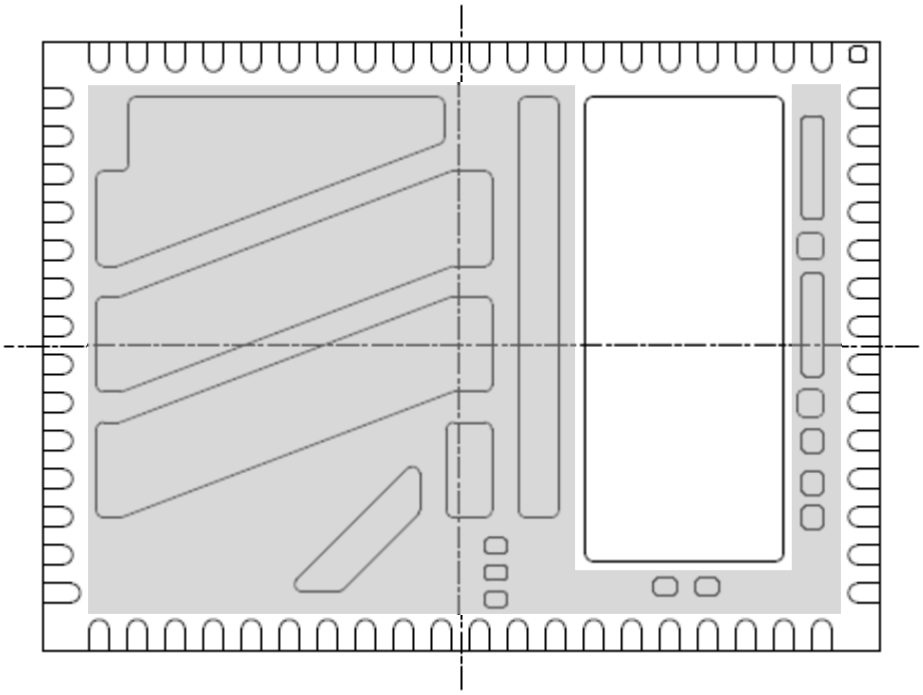


Figure 10: Lead-Frame Exposed Metal. Gray area highlights exposed metal below which there should not be any metal (traces, vias, or planes) on the top layer of the PCB

Recommended PCB Footprint

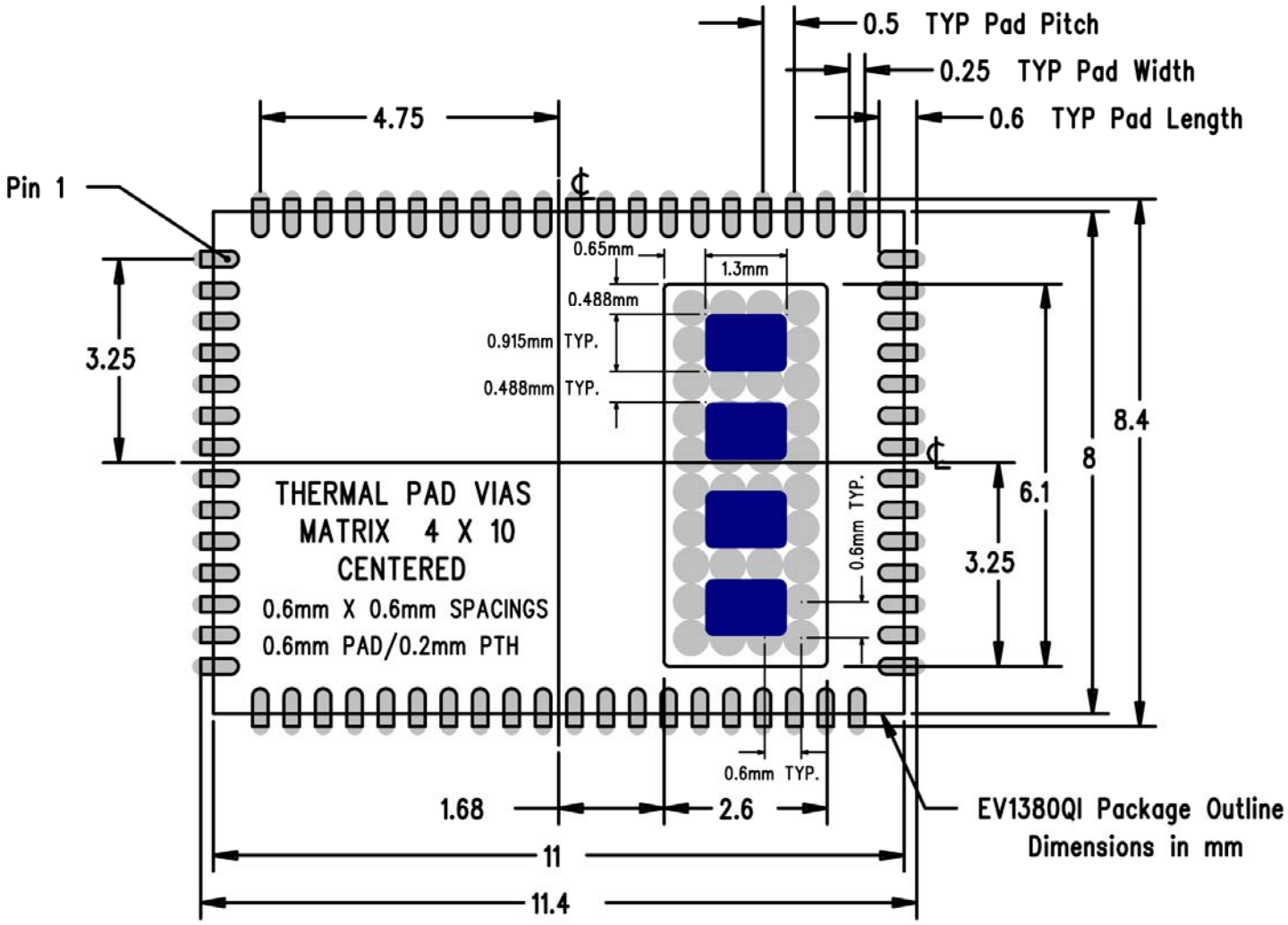


Figure 11: EV1380QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

Package and Mechanical

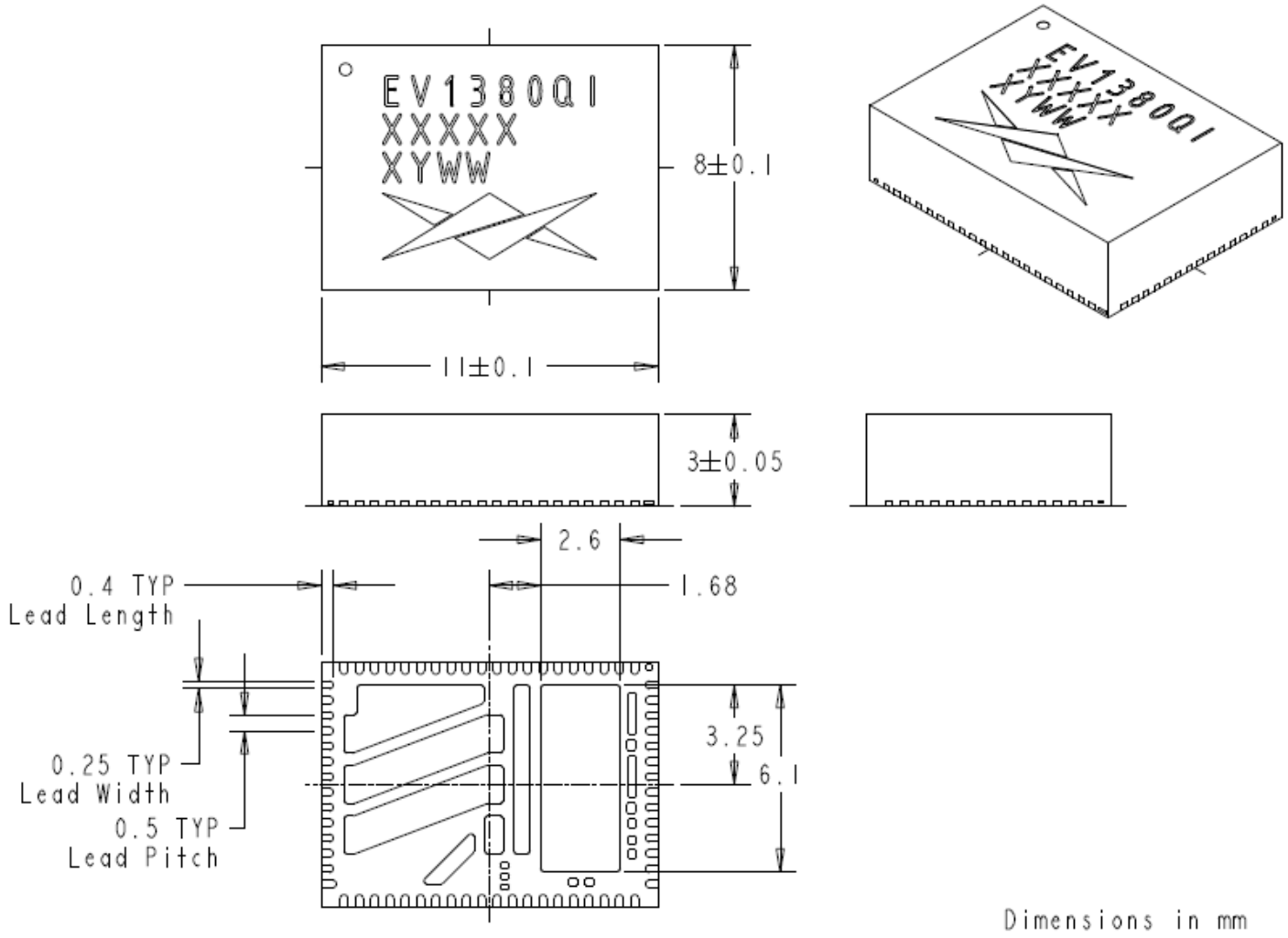


Figure 12: EV1380 Package Dimensions

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