10-Bit, 65/80/105 MSPS Dual A/D Converter

AD9216

FEATURES

Integrated dual 10-bit ADC
Single 3 V supply operation
SNR = 57.6 dBc (to Nyquist, AD9216-105)
SFDR = 74 dBc (to Nyquist, AD9216-105)
Low power: 150 mW/ch at 105 MSPS
Differential input with 300 MHz 3 dB bandwidth
Exceptional crosstalk immunity < -80 dB
Offset binary or twos complement data format
Clock duty cycle stabilizer

APPLICATIONS

Ultrasound equipment
IF sampling in communications receivers
3G, radio point-to-point, LMDS, MMDS
Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes

GENERAL DESCRIPTION

The AD9216 is a dual, 3 V, 10-bit, 105 MSPS analog-to-digital converter (ADC). It features dual high performance sample-and-hold amplifiers (SHAs) and an integrated voltage reference. The AD9216 uses a multistage differential pipelined architecture with output error correction logic to provide 10-bit accuracy and guarantee no missing codes over the full operating temperature range at up to 105 MSPS data rates. The wide bandwidth, differential SHA allows for a variety of user selectable input ranges and offsets, including single-ended applications. The AD9216 is suitable for various applications, including multiplexed systems that switch full-scale voltage levels in successive channels and for sampling inputs at frequencies well beyond the Nyquist rate.

Dual single-ended clock inputs are used to control all internal conversion cycles. A duty cycle stabilizer is available on the AD9216 and can compensate for wide variations in the clock duty cycle, allowing the converters to maintain excellent performance. The digital output data is presented in either straight binary or twos complement format.

FUNCTIONAL BLOCK DIAGRAM

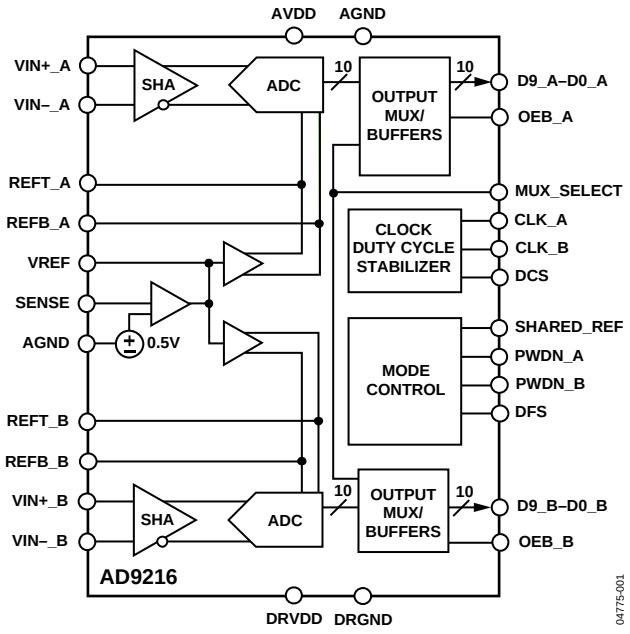

Figure 1.

Fabricated on an advanced CMOS process, the AD9216 is available in a space saving, Pb-free, 64-lead LFCSP (9 mm × 9 mm) and is specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Pin compatible with AD9238, dual 12-bit 20 MSPS/40 MSPS/65 MSPS ADC and AD9248, dual 14-bit 20 MSPS/40 MSPS/65 MSPS ADC.
2. 105 MSPS capability allows for demanding, high frequency applications.
3. Low power consumption: AD9216–105: 105 MSPS = 300 mW.
4. The patented SHA input maintains excellent performance for input frequencies up to 200 MHz and can be configured for single-ended or differential operation.
5. Typical channel crosstalk of < –80 dB at f_{IN} up to 70 MHz.
6. The clock duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

Rev. A

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SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9216BCPZ-65 Min	AD9216BCPZ-65 Typ	AD9216BCPZ-65 Max	AD9216BCPZ-80 Min	AD9216BCPZ-80 Typ	AD9216BCPZ-80 Max	AD9216BCPZ-105 Min	AD9216BCPZ-105 Typ	AD9216BCPZ-105 Max	Unit
RESOLUTION	Full	VI	10			10			10			Bits
ACCURACY												
No Missing Codes	Full	VI	Guaranteed			Guaranteed			Guaranteed			
Offset Error	Full	VI	-1.9	±0.3	+1.9	-1.9	±0.3	+1.9	−2.2	±0.3	+2.2	% FSR
Gain Error[1]	25°C	VI	-1.6	±0.4	+1.6	-1.6	±0.4	+1.6	−1.6	±0.4	+1.6	% FSR
Differential Nonlinearity (DNL)[2]	Full	IV	-1.0	±0.3	+1.0	-1.0	±0.4	+1.0	−1.0	±0.5	+1.0	LSB
	25°C	I	-0.9	±0.3	+0.9	-0.9	±0.4	+0.9	−1.0	±0.5	+1.0	LSB
Integral Nonlinearity (INL)[2]	Full	IV	-1.4	±0.5	+1.4	-1.6	±0.5	+1.6	−2.5	±1.0	+2.5	LSB
	25°C	I	-1.0	±0.5	+1.0	-1.1	±0.5	+1.1	−1.5	±1.0	+1.5	LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±10			±10			±10		µV/°C
Gain Error[1]	Full	V		±75			±75			±75		ppm/°C
Reference Voltage	Full	V		±15			±15			±15		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error	Full	VI		±2	±35		±2	±35		±2	±35	mV
Load Regulation @ 1.0 mA	25°C	V		1.0			1.0			1.0		mV
INPUT REFERRED NOISE												
Input Span = 2.0 V	25°C	V		0.5			0.5			0.5		LSB_{rms}
ANALOG INPUT												
Input Span, VREF = 1.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	25°C	V		2			2			2		pF
REFERENCE INPUT RESISTANCE	25°C	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.3	2.7	3.0	3.3	2.7	3.0	3.3	V
DRVDD	Full	IV	2.25	2.5	3.3	2.25	2.5	3.3	2.25	2.5	3.3	V
Supply Current												
IAVDD[4]	Full	VI		72	80		78	85		100	110	mA
IDRVDD[4]	Full	VI		15			18			24		mA
PSRR	25°C	V		±0.1			±0.1			±0.1		% FSR
POWER CONSUMPTION												
P_{AVDD}[4]	25°C	I		216	240		234	255		300	330	mW
P_{DRVDD}[4]	25°C	V		38			45			60		mW
Standby Power[5]	25°C	V		3.0			3.0			3.0		mW
MATCHING CHARACTERISTICS												
Offset Matching Error[6]	25°C	I	-2.6	±0.2	+2.6	-2.6	±0.2	+2.6	−3.5	±0.3	+3.5	% FSR
Gain Matching Error (Shared Reference Mode)	25°C	I	-0.4	±0.1	+0.4	-0.4	±0.1	+0.4	−0.6	±0.1	+0.6	% FSR
Gain Matching Error (Nonshared Reference Mode)	25°C	I	-1.6	±0.1	+1.6	-1.6	±0.1	+1.6	−1.6	±0.3	+1.6	% FSR

[1] Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).
[2] Measured with low frequency ramp at maximum clock rate.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AVSS. Refer to Figure 37 for the equivalent analog input structure.
[4] Measured with low frequency analog input at maximum clock rate with approximately 5 pF loading on each output bit.
[5] Standby power is measured with the CLK_A and CLK_B pins inactive (that is, set to AVDD or AGND).
[6] Both shared reference mode and nonshared reference mode.

AC SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	AD9216BCPZ-65 Min	AD9216BCPZ-65 Typ	AD9216BCPZ-65 Max	AD9216BCPZ-80 Min	AD9216BCPZ-80 Typ	AD9216BCPZ-80 Max	AD9216BCPZ-105 Min	AD9216BCPZ-105 Typ	AD9216BCPZ-105 Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)												
f_{INPUT} = 2.4 MHz	25°C	V		58.6			58.5			58.0		dB
f_{INPUT} = Nyquist[1]	Full	IV	56.6	58.4		55.9	58.1		54.8	57.6		dB
	25°C	I	57.2	58.4		56.4	58.5		56.4	57.6		dB
f_{INPUT} = 69 MHz	25°C	V		58.0			58.0			57.4		dB
f_{INPUT} = 100 MHz	25°C	V		57.5			57.5			57.3		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)												
f_{INPUT} = 2.4 MHz	25°C	V		58.5			58.2			57.8		dB
f_{INPUT} = Nyquist[1]	Full	IV	56.4	58.3		55.4	58.0		53.4	57.4		dB
	25°C	I	57.0	58.3		56.2	58.0		56.1	57.4		dB
f_{INPUT} = 69 MHz	25°C	V		57.5			57.5			56.8		dB
f_{INPUT} = 100 MHz	25°C	V		57.0			57.0			56.7		dB
EFFECTIVE NUMBER OF BITS (ENOB)												
f_{INPUT} = 2.4 MHz	25°C	V		9.4			9.4			9.3		Bits
f_{INPUT} = Nyquist[1]	Full	IV	9.1	9.4		8.9	9.3		8.6	9.3		Bits
	25°C	I	9.2	9.4		9.0	9.3		9.1	9.3		Bits
f_{INPUT} = 69 MHz	25°C	V		9.3			9.3			9.2		Bits
f_{INPUT} = 100 MHz	25°C	V		9.3			9.3			9.2		Bits
WORST HARMONIC (SECOND OR THIRD)												
f_{INPUT} = 2.4 MHz	Full	IV		−82.0			−81.0			−76.0		dBc
f_{INPUT} = Nyquist[1]	Full	IV		−79.5	-65.1		−77.0	-64.1		−74.0	−60.0	dBc
	25°C	I		−79.5	-67.8		−77.0	-67.2		−74.0	−66.5	dBc
f_{INPUT} = 69 MHz	25°C	V		−79.0			−76.5			−74.0		dBc
f_{INPUT} = 100 MHz	25°C	V		−78.5			−76.0			−74.0		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)												
f_{INPUT} = 2.4 MHz	Full	IV		−82.5			−81.5			−76.5		dBc
f_{INPUT} = Nyquist[1]	Full	IV		−80.5	-65.8		−78.0	-64.5		−75.0	−62.0	dBc
	25°C	I		−80.5	-68.7		−78.0	-67.8		−75.0	−67.5	dBc
f_{INPUT} = 69 MHz	25°C	V		−80.0			−77.5			−75.0		dBc
f_{INPUT} = 100 MHz	25°C	V		−79.5			−77.0			−75.0		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)												
f_{INPUT} = 2.4 MHz	Full	IV		82.0			81.0			76.0		dBc
f_{INPUT} = Nyquist[1]	Full	IV	65.1	79.5		64.1	77.0		60.0	74.0		dBc
	25°C	I	67.8	79.5		67.2	77.0		66.5	74.0		dBc
f_{INPUT} = 69 MHz	25°C	V		79.0			76.5			74.0		dBc
f_{INPUT} = 100 MHz	25°C	V		78.5			76.0			74.0		dBc
TWO-TONE SFDR (A_{IN} = −7 dBFS)												
f_{IN1} = 69.1 MHz, f_{IN2} = 70.1 MHz	25°C	V		71.0			70.0			70.0		dBc
f_{IN1} = 100.1 MHz, f_{IN2} = 101.1 MHz	25°C	V		70.0			69.0			69.0		dBc
ANALOG BANDWIDTH	25°C	V		300			300			300		MHz
CROSSTALK	25°C	V		−80.0			−80.0			−80.0		dB

[1] Nyquist = approximately 32 MHz, 40MHz, 50MHz for the −65, −80, and −105 grades respectively

LOGIC SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	AD9216BCPZ-65			AD9216BCPZ-80			AD9216BCPZ-105			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LOGIC INPUTS												
High Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High Level Input Current	Full	IV	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	Full	IV	−10		+10	−10		+10	−10		+10	µA
Input Capacitance	Full	IV		2			2			2		pF
LOGIC OUTPUTS[1]												
DRVDD = 2.5 V												
High Level Output Voltage	Full	IV	2.45			2.45			2.45			V
Low Level Output Voltage	Full	IV			0.05			0.05			0.05	V

[1] Output voltage levels measured with 5 pF load on each output.

SWITCHING SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 4.

			AD9216BCPZ-65			AD9216BCPZ-80			AD9216BCPZ-105			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	65			80			105			MSPS
Minimum Conversion Rate	Full	IV			10			10			10	MSPS
CLK Period	Full	VI	15.4			12.5			9.5			nS
CLK Pulse Width High	Full	VI	4.6			4.4			3.8			nS
CLK Pulse Width Low	Full	VI	4.6			4.4			3.8			nS
OUTPUT PARAMETERS[1]												
Output Propagation Delay[2] (t_{PD})	25°C	I		4.5	6.4		4.5	6.4		4.5	6.4	nS
Valid Time[3] (t_V)	25°C	I	2.0			2.0			2.0			
Output Rise Time (10% to 90%)	25°C	V		1.0			1.0			1.0		nS
Output Fall Time (10% to 90%)	25°C	V		1.0			1.0			1.0		nS
Output Enable Time[4]	Full	IV			1			1			1	Cycle
Output Disable Time[4]	Full	IV			1			1			1	Cycle
Pipeline Delay (Latency)	Full	IV		6			6			6		Cycle
APERTURE												
Aperture Delay (t_A)	25°C	V		1.5			1.5			1.5		nS
Aperture Uncertainty (t_J)	25°C	V		0.5			0.5			0.5		pS $_{rms}$
Wake-Up Time[5]	25°C	V		7			7			7		ms
OUT-OF-RANGE RECOVERY TIME	25°C	V		1			1			1		Cycle

[1] C_{LOAD} equals 5 pF maximum for all output switching parameters.
[2] Output delay is measured from clock 50% transition to data 50% transition.
[3] Valid time is approximately equal to the minimum output propagation delay.
[4] Output enable time is OEB_A, OEB_B falling to respective channel outputs coming out of high impedance. Output disable time is OEB_A, OEB_B rising to respective channel outputs going into high impedance.
[5] Wake-up time is dependent on value of decoupling capacitors; typical values shown for 0.1 µF and 10 µF capacitors on REFT and REFB.

TIMING DIAGRAM

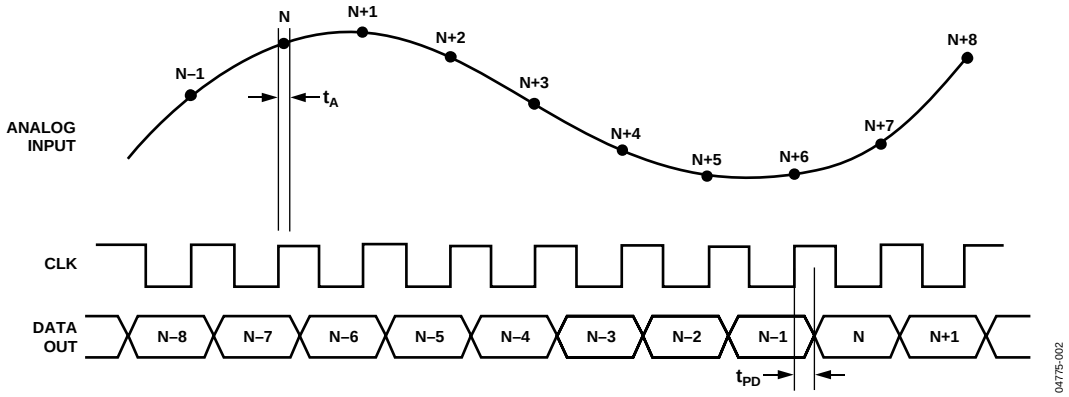

Figure 2.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	To	Rating
ELECTRICAL		
AVDD	AGND	−0.3 V to +3.9 V
DRVDD	DRGND	−0.3 V to +3.9 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD	DRVDD	−0.3 V to +3.9 V
Digital Outputs	DRGND	−0.3 V to DRVDD + 0.3 V
CLK_A, CLK_B, DCS, DFS, MUX_SELECT, OEB_A, OEB_B, SHARED_REF, PDWN_A, PDWN_B	AGND	−0.3 V to AVDD + 0.3 V
VIN−_A, VIN+_A, VIN−_B, VIN+_B	AGND	−0.3 V to AVDD + 0.3 V
REFT_A, REFB_A,VREF, REFT_B, REFB_B, SENSE	AGND	−0.3 V to AVDD + 0.3 V
ENVIRONMENTAL[1]		
Operating Temperature		−40°C to +85°C
Junction Temperature		150°C
Lead Temperature (10 sec)		300°C
Storage Temperature		−65°C to +150°C

[1] Typical thermal impedances (64-lead LFCSP); θ_{JA} = 26.4°C/W. These measurements were taken on a 4-layer board (with thermal via array) in still air, in accordance with EIA/JESD51-7.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Table 6.

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

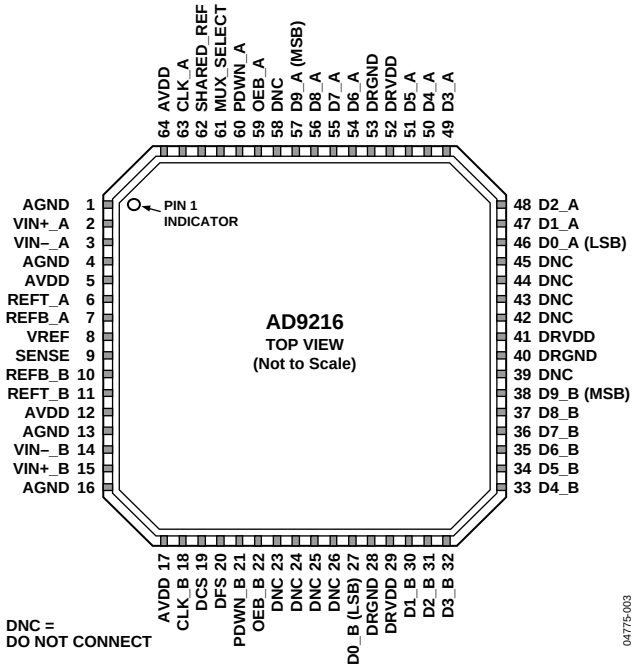

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 13, 16	AGND[1]	Analog Ground.
2	VIN+_A	Analog Input Pin (+) for Channel A.
3	VIN−_A	Analog Input Pin (−) for Channel A.
5, 12, 17, 64	AVDD	Analog Power Supply.
6	REFT_A	Differential Reference (+) for Channel A.
7	REFB_A	Differential Reference (−) for Channel A.
8	VREF	Voltage Reference Input/Output.
9	SENSE	Reference Mode Selection.
10	REFB_B	Differential Reference (−) for Channel B.
11	REFT_B	Differential Reference (+) for Channel B.
14	VIN−_B	Analog Input Pin (−) for Channel B.
15	VIN+_B	Analog Input Pin (+) for Channel B.
18	CLK_B	Clock Input Pin for Channel B.
19	DCS	Duty Cycle Stabilizer (DCS) Mode Pin (Active High).
20	DFS	Data Output Format Select Pin. Low for offset binary; high for twos complement.
21	PDWN_B	Power-Down Function Selection for Channel B. Logic 0 enables Channel B. Logic 1 powers down Channel B. (Outputs static, not High-Z.)
22	OEB_B	Output Enable for Channel B. Logic 0 enables Data Bus B. Logic 1 sets outputs to High-Z.
23 to 26, 39, 42 to 45, 58	DNC	Do Not Connect Pins. Should be left floating.
27, 30 to 38	D0_B (LSB) to D9_B (MSB)	Channel B Data Output Bits.
28, 40, 53	DRGND	Digital Output Ground.
29, 41, 52	DRVDD	Digital Output Driver Supply. Must be decoupled to DRGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF capacitor in parallel with 10 µF.

Pin No.	Mnemonic	Description
46 to 51, 54 to 57	D0_A (LSB) to D9_A (MSB)	Channel A Data Output Bits.
59	OEB_A	Output Enable for Channel A. Logic 0 enables Data Bus A. Logic 1 sets outputs to High-Z.
60	PDWN_A	Power-Down Function Selection for Channel A. Logic 0 enables Channel A. Logic 1 powers down Channel A. (Outputs static, not High-Z.)
61	MUX_SELECT	Data Multiplexed Mode. (See Data Format section for how to enable.)
62	SHARED_REF	Shared Reference Control Bit. Low for independent reference mode; high for shared reference mode.
63	CLK_A	Clock Input Pin for Channel A.

[1] It is recommended that all ground pins (AGND and DRGND) be tied to a common ground plane.

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the encode command and the instant the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle
Pulse-width high is the minimum amount of time that the clock pulse should be left in a Logic 1 state to achieve rated performance; pulse-width low is the minimum time clock pulse should be left in a low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Crosstalk
Coupling onto one channel being driven by a low level (−40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180° and by taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
The ENOB is calculated from the measured SINAD based on the equation (assuming full-scale input)

$$ENOB = \frac{SINAD_{MEASURED} - 1.76\ \text{dB}}{6.02}$$

Full-Scale Input Power
Expressed in dBm and computed using the following equation.

$$Power_{FULL\ SCALE} = 10 \log \left(\frac{\frac{V^2{}_{FULL\ SCALE}\ rms}{Z_{INPUT}}}{0.001} \right)$$

Gain Error
The difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a 50% crossing of the CLK rising edge and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)
This value includes both thermal and quantization noise.

$$V_{noise} = \sqrt{Z \times 0.001 \times 10\left(\frac{FS_{\mathrm{dBm}} - SNR_{\mathrm{dBc}} - Signal_{\mathrm{dBFS}}}{10}\right)}$$

where:

Z is the input impedance.

FS is the full scale of the device for the frequency in question.

SNR is the value for the particular input level.

Signal is the signal level within the ADC reported in dB below full scale.

Power Supply Rejection Ratio
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first seven harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (that is, degrades as signal level is lowered) or dBFS (that is, always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product, in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It also may be reported in dBc (that is, degrades as signal level is lowered) or in dBFS (that is, always relates back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic), reported in dBc.

Transient Response Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.0 V, DRVDD = 2.5 V, T = 25°C, A_{IN} differential drive, internal reference, DCS on, unless otherwise noted.

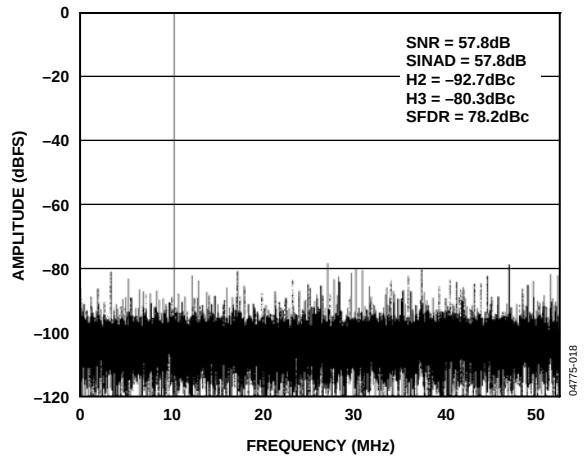

Figure 4. FFT: f_S = 105 MSPS, A_{IN} = 10.3 MHz at –0.5 dBFS (–105 Grade)

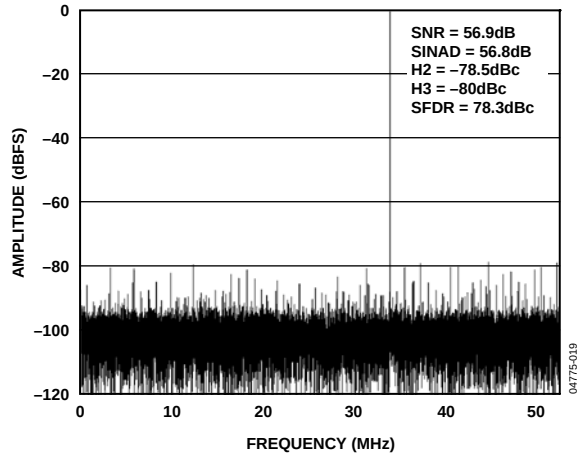

Figure 5. FFT: f_S = 105 MSPS, A_{IN} = 70 MHz at –0.5 dBFS (–105 Grade)

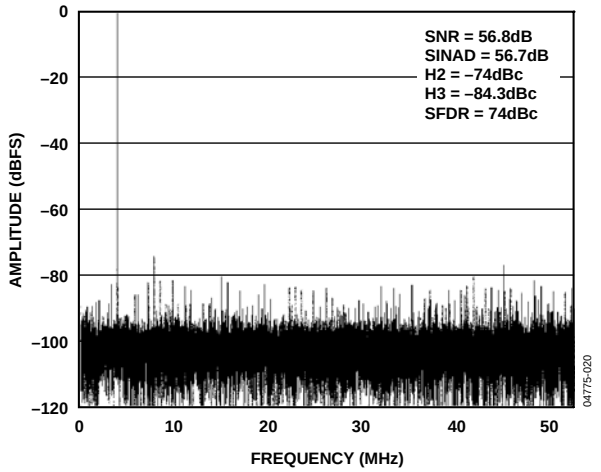

Figure 6. FFT: f_S = 105 MSPS, A_{IN} = 100 MHz at –0.5 dBFS (–105 Grade)

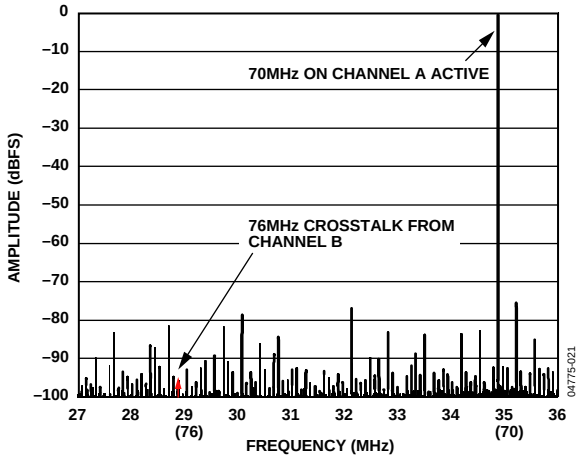

Figure 7. FFT: f_S = 105 MSPS, A_{IN} =70 MHz, 76 MHz (–105 Grade) (A Port FFT while Both A and B Ports Are Driven at –0.5 dBFS)

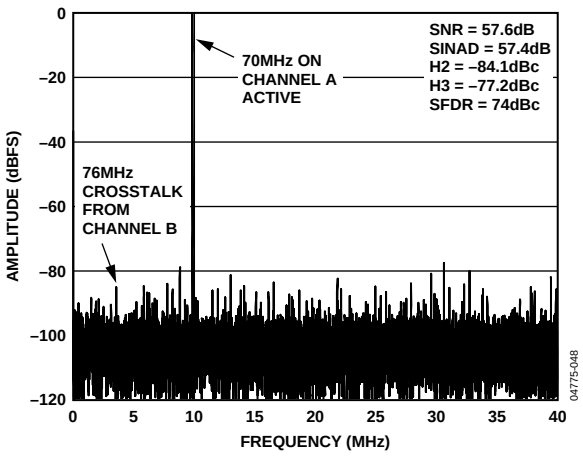

Figure 8. FFT: f_S = 80 MSPS, A_{IN} =70 MHz, 76 MHz (–80 Grade) (A Port FFT while Both A and B Ports Are Driven at –0.5 dBFS)

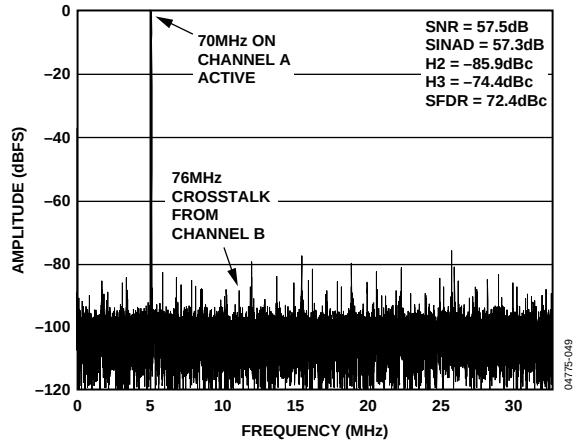

Figure 9. FFT: f_S = 65 MSPS, A_{IN} =70 MHz, 76 MHz (–65 Grade) (A Port FFT while Both A and B Ports Are Driven at –0.5 dBFS)

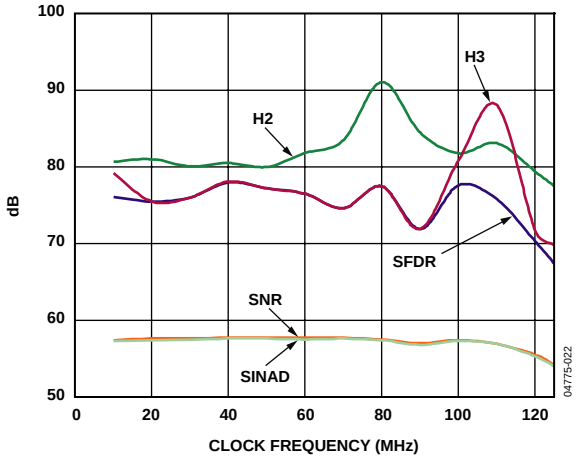

Figure 10. SNR, SINAD, H2, H3, SFDR vs. Sample Clock Frequency A_{IN} = 70 MHz at −0.5 dBFS (−105 Grade)

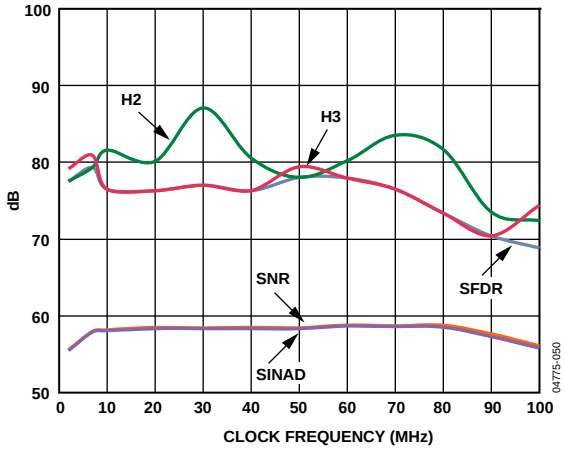

Figure 11. SNR, SINAD, H2, H3, SFDR vs. Sample Clock Frequency, A_{IN} = 70 MHz at −0.5 dBFS (−65/80 Grade)

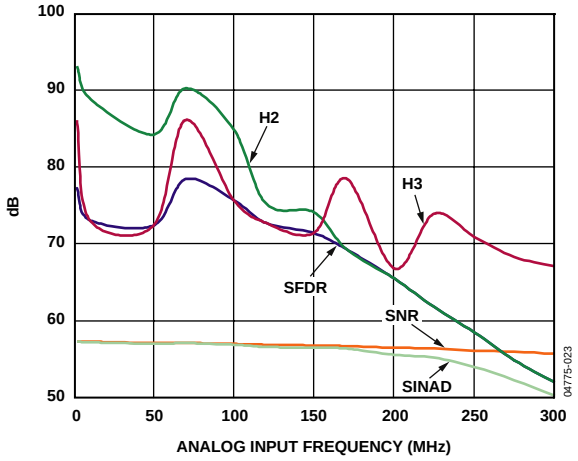

Figure 12. Analog Input Frequency Sweep, AIN = −0.5 dBFS, f_S = 105 MSPS (−105 Grade)

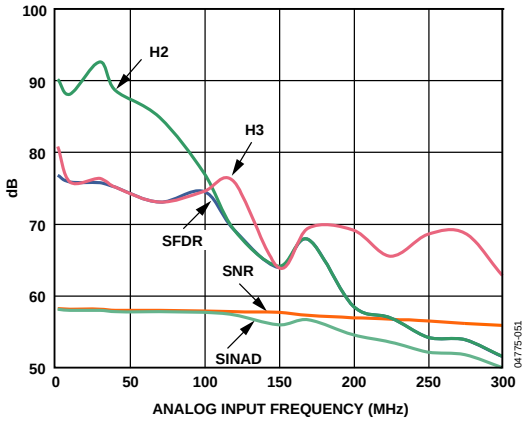

Figure 13. Analog Input Frequency Sweep, A_{IN} = −0.5 dBFS, f_S = 80 MSPS (−80 Grade)

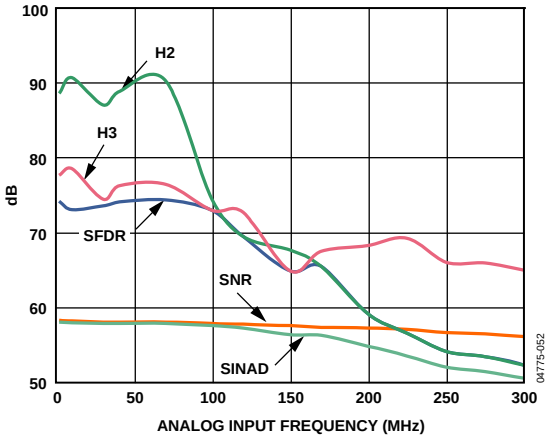

Figure 14. Analog Input Frequency Sweep, A_{IN} = −0.5 dBFS, f_S = 65 MSPS (−65 Grade)

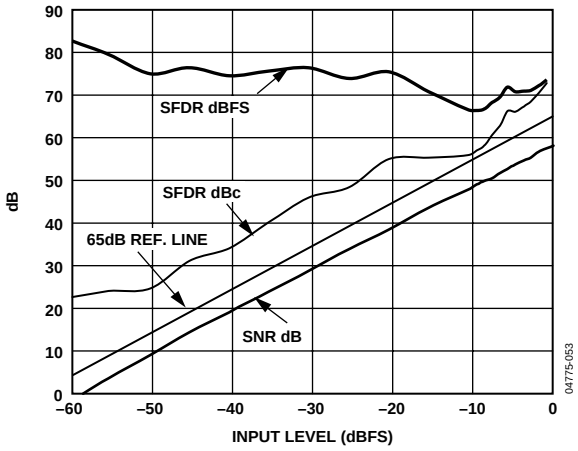

Figure 15. SFDR vs. Analog Input Level, A_{IN} = 70 MHz, f_S = 105 MSPS (−105 Grade)

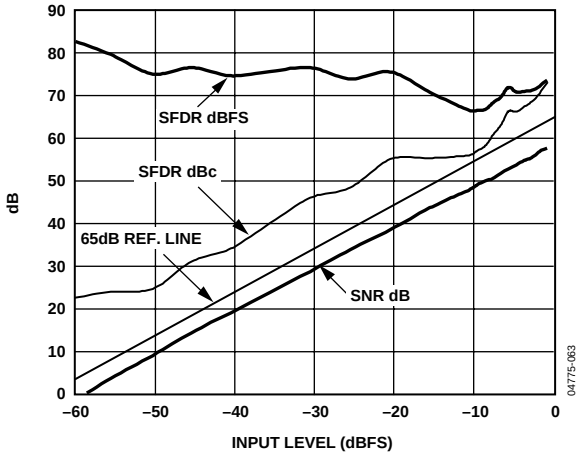

Figure 16. SFDR vs. Analog Input Level, A_{IN} = 70 MHz, f_S = 80 MSPS (−80 Grade)

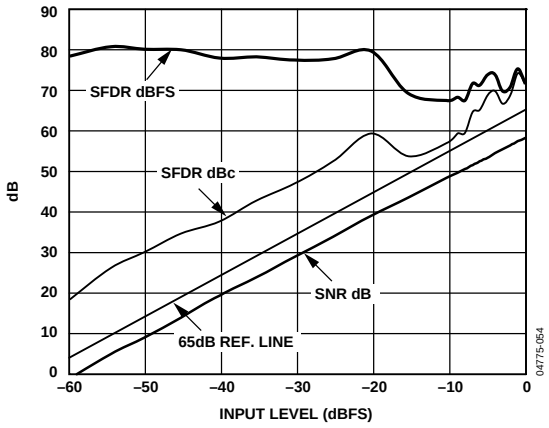

Figure 17. SFDR vs. Analog Input Level, A_{IN} = 70 MHz, f_S = 65 MSPS (−65 Grade)

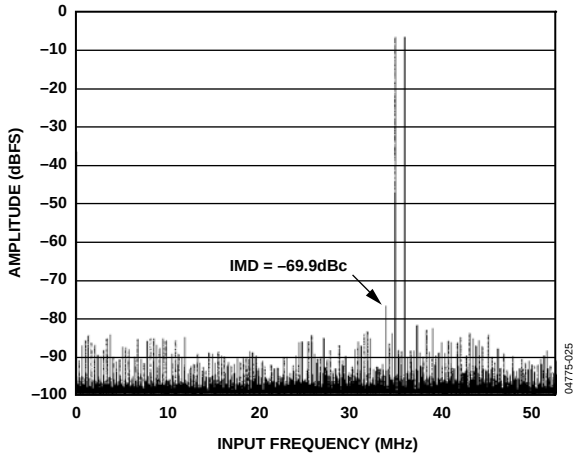

Figure 18. Two-Tone IMD Performance F1, F2 = 69.1 MHz, 70.1 MHz at −7 dBFS, 105 MSPS (−105 Grade)

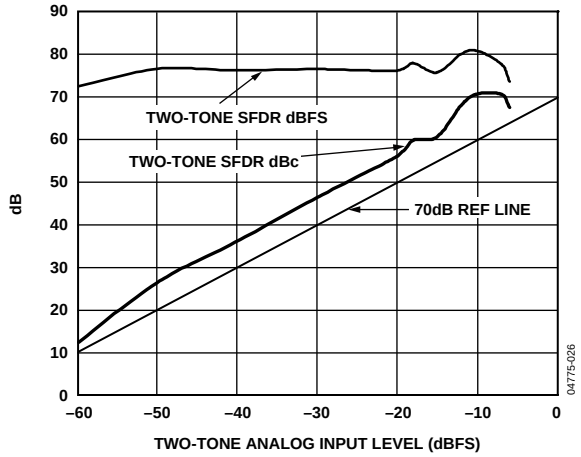

Figure 19. Two-Tone IMD Performance vs. Input Drive Level (69.1 MHz and 70.1 MHz; f_S = 105 MSPS (−105 Grade); F1, F2 Levels Equal)

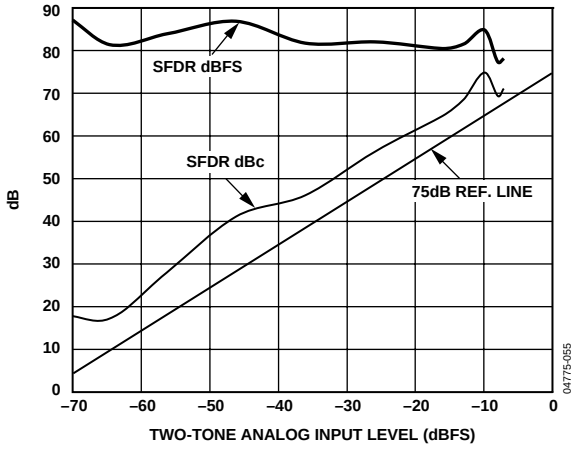

Figure 20. Two-Tone IMD Performance vs. Input Drive Level (69.1 MHz and 70.1 MHz; f_S = 80 MSPS (−80 Grade); F1, F2 Levels Equal)

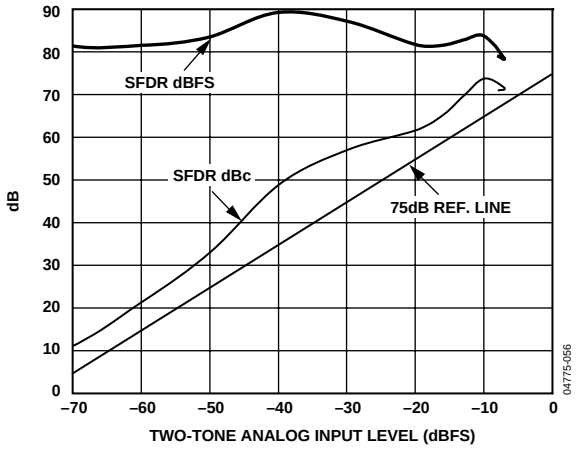

Figure 21. Two-Tone IMD Performance vs. Input Drive Level (69.1 MHz and 70.1 MHz; f_S = 65 MSPS (−65 Grade); F1, F2 Levels Equal)

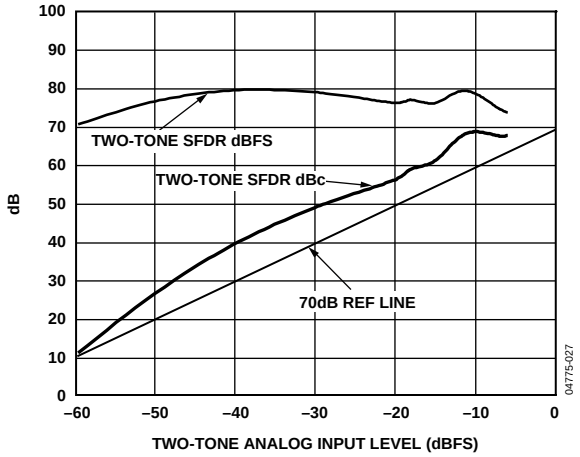

Figure 22. Two-Tone IMD Performance vs. Input Drive Level
(100.1 MHz and 101.1 MHz; f_S = 105 MSPS (−105 Grade); F1, F2 Levels Equal)

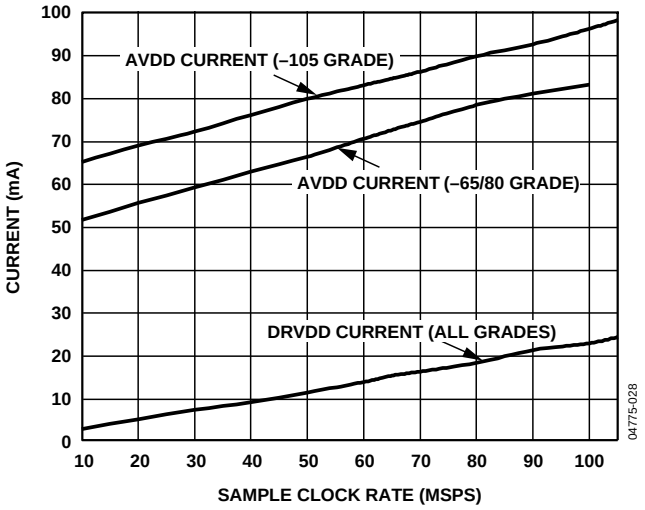

Figure 23. I_{AVDD}, I_{DRVDD} vs. Sample Clock Frequency,
C_{LOAD} = 5 pF, A_{IN} = 70 MHz @ –0.5 dBFS

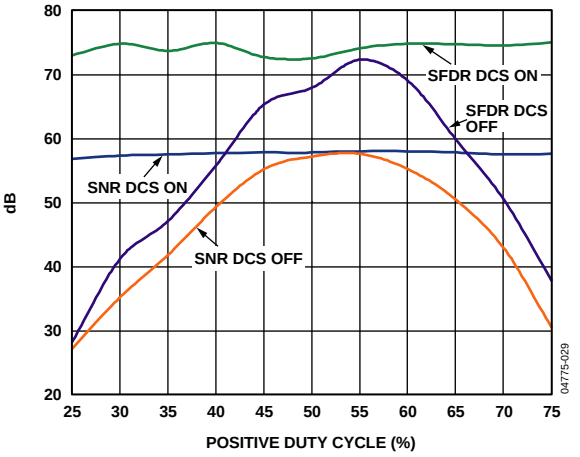

Figure 24. SNR, SFDR vs. Positive Duty Cycle DCS Enabled, Disabled;
A_{IN} = 70 MHz at –0.5 dBFS, 105 MSPS (−105 Grade)

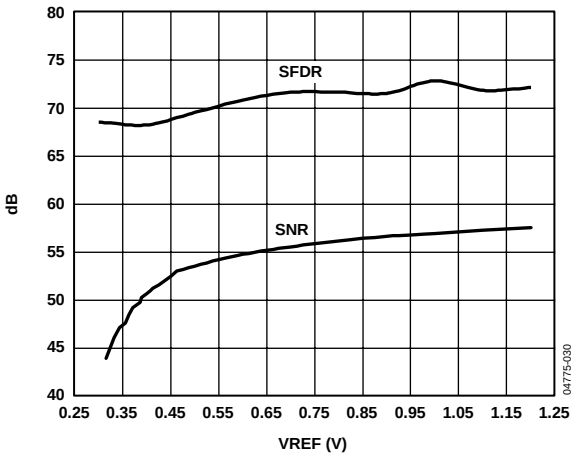

Figure 25. SNR, SFDR vs. External VREF (Full Scale = 2 × VREF)
A_{IN} = 70.3 MHz at –0.5 dBFS, 105 MSPS (−105 Grade)

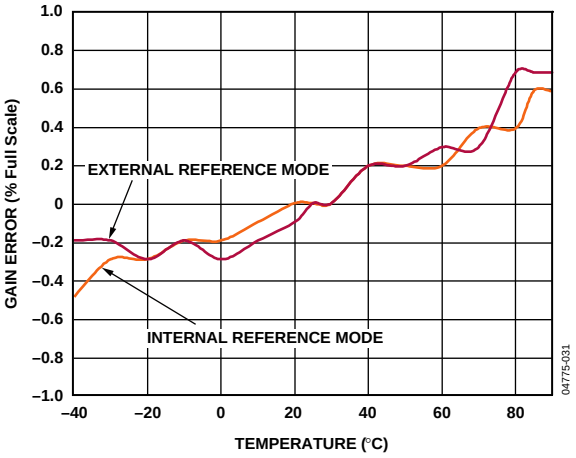

Figure 26. Typical Gain Error Variation vs. Temperature, (−105 Grade)
A_{IN} = 70 MHz at 0.5 dBFS, 105 MSPS (Normalized to 25°C)

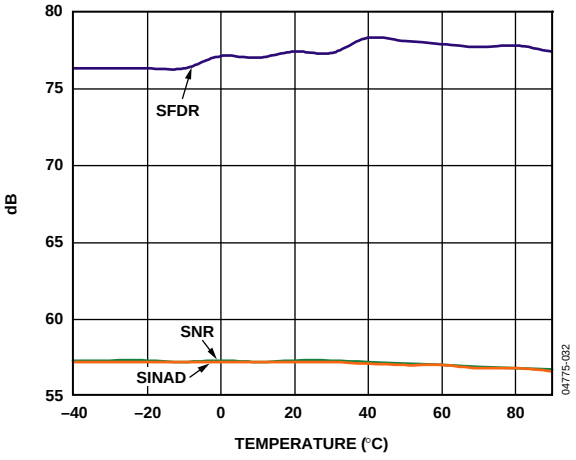

Figure 27. SNR, SINAD, SFDR vs. Temperature, (−105 Grade)
A_{IN} = 70 MHz at –0.5 dBFS, 105 MSPS, Internal Reference Mode

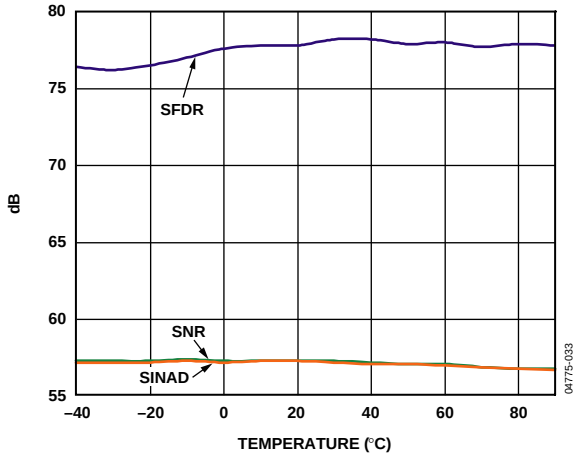

Figure 28. SNR, SINAD, SFDR vs. Temperature, (–105 Grade)
A_{IN} = 70 MHz at –0.5 dBFS, 105 MSPS , External Reference Mode

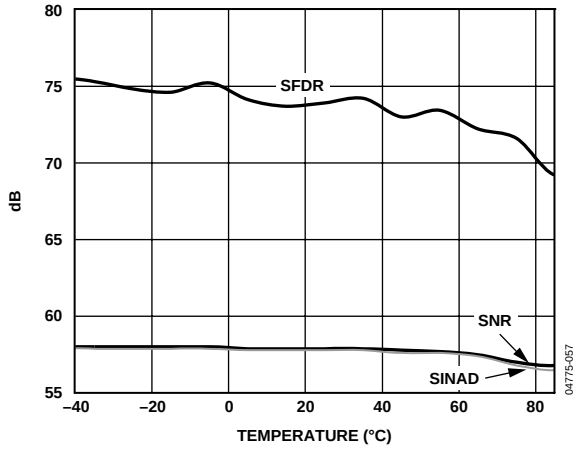

Figure 29. SNR, SINAD, SFDR vs. Temperature, (-80 Grade)
A_{IN} = 70 MHz at –0.5 dBFS, 80 MSPS, Internal Reference Mode

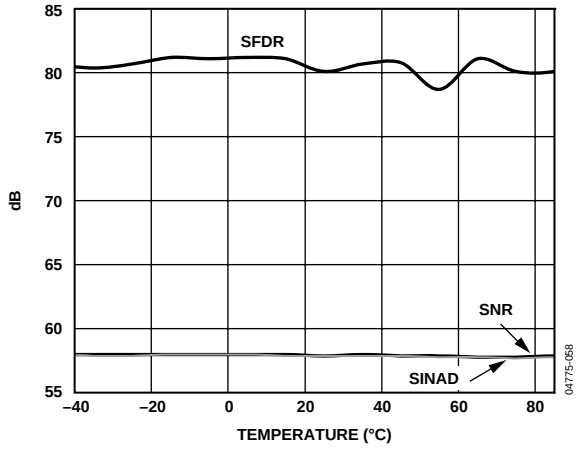

Figure 30. SNR, SINAD, SFDR vs. Temperature, (-65 Grade)
A_{IN} = 70 MHz at –0.5 dBFS, 65 MSPS,, Internal Reference Mode

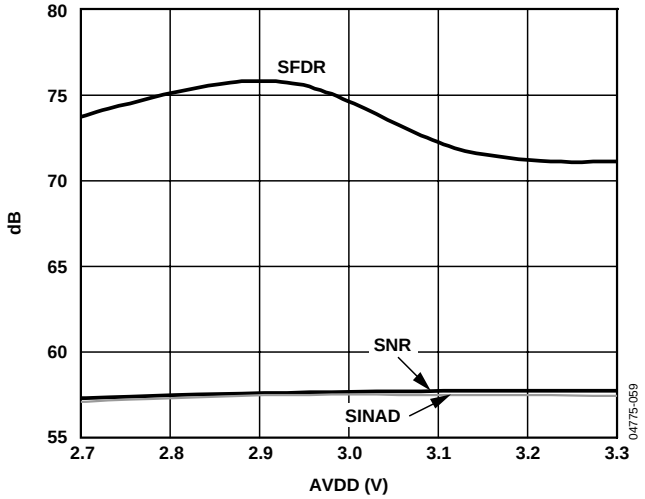

Figure 31. SNR, SINAD, SFDR vs. AVDD, A_{IN} = 70 MHz at –0.5 dBFS, 105 MSPS (–105 Grade)

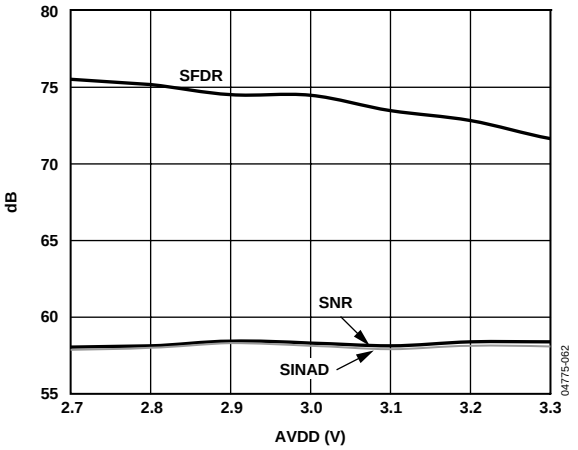

Figure 32. SNR, SINAD, SFDR vs. AVDD, A_{IN} = 70 MHz at –0.5 dBFS, 80 MSPS (–80 Grade)

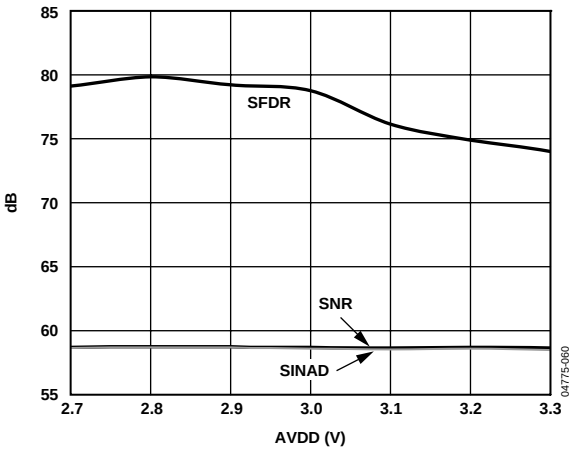

Figure 33. SNR, SINAD, SFDR vs. AVDD, A_{IN} = 70 MHz at –0.5 dBFS, 65MSPS (–65 Grade)

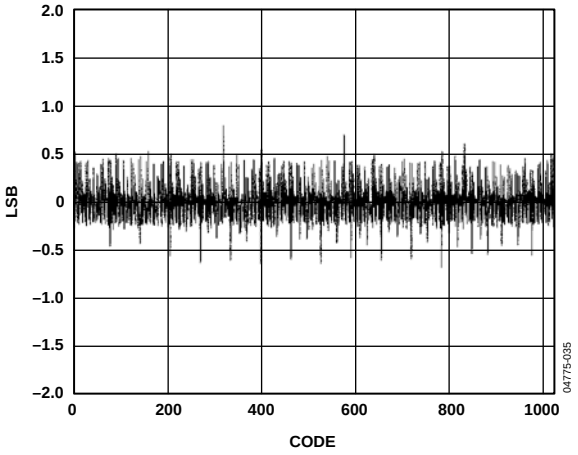

Figure 34. Typical DNL Plot, A_{IN} = 10.3 MHz at −0.5 dBFS, 105 MSPS (−105 Grade)

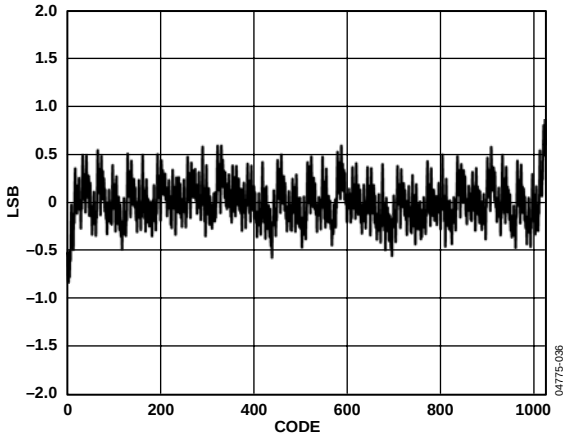

Figure 35. Typical INL Plot, A_{IN} = 10.3 MHz at −0.5 dBFS, 105 MSPS (−105 Grade)

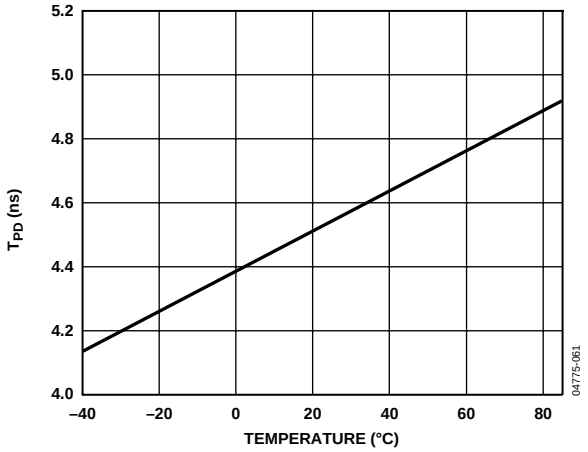

Figure 36. Typical Propagation Delay vs. Temperature (All Speed Grades)

EQUIVALENT CIRCUITS

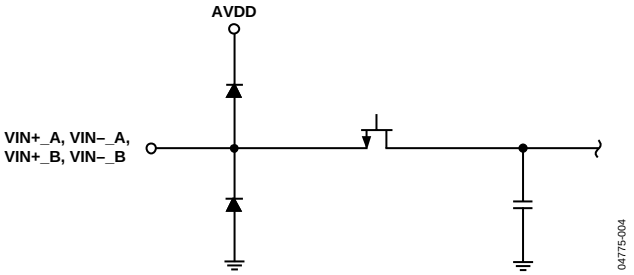

Figure 37. Equivalent Analog Input

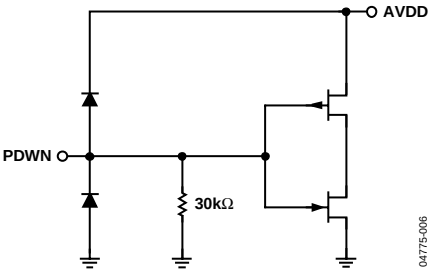

Figure 39. Power-Down Input

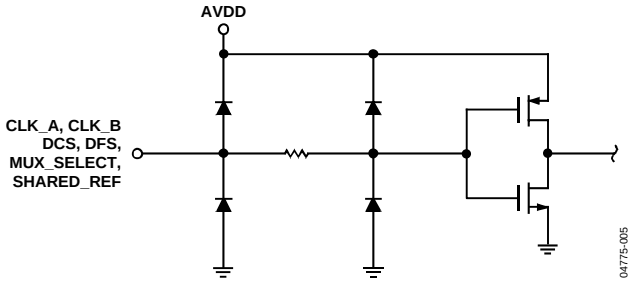

Figure 38. Equivalent Clock, Digital Inputs Circuit

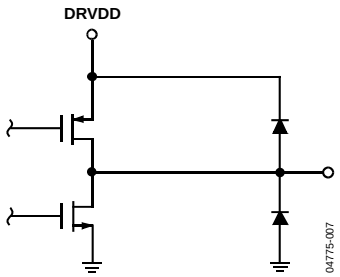

Figure 40. Digital Outputs

THEORY OF OPERATION

The AD9216 consists of two high performance ADCs that are based on the AD9215 converter core. The dual ADC paths are independent, except for a shared internal band gap reference source, VREF. Each of the ADC paths consists of a proprietary front end SHA followed by a pipelined, switched-capacitor ADC. The pipelined ADC is divided into three sections, consisting of a sample-and-hold amplifier, followed by seven 1.5-bit stages, and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined through the digital correction logic block into a final 10-bit result. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the respective clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the flash ADC output to control a switched capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the stage's input signal and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing.

ANALOG INPUT

The analog input to the AD9216 is a differential switched-capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input accepts inputs over a wide common-mode range. An input common-mode voltage of midsupply is recommended to maintain optimal performance.

The SHA input is a differential switched-capacitor circuit. In Figure 41, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents.

This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependant on the application. In IF under-sampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they would limit the input bandwidth. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched, so the common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

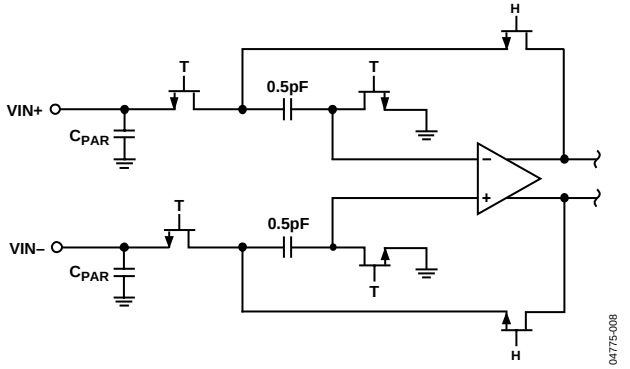

Figure 41. Switched-Capacitor Input

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as:

$$REFT = 1/2\ (AVDD + VREF)$$

$$REFB = 1/2\ (AVDD - VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as

$$VCM_{MIN} = VREF/2$$

$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD9216 to accommodate ground-referenced inputs. Although optimum performance is achieved with a differential input, a single-ended source may be driven into VIN+ or VIN−. In this configuration, one input accepts the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference.

For example, a 2 V p-p signal may be applied to VIN+, while a 1 V reference is applied to VIN−. The AD9216 then accepts an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies.

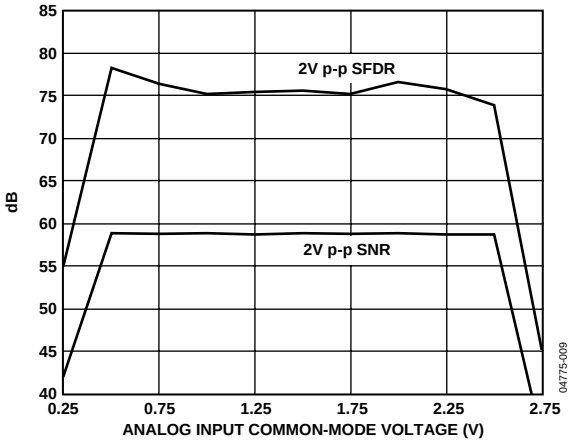

Figure 42. Input Common-Mode Voltage Sensitivity

Differential Input Configurations

As previously detailed, optimum performance is achieved while driving the AD9216 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9216. This is especially true in IF under-sampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 43.

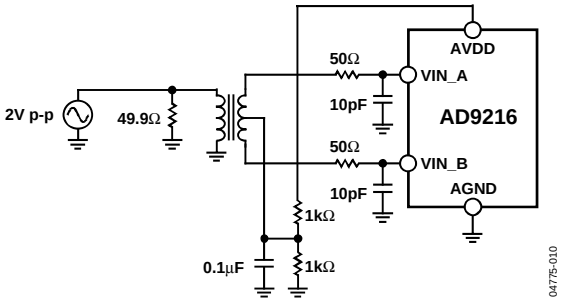

Figure 43. Differential Transformer Coupling

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

For dc-coupled applications, the AD8138, AD8139, or AD8351 can serve as a convenient ADC driver, depending on requirements. Figure 44 shows an example with the AD8138. The AD9216 PCB has an optional AD8139 on board, as shown in Figure 53. Note the AD8351 typically yields better performance for frequencies greater than 30 MHz to 40 MHz.

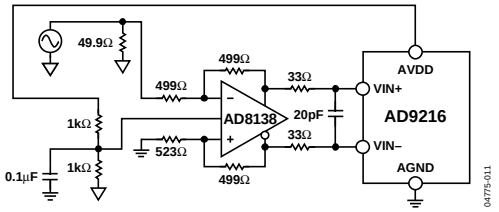

Figure 44. Driving the ADC with the AD8138

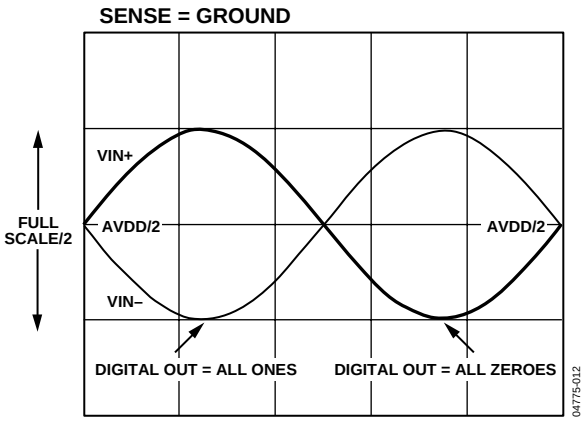

Figure 45. Analog Input Full Scale (Full Scale = 2 V)

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there is a degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance.

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9216 provides separate clock inputs for each channel. The optimum performance is achieved with the clocks operated at the same frequency and phase. Clocking the channels asynchronously may degrade performance significantly. In some applications, it is desirable to skew the clock timing of adjacent channels. The AD9216's separate clock inputs allow for clock timing skew (typically ±1 ns) between the channels without significant performance degradation.

The AD9216 contains two clock duty cycle stabilizers, one for each converter, that retime the nonsampling edge, providing an internal clock with a nominal 50% duty cycle. Faster input clock rates, where it becomes difficult to maintain 50% duty cycles, can benefit from using DCS, as a wide range of input clock duty cycles can be accommodated. Maintaining a 50% duty cycle clock is particularly important in high speed applications, when proper track-and-hold times for the converter are required to maintain high performance. The DCS can be enabled by tying the DCS pin high.

The duty cycle stabilizer uses a delay-locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 2 µs to 3 µs to allow the DLL to acquire and settle to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated by

$$SNR\ degradation = 2 \times \log 10[1/2 \times p \times f_{INPUT} \times t_J]$$

In the equation, the rms aperture jitter, t_J, represents the root-sum square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

For optimal performance, especially in cases where aperture jitter may affect the dynamic range of the AD9216, it is important to minimize input clock jitter. The clock input circuitry should use stable references; for example, use analog power and ground planes to generate the valid high and low digital levels for the AD9216 clock input. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD9216 is proportional to its sampling rates. The digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of bits changing, and C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased, so each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases with clock frequency.

Either channel of the AD9216 can be placed into standby mode independently by asserting the PWDN_A or PDWN_B pins. Time to go into or come out of standby mode is 5 cycles maximum when only one channel is being powered down. When both channels are powered down, VREF goes to ground, resulting in a wake-up time of ~7 ms dependent on decoupling capacitor values.

It is recommended that the input clock(s) and analog input(s) remain static during either independent or total standby, which results in a typical power consumption of 3 mW for the ADC. If the clock inputs remain active while in total standby mode, typical power dissipation of 10 mW results.

The minimum standby power is achieved when both channels are placed into full power-down mode (PDWN_A = PDWN_B = HI). Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time is directly related to the recharging of the REFT and REFB decoupling capacitors and to the duration of the power-down.

A single channel can be powered down for moderate power savings. The powered-down channel shuts down internal circuits, but both the reference buffers and shared reference remain powered on. Because the buffer and voltage reference remain powered on, the wake-up time is reduced to several clock cycles.

DIGITAL OUTPUTS

The AD9216 output drivers can interface directly with 3 V logic families. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches because large drive currents tend to cause current glitches on the supplies that may affect converter performance.

The data format can be selected for either offset binary or twos complement. This is discussed in the Data Format section.

OUTPUT CODING

Table 8.

Code	(VIN+) – (VIN–)	Offset Binary	Twos Complement
1023	> +0.998 V	11 1111 1111	01 1111 1111
1023	+0.998 V	11 1111 1111	01 1111 1111
1022	+0.996 V	11 1111 1110	01 1111 1110
•	•	•	•
•	•	•	•
513	+0.002 V	10 0000 0001	00 0000 0001
512	+0.0 V	10 0000 0000	00 0000 0000
511	−0.002 V	01 1111 1111	11 1111 1111
•	•	•	•
•	•	•	•
1	−0.998 V	00 0000 0001	10 0000 0001
0	−1.000 V	00 0000 0000	10 0000 0000
0	< −1.000 V	00 0000 0000	10 0000 0000

TIMING

The AD9216 provides latched data outputs with a pipeline delay of six clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9216. These transients can detract from the converter's dynamic performance. The lowest conversion rate of the AD9216 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance may degrade.

DATA FORMAT

The AD9216 data output format can be configured for either twos complement or offset binary. This is controlled by the data format select pin (DFS). Connecting DFS to AGND produces offset binary output data. Conversely, connecting DFS to AVDD formats the output data as twos complement.

The output data from the dual ADCs can be multiplexed onto a single, 10-bit output bus. The multiplexing is accomplished by toggling the MUX_SELECT bit, which directs channel data to the same or opposite channel data port. When MUX_SELECT is logic high, the Channel A data is directed to the Channel A output bus, and the Channel B data is directed to the Channel B output bus. When MUX_SELECT is logic low, the channel data is reversed; that is, the Channel A data is directed to the Channel B output bus, and the Channel B data is directed to the Channel A output bus. By toggling the MUX_SELECT bit, multiplexed data is available on either of the output data ports.

If the ADCs are run with synchronized timing, this same clock can be applied to the MUX_SELECT pin. Any skew between CLK_A, CLK_B, and MUX_SELECT can degrade ac performance. It is recommended to keep the clock skew < 100 pHs. After the MUX_SELECT rising edge, either data port has the data for its respective channel; after the falling edge, the alternate channel's data is placed on the bus. Typically, the other unused bus is disabled by setting the appropriate OEB high to reduce power consumption and noise. Figure 46 shows an example of multiplex mode. When multiplexing data, the data rate is two times the sample rate. Note that both channels must remain active in this mode and that each channel's power-down pin must remain low.

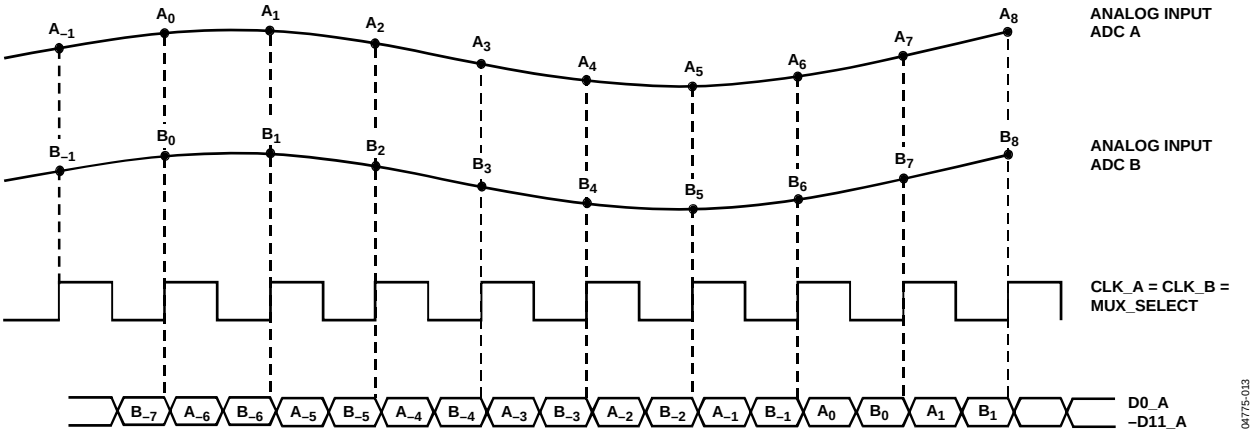

Figure 46. Example of Multiplexed Data Format Using the Channel A Output and the Same Clock Tied to CLK_A, CLK_B, and MUX_SELECT

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9216. The input range can be adjusted by varying the reference voltage applied to the AD9216, using either the internal reference with different external resistor configurations or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

Internal Reference Connection

A comparator within the AD9216 detects the potential at the SENSE pin and configures the reference into three possible states, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 47), setting VREF to 1 V. If a resistor divider is connected, as shown in Figure 48, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times (1 + R2/R1)$$

Note: The optimum performance is obtained with VREF = 1.0 V; performance degrades as VREF (and full scale) reduces (see Figure 25). In all reference configurations, REFT and REFB drive the ADC core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

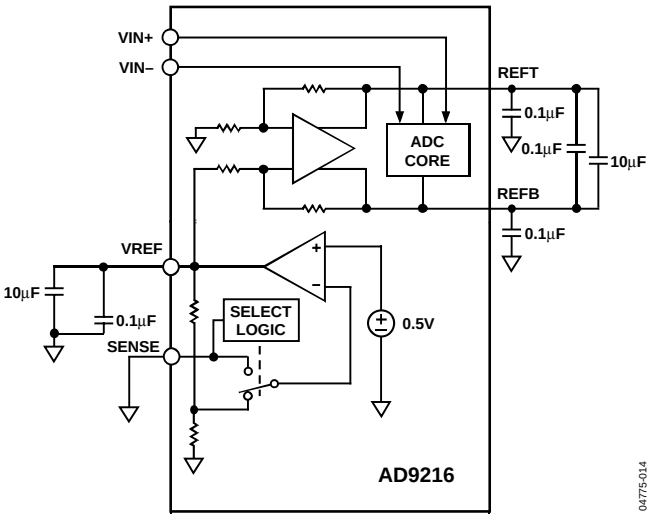

Figure 47. Internal Reference Configuration (One Channel Shown)

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Programmable Reference	0.2 V to VREF	0.5 × (1 + R2/R1)	2 × VREF (see Figure 48)
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve the thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 49 shows the typical drift characteristics of the internal reference.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V. If the internal reference of the AD9216 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 50 depicts how the internal reference voltage is affected by loading.

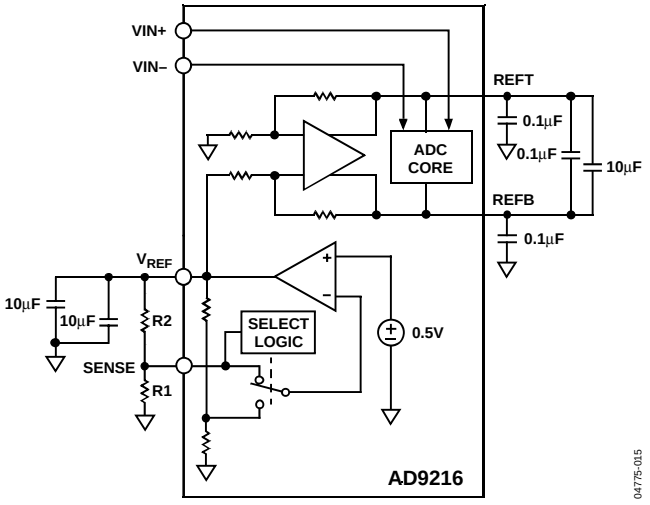

Figure 48. Programmable Reference Configuration (one channel shown)

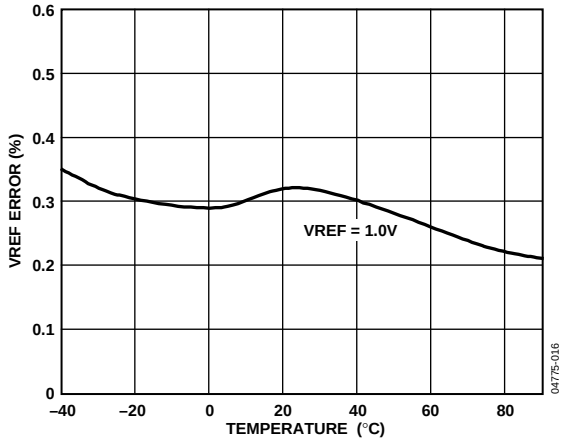

Figure 49. Typical VREF Drift

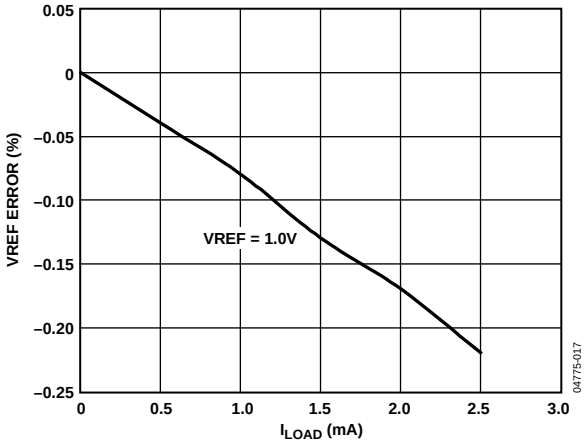

Figure 50. VREF Accuracy vs. Load

Shared Reference Mode

The shared reference mode allows the user to connect the references from the dual ADCs together externally for superior gain and offset matching performance. If the ADCs are to function independently, the reference decoupling can be treated independently and can provide superior isolation between the dual channels. To enable shared reference mode, the SHARED_REF pin must be tied high, and the external differential references must be externally shorted. (REFT_A must be externally shorted to REFT_B, and REFB_A must be shorted to REFB_B.)

DUAL ADC LFCSP PCB

The PCB requires a low jitter clock source, analog sources, and power supplies. The PCB interfaces directly with ADI's standard dual-channel data capture board (HSC-ADC-EVAL-DC), which together with ADI's ADC Analyzer™ software allows for quick ADC evaluation.

POWER CONNECTOR

Power is supplied to the board via three detachable 4-lead power strips.

Table 10. Power Connector

Terminal	Comments
VCC[1] 3.0 V	Analog supply for ADC
VDD[1] 2.5 V	Output supply for ADC
VDL[1] 2.5 V	Buffer supply
VCLK 3.0 V	Supply for XOR Gates
+5 V	Optional op amp supply
−5 V	Optional op amp supply

[1]VCC, VDD, and VDL are the minimum required power connections.

ANALOG INPUTS

The evaluation board accepts a 2 V p-p analog input signal centered at ground at two SMB connectors, Input A and Input B. These signals are terminated at their respective primary side transformer. T1 and T2 are wideband RF transformers that provide the single-ended-to-differential conversion, allowing the ADC to be driven differentially, minimizing even-order harmonics. The analog signals can be low-pass filtered at the secondary transformer to reduce high frequency aliasing.

OPTIONAL OPERATIONAL AMPLIFIER

The PCB has been designed to accommodate an optional AD8139 op amp that can serve as a convenient solution for dc-coupled applications. To use the AD8139 op amp, remove C14, R4, R5, C13, R37, and R36, and place R22, R23, R30, and R24.

CLOCK

The single-clock input is at J5; the input clock is buffered and drives both channel input clocks from Pin 3 at U8 through R79, R40, and R85. Jumper E11 to E19 allows for inverting the input clock. U8 also provides CLKA and CLKB outputs, which are buffered by U6 and U5, which drive the DRA and DRB signals (these are the data-ready clocks going off card). DRA and DRB can also be inverted at their respective jumpers.

Table 11. Jumpers

Terminal	Comments
OEB A	Output Enable for A Side
PWDN A	Power-Down A
MUX	Mux Input
SHARED REF	Shared Reference Input
DRA	Invert DRA
LATA	Invert A Latch Clock
ENC A	Invert Encode A
OEB B	Output Enable for B Side
PWDN B	Power-Down B
DFS	Data Format Select
SHARED REF	Shared Reference Input
DRB	Invert DRB
LATB	Invert B Latch Clock
ENC B	Invert Encode B

VOLTAGE REFERENCE

The ADC SENSE pin is brought out to E41, and the internal reference mode is selected by placing a jumper from E41 to ground (E27). External reference mode is selected by placing a jumper from E41 to E25 and E30 to E2. R56 and R45 allow for programmable reference mode selection.

DATA OUTPUTS

The ADC outputs are buffered on the PCB at U2, U4. The ADC outputs have the recommended series resistors in line to limit switching transient effects on ADC performance.

LFCSP EVALUATION BOARD BILL OF MATERIALS (BOM)

Table 12. Dual CSP PCB Rev. B

No.	Quan.	Reference Designator	Device	Package	Value
1	2	C1, C3	Capacitors	0201	20 pF
2	7	C2, C5, C7, C9, C10, C22, C36	Capacitors	0805	10 µF
3	44	C4, C6, C8, C11 to C15, C20, C21, C24 to C27, C29 to C35, C39 to C66	Capacitors	0402	0.1 µF, (C59, C61 NP[1])
4	7	C16 to C19, C37, C38,C67	Capacitors	TAJD	10 µF
5	2	C23, C28	Capacitors	0201	0.1 µF
6	40	E1 to E7, E9 to E22, E24 to E27, E29 to E31, E33 to E38, E40 to E43, E49, E61	Jumpers		
7	6	J1 to J6	SMA		
8	3	P1, P4, P11	Power Connector Posts	Z5.531.3425.0	Wieland
9	3	P1, P4, P11	Detachable Connectors	25.602.5453.0	Wieland
10	1	P3, P8 (implemented as one 80 pin connector)	Connector	TSW-140-08-L-D-RA	Samtec
11	4	R1, R2, R32, R34	Resistors	0402	36 Ω (All NP[1])
12	6	R3, R7, R11, R14, R51, R61	Resistors	0402	50 Ω, (R11, R51 NP[1])
13	4	R6, R8, R33, R42	Resistors	0402	100 Ω, (All NP[1])
14	4	R4, R5, R36, R37	Resistors	0402	33 Ω
15	10	R9, R12, R20, R35, R40, R43, R50, R53, R84, R85	Resistors	0402	Zero Ω (R9, R12, R35, R43, R50, R84 NP[1])
16	6	R15, R16, R18, R26, R29, R31	Resistors	0402	499 Ω (R16, R29 NP[1])
17	2	R17, R25	Resistors	0402	525 Ω
18	34	R19, R21, R27, R28, R39, R41, R44, R46 to R49, R52, R54, R55, R57 to R60, R62 to R73, R75, R77, R78, R81 to R83	Resistors	0402	1 kΩ (R64, R78, R81, R82, R83 NP[1])
19	4	R22 to R24, R30	Resistors	0402	40 Ω (R22, R23, R24, R30 NP[1])
20	2	R45, R56	Resistors	0402	10 kΩ (R45, R56 NP[1])
21	7	R10, R13, R38, R74, R76, R79, R80	Resistor	0402	22 Ω
22	8	RZ1, RZ2, RZ3, RZ4, RZ5, RZ6, RZ9, RZ10	Resistor Pack	CTS 742C163470J	47 Ω
24	2	T1, T2	Transformers	T1-1WT	Minicircuits
25	1	U1	AD9216/AD9238/AD9248	LFCSP-64	
26	2	U2, U4	Transparent Latch/Buffer	TSSOP-48	SN74LVCH16373ADGGR
27	2	U3, U7	Inverter	SC-70	SN74LVC1G04DCKT (U3, U7 NP[1])
28	3	U5, U6, U8	XOR	SO-14	SN74VCX86
29	2	U11, U12	Amp	SO-8/EP	AD8139
30	14	P2, P5 to P7, P9, P10, P12 to P18, P21	Solder Bridge		

[1] Not Populated.

LFCSP PCB SCHEMATICS

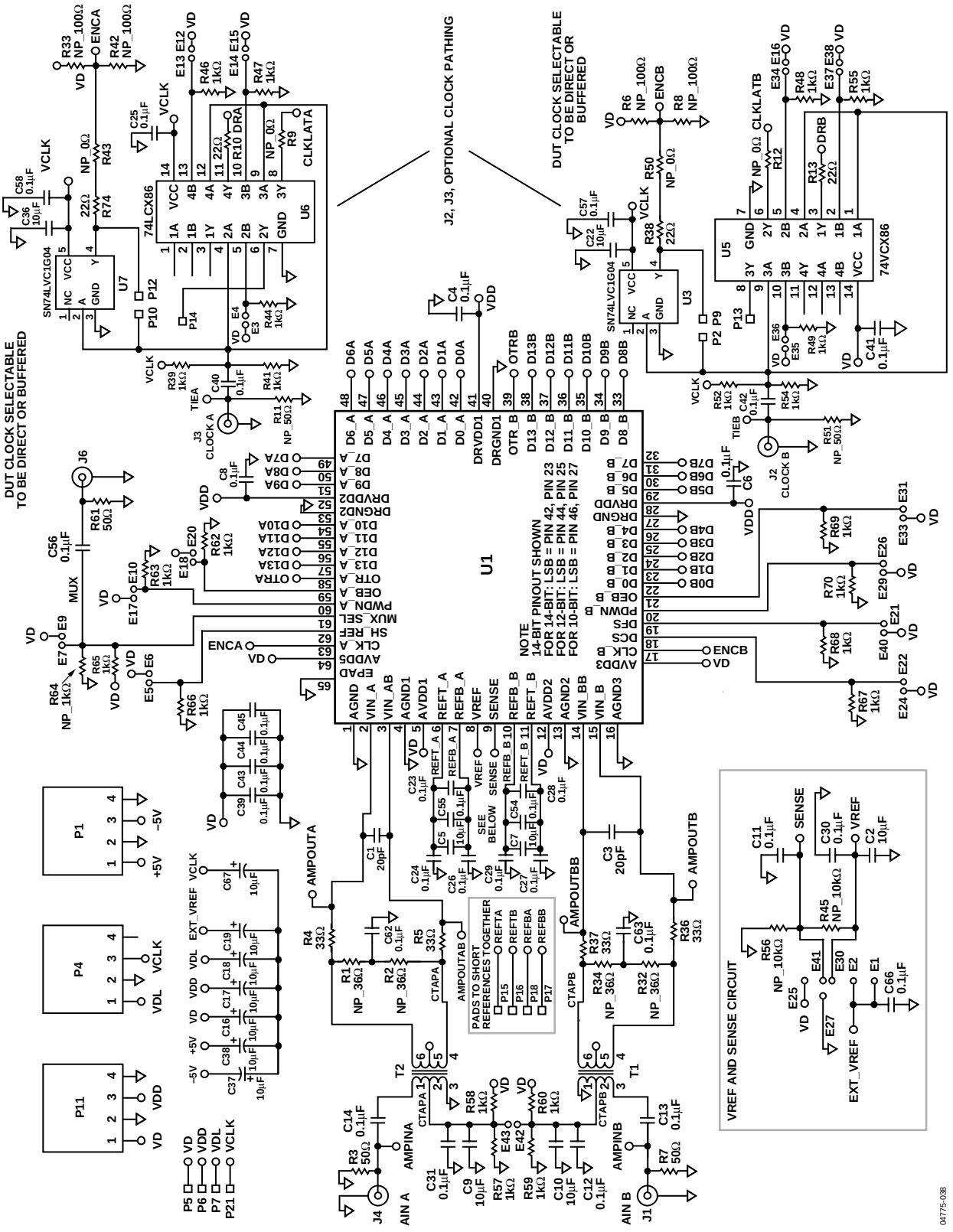

Figure 51. PCB Schematic (1 of 3)

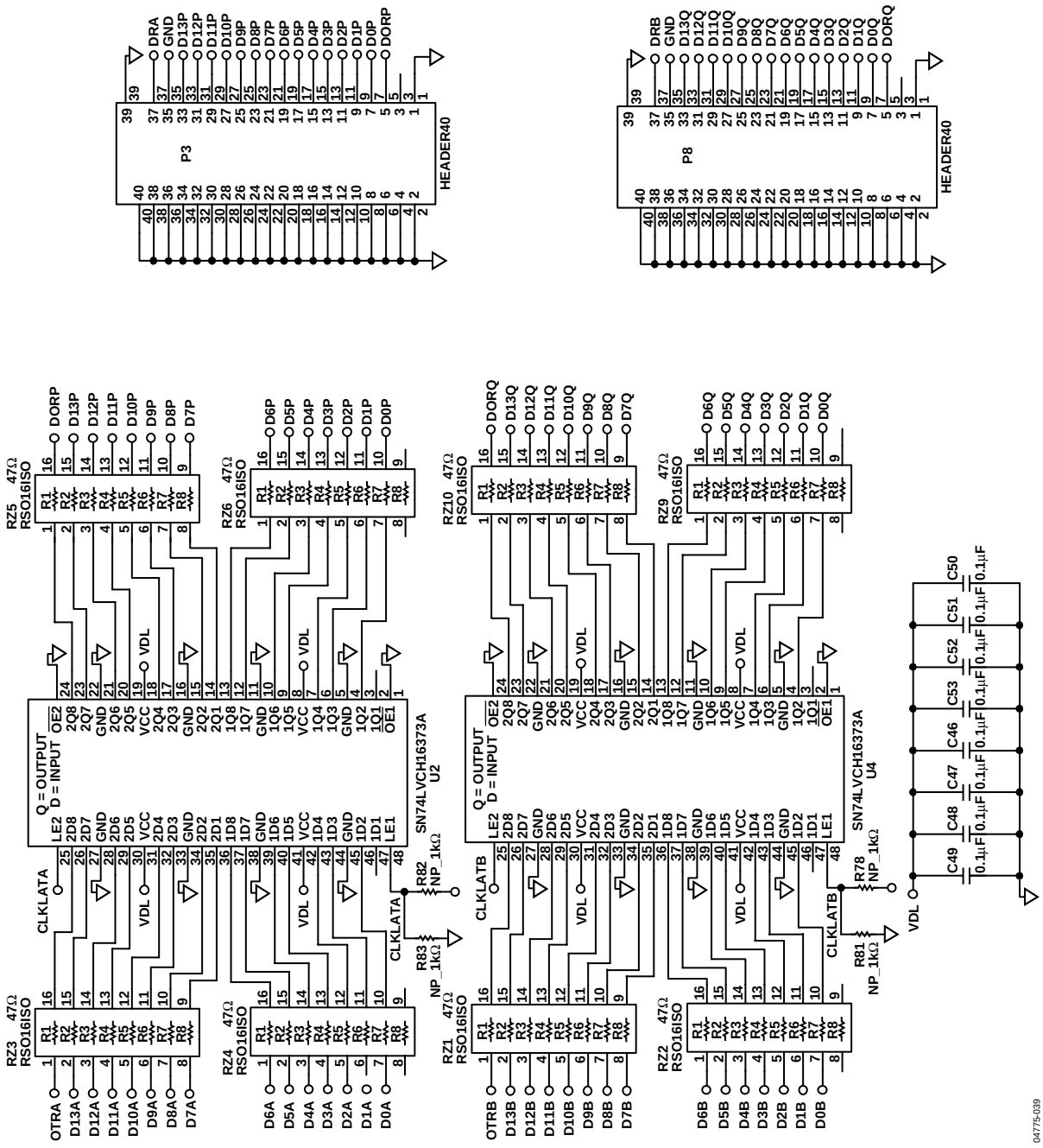

Figure 52. PCB Schematic (2 of 3)

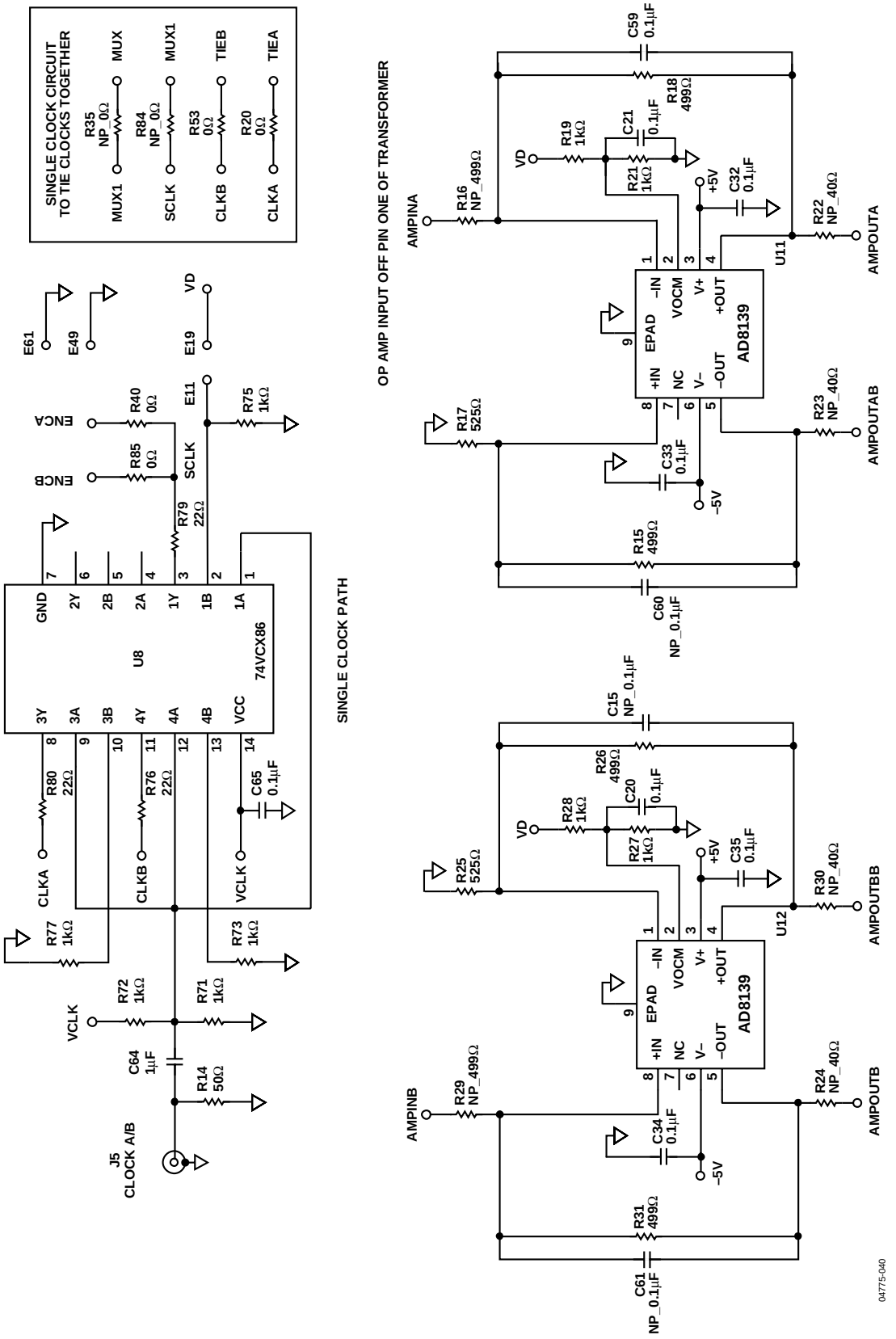

Figure 53. PCB Schematic (3 of 3)

LFCSP PCB LAYERS

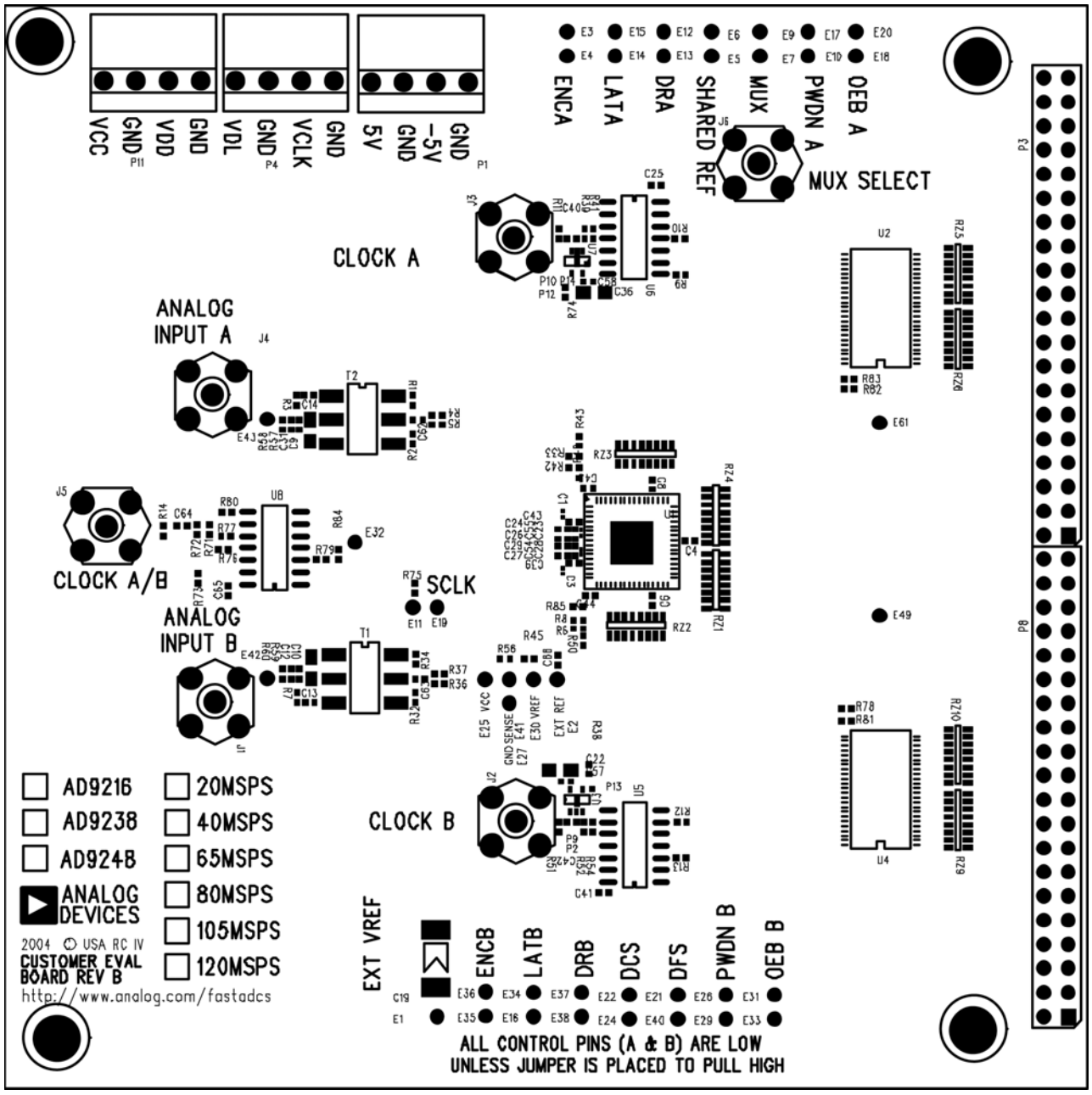

Figure 54. PCB Top-Side Silkscreen

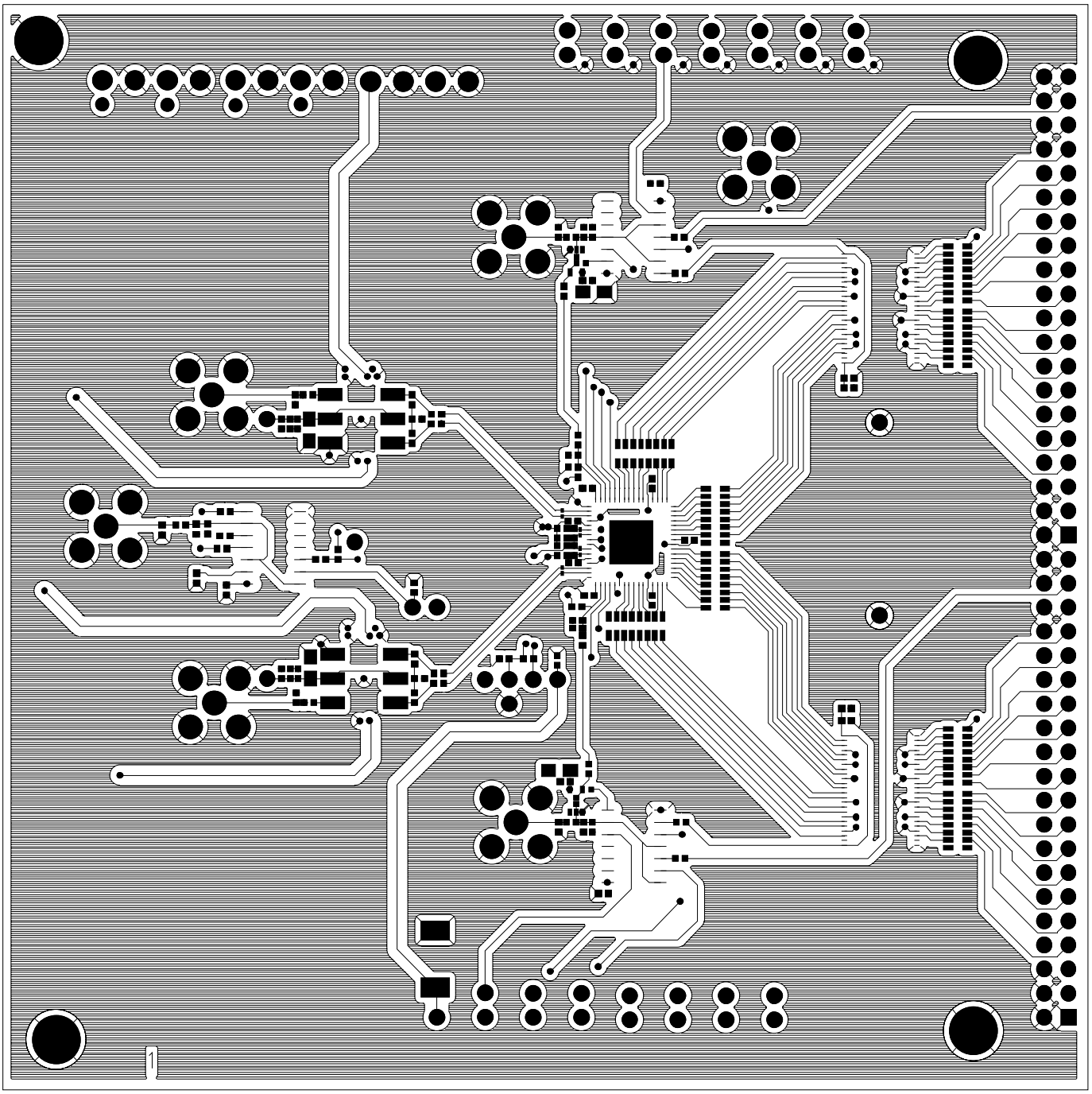

Figure 55. PCB Top-Side Copper Routing

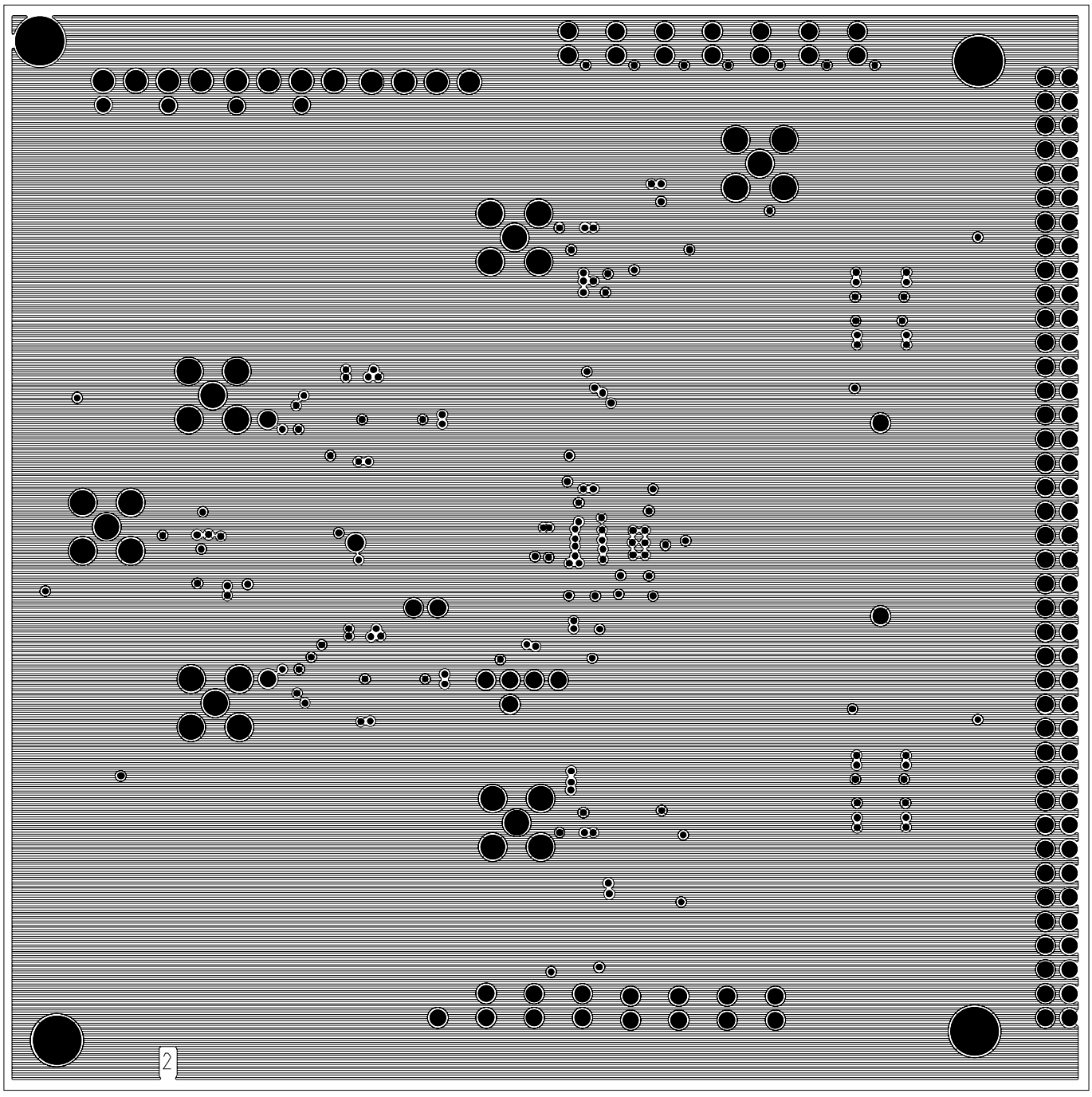

Figure 56. PCB Ground Layer

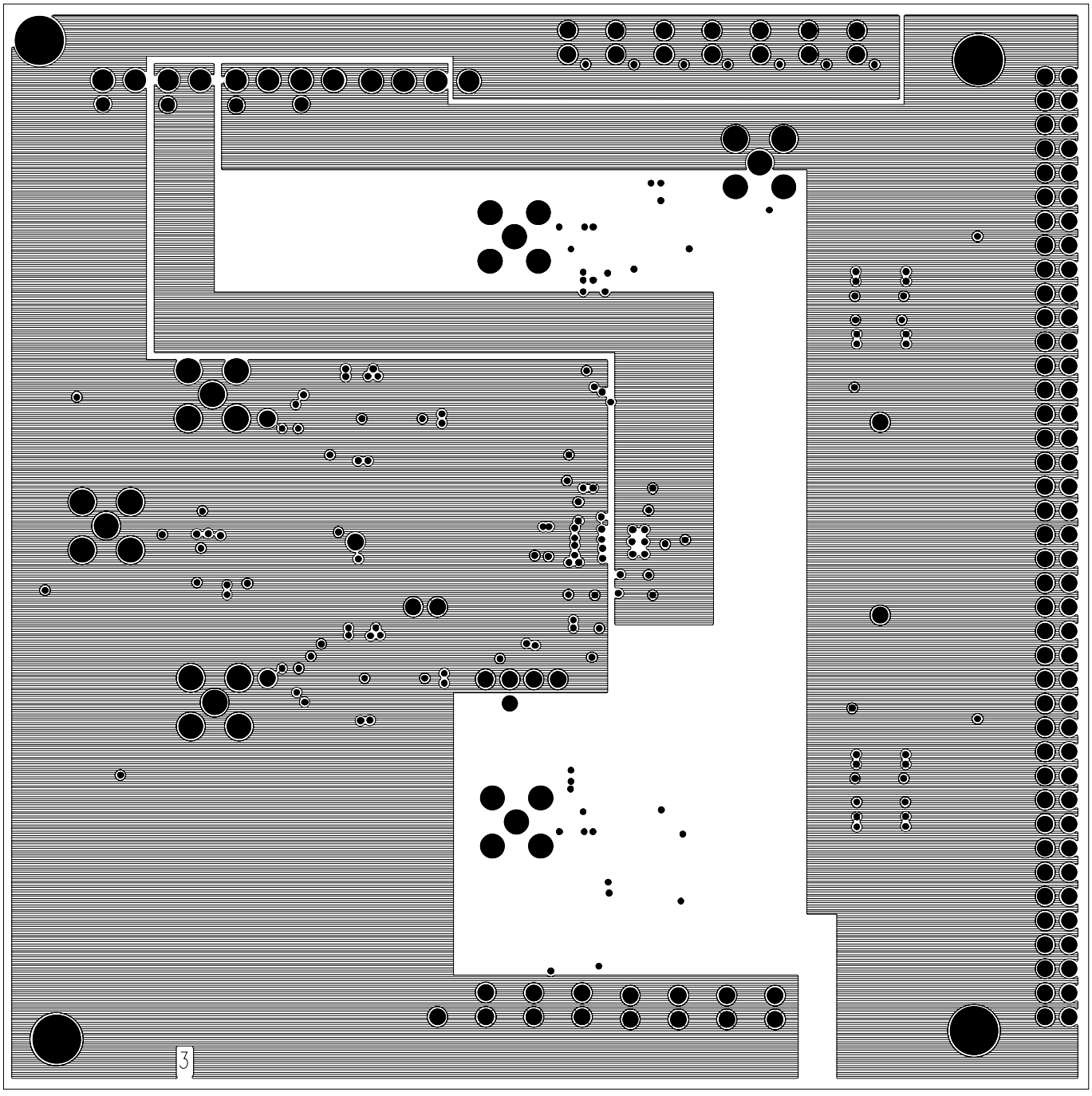

Figure 57. PCB Split Power Plane

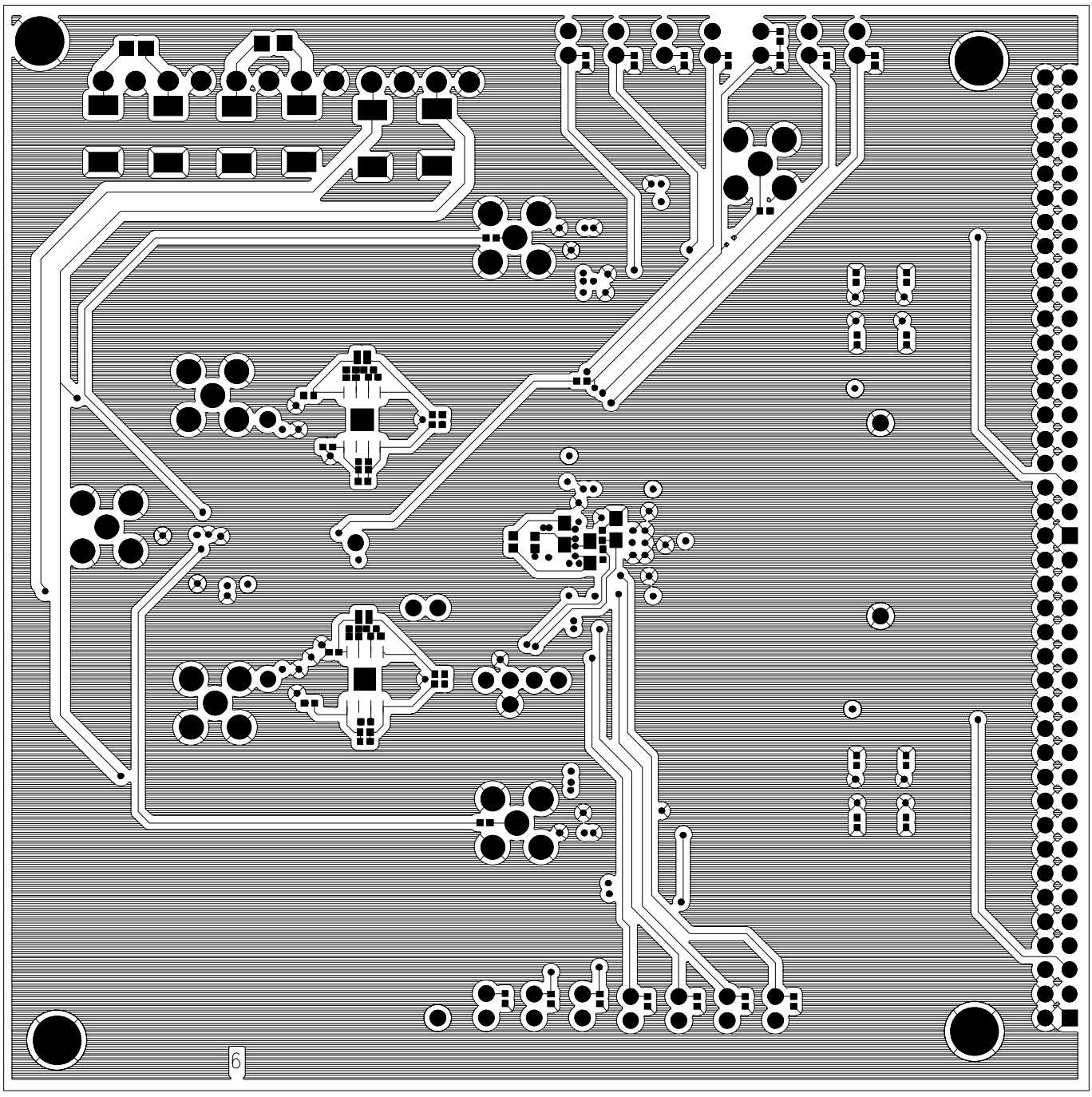

Figure 58. PCB Bottom-Side Copper Routing

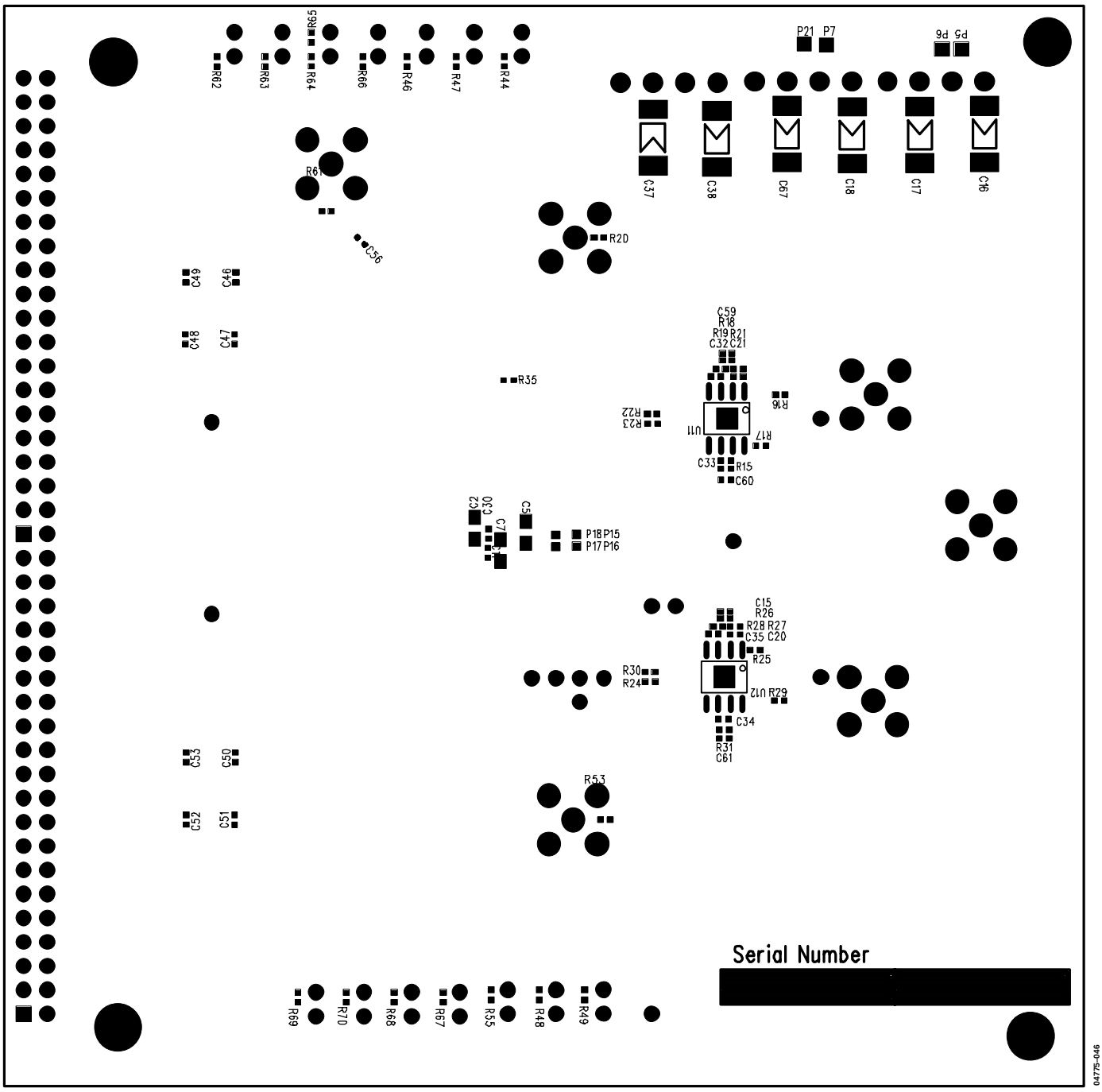

Figure 59. PCB Bottom-Side Silkscreen

THERMAL CONSIDERATIONS

The AD9216 LFCSP package has an integrated heat slug that improves the thermal and electrical properties of the package when locally attached to a ground plane at the PCB. A thermal (filled) via array to a ground plane beneath the part provides a path for heat to escape the package, lowering junction temperature. Improved electrical performance also results from the reduction in package parasitics due to proximity of the ground plane. Recommended array is 0.3 mm vias on 1.2 mm pitch. θ_{JA} = 26.4°C/W with this recommended configuration. Soldering the slug to the PCB is a requirement for this package.

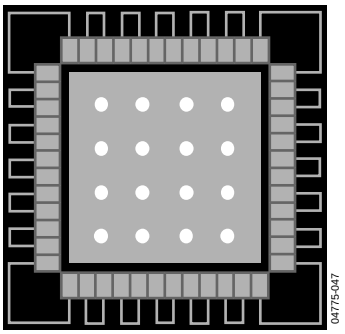

Figure 60. Thermal Via Array

OUTLINE DIMENSIONS

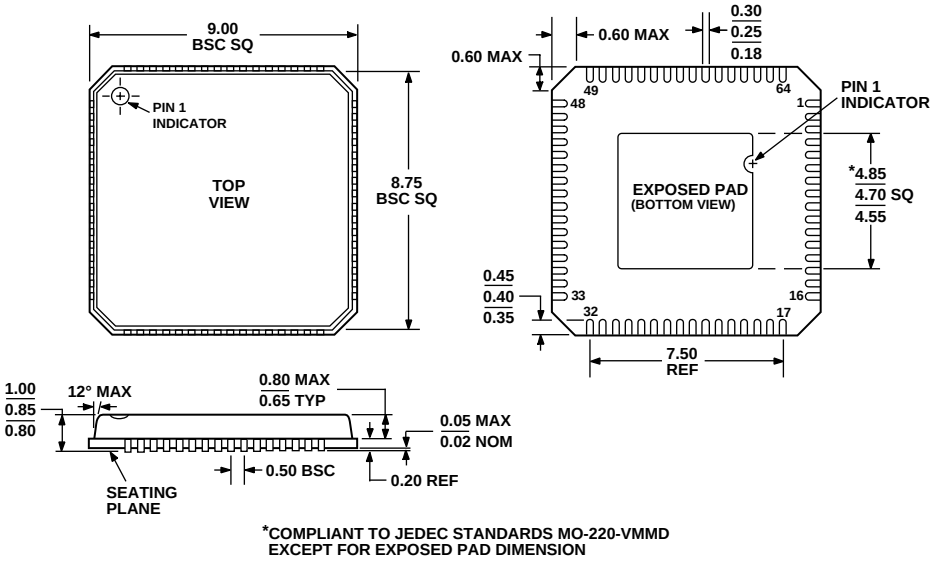

Figure 61. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 × 9 mm Body, Very Thin Quad (CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9216BCPZ-65[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-64-1
AD9216BCPZRL7-65[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-64-1
AD9216BCPZ-80[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-64-1
AD9216BCPZRL7-80[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-64-1
AD9216BCPZ-105[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-64-1
AD9216BCPZRL7-105[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP-VQ)	CP-64-1
AD9216-80PCB[2]		Evaluation Board with AD9216BCPZ-80	
AD9216-105PCB		Evaluation Board with AD9216BCPZ-105	

[1] Z = Pb-free part.
[2] Supports AD9216-65 and AD9216-80 Evaluation.

NOTES

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D04775–0–6/05(A)

Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:

AD9216BCPZRL7-65 AD9216BCPZ-105 AD9216BCPZRL7-80 AD9216BCPZ-80 AD9216BCPZ-65