2 A, Ultralow Noise, High PSRR, RF Linear Regulator

Data Sheet

ADP7159

FEATURES

- Input voltage range: 2.3 V to 5.5 V
- Adjustable output voltage range (V_{OUT}): 1.2 V to 3.3 V
- Maximum load current: 2 A
- Low noise
  - 0.9 µV rms total integrated noise from 100 Hz to 100 kHz
  - 1.6 µV rms total integrated noise from 10 Hz to 100 kHz
- Noise spectral density: 1.7 nV/√Hz from 10 kHz to 1 MHz
- Power supply rejection ratio (PSRR)
  - 68 dB from 1 kHz to 100 kHz
  - 45 dB at 1 MHz
- Dropout voltage: 200 mV typical at I_{OUT} = 2 A, V_{OUT} = 3.3 V
- Initial accuracy: ±0.6% at I_{LOAD} = 10 mA
- Accuracy over line, load, and temperature: ±1.5%
- Quiescent current (I_{GND})
  - 4.0 mA typical at 0 µA
  - 9.0 mA typical at 2 A
- Low shutdown current: 0.2 µA typical
- Stable with a 10 µF ceramic output capacitor
- 10-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages
- Precision enable
- Supported by ADIsimPower tool

APPLICATIONS

- Regulation to noise sensitive applications: phase-locked loops (PLLs), voltage controlled oscillators (VCOs), and PLLs with integrated VCOs
- Communications and infrastructure
- Backhaul and microwave links

GENERAL DESCRIPTION

The ADP7159 is an adjustable linear regulator that operates from 2.3 V to 5.5 V and provides up to 2 A of output current. Output voltages from 1.2 V to 3.3 V are possible depending on the model. Using an advanced proprietary architecture, the device provides high power supply rejection and ultralow noise, achieving excellent line and load transient response with only a 10 µF ceramic output capacitor.

The ADP7159 is available in four models that optimize power dissipation and PSRR performance as a function of the input and output voltage. See Table 9 and Table 10 for selection guides.

The typical output noise of the ADP7159 regulator is 0.9 µV rms from 100 Hz to 100 kHz and 1.7 nV/√Hz for noise spectral density from 10 kHz to 1 MHz. The ADP7159 is available in 10-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages, making it not only a very compact solution, but also providing excellent thermal performance for applications requiring up to 2 A of output current in a small, low profile footprint.

TYPICAL APPLICATION CIRCUIT

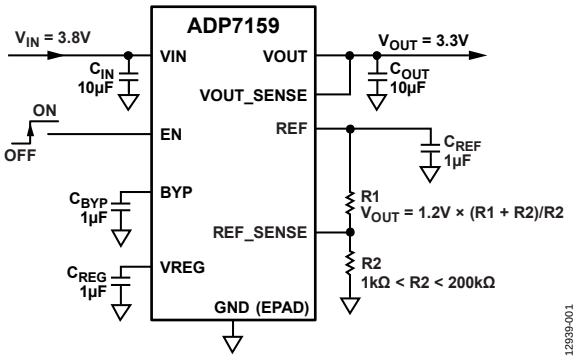

Figure 1. Regulated 3.3 V Output from 3.8 V Input

Table 1. Related Devices

Model	Input Voltage	Output Current	Fixed/ Adjustable	Package
ADP7158	2.3 V to 5.5 V	2 A	Fixed	10-Lead LFCSP/ 8-Lead SOIC
ADP7156, ADP7157	2.3 V to 5.5 V	1.2 A	Fixed/ Adjustable	10-Lead LFCSP/ 8-Lead SOIC
ADM7150, ADM7151	4.5 V to 16 V	800 mA	Fixed/ Adjustable	8-Lead LFCSP/ 8-Lead SOIC
ADM7154, ADM7155	2.3 V to 5.5 V	600 mA	Fixed/ Adjustable	8-Lead LFCSP/ 8-Lead SOIC
ADM7160	2.2 V to 5.5 V	200 mA	Fixed	6-Lead LFCSP/ 5-Lead TSOT

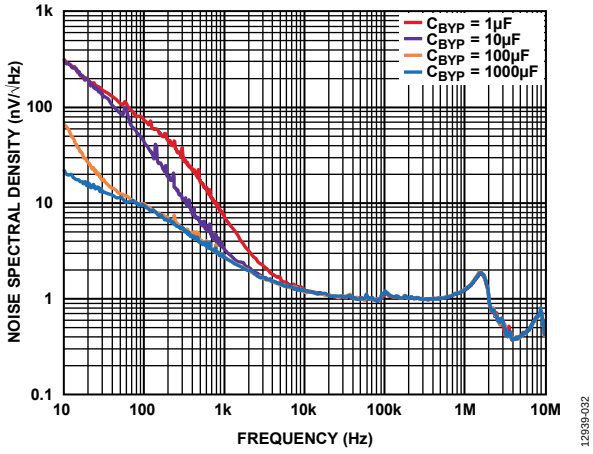

Figure 2. Noise Spectral Density at Different Values of C_{BYP}, V_{OUT} = 3.3 V

Rev. A
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

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REVISION HISTORY

5/2016—Rev. 0 to Rev. A

Added Note 2 to Table 2; Renumbered Sequentially ... 4
Change to Figure 4 ... 6
Change to Programmable Precision Enable Section ... 16

3/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{OUT_MAX}[1] + 0.5 V; V_{EN} = V_{IN}; I_{LOAD} = 10 mA; C_{IN} = C_{OUT} = 10 µF; C_{REG} = C_{REF} = C_{BYP} = 1 µF; T_A = 25°C for typical specifications; T_A = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.3		5.5	V
LOAD CURRENT	I_{LOAD}				2	A
OPERATING SUPPLY CURRENT	I_{GND}	I_{LOAD} = 0 µA		4.0	8.0	mA
		I_{LOAD} = 2 A		9.0	14.0	mA
SHUTDOWN CURRENT	I_{IN-SD}	EN = ground		0.2	4	µA
NOISE[2]		V_{OUT} = 1.2 V to 3.3 V				
Output Noise	OUT_{NOISE}	10 Hz to 100 kHz		1.6		µV rms
		100 Hz to 100 kHz		0.9		µV rms
Noise Spectral Density	OUT_{NSD}	10 kHz to 1 MHz		1.7		nV/√Hz
POWER SUPPLY REJECTION RATIO[2]	PSRR	I_{LOAD} = 2 A				
ADP7159-01		1 kHz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V		55		dB
		1 MHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V		40		dB
ADP7159-02		1 kHz to 100 kHz, V_{IN} = 2.8 V, V_{OUT} = 2.3 V		61		dB
		1 MHz, V_{IN} = 2.8 V, V_{OUT} = 2.3 V		45		dB
ADP7159-03		1 kHz to 100 kHz, V_{IN} = 3.4 V, V_{OUT} = 2.9 V		65		dB
		1 MHz, V_{IN} = 3.4 V, V_{OUT} = 2.9 V		45		dB
ADP7159-04		1 kHz to 100 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V		68		dB
		1 MHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V		45		dB
OUTPUT VOLTAGE ACCURACY						
Output Voltage[3]	V_{OUT}		1.2		3.3	V
Initial Accuracy		I_{LOAD} = 10 mA, T_A = 25°C	−0.6		+0.6	%
		10 mA < I_{LOAD} < 2 A, T_A = 25°C	−1.0		+1.0	%
		10 mA < I_{LOAD} < 2 A, T_A = −40°C to +125°C	−1.5		+1.5	%
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT_MAX} + 0.5 V to 5.5 V	−0.1		+0.1	%/V
Load[4]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 2 A			0.3	%/A
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}					
REF				22		mA
VOUT			2.4	3	3.8	A
DROPOUT VOLTAGE[6]	$V_{DROPOUT}$	I_{OUT} = 1.2 A, V_{OUT} = 3.3 V		120	170	mV
		I_{OUT} = 2 A, V_{OUT} = 3.3 V		200	280	mV
PULL-DOWN RESISTANCE		EN = 0 V, V_{IN} = 5.5 V				
VOUT	$V_{OUT-PULL}$	V_{OUT} = 1 V		650		Ω
VREG	$V_{REG-PULL}$	V_{REG} = 1 V		31		kΩ
REF	$V_{REF-PULL}$	V_{REF} = 1 V		850		Ω
BYP	$V_{BYP-PULL}$	V_{BYP} = 1 V		650		Ω
START-UP TIME[2, 7]		V_{OUT} = 3.3 V				
VOUT	$t_{START-UP}$			1.2		ms
VREG	$t_{REG-START-UP}$			0.6		ms
REF	$t_{REF-START-UP}$			0.5		ms
THERMAL SHUTDOWN[2]						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			15		°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UNDERVOLTAGE THRESHOLDS						
Input Voltage						
Rising	$UVLO_{RISE}$			2.22	2.29	V
Falling	$UVLO_{FALL}$		1.95	2.02		V
Hysteresis	$UVLO_{HYS}$			200		mV
V_{REG} THRESHOLDS[8]						
Rising	$VREGUVLO_{RISE}$				1.94	V
Falling	$VREGUVLO_{FALL}$		1.60			V
Hysteresis	$VREGUVLO_{HYS}$			185		mV
EN INPUT PRECISION		2.3 V ≤ V_{IN} ≤ 5.5 V				
EN Input						
Logic High	V_{EN_HIGH}		1.13	1.22	1.31	V
Logic Low	V_{EN_LOW}		1.05	1.13	1.22	V
Logic Hysteresis	V_{EN_HYS}			90		mV
LEAKAGE CURRENT						
REF_SENSE	$I_{REF\_SENSE\_LKG}$			10		nA
EN	I_{EN_LKG}	EN = V_{IN} or ground		0.01	1	µA

[1] V_{OUT_MAX} is the maximum output voltage of each version of the ADP7159.
[2] Guaranteed by characterization, but not production tested.
[3] This output voltage specification is for ADP7159-04 version. Table 10 provides a guide for selecting one of the four versions of the ADP7159 based on voltage range.
[4] This specification is based on an endpoint calculation using 10 mA and 2 A loads.
[5] Current-limit threshold is the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is the current that causes the output voltage to drop to 90% of 3.0 V or 2.7 V.
[6] Dropout voltage is the input to output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages above 2.3 V.
[7] Start-up time is the time from the rising edge of V_{EN} to V_{OUT}, V_{REG}, or V_{REF} being at 90% of its nominal value.
[8] The output voltage is disabled until the V_{REG} UVLO rise threshold is crossed. The V_{REG} output is disabled until the input voltage UVLO rising threshold is crossed.

Table 3. Input and Output Capacitors, Recommended Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM CAPACITANCE		T_A = −40°C to +125°C				
Input[1]	C_{IN}		10.0			µF
Regulator[1]	C_{REG}		1.0			µF
Output[1]	C_{OUT}		10.0			µF
Bypass	C_{BYP}		1.0			µF
Reference	C_{REF}		1.0			µF
CAPACITOR EFFECTIVE SERIES RESISTANCE (ESR)	R_{ESR}	T_A = −40°C to +125°C				
C_{REG}, C_{OUT}, C_{IN}, C_{REF}			0.001		0.2	Ω
C_{BYP}			0.001		2.0	Ω

[1] The minimum input, regulator, and output capacitances must be greater than 7.0 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN to Ground	−0.3 V to +7 V
VREG to Ground	−0.3 V to VIN or +4 V (whichever is less)
VOUT to Ground	−0.3 V to VREG or +4 V (whichever is less)
VOUT_SENSE to Ground	−0.3 V to VREG or +4 V (whichever is less)
VOUT to VOUT_SENSE	±0.3 V
BYP to VOUT	±0.3 V
EN to Ground	−0.3 V to +7 V
BYP to Ground	−0.3 V to VREG or +4 V (whichever is less)
REF to Ground	−0.3 V to VREG or +4 V (whichever is less)
REF_SENSE to Ground	−0.3 V to +4 V
Storage Temperature Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7159 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}).

The maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The θ_{JA} value may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See the JESD51-7 standard and the JESD51-9 standard for detailed information on the board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
10-Lead LFCSP	53.8	15.6	29.1	°C/W
8-Lead SOIC	50.4	42.3	30.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

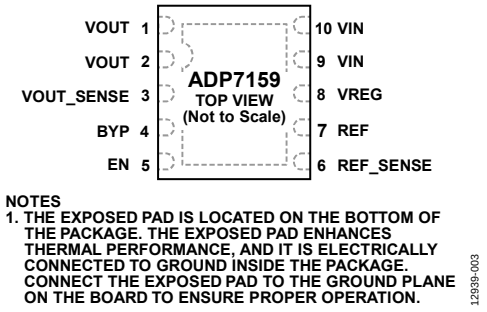

Figure 3. 10-Lead LFCSP Pin Configuration

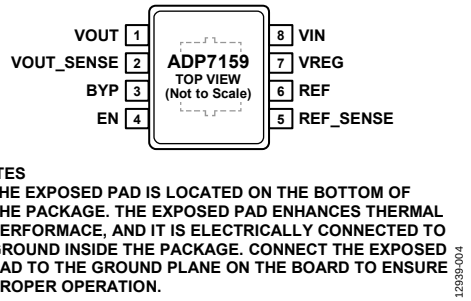

Figure 4. 8-Lead SOIC Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
LFCSP	**SOIC**	**Mnemonic**	**Description**
1, 2	1	VOUT	Regulated Output Voltage. Bypass VOUT to ground with a 10 µF or greater capacitor.
3	2	VOUT_SENSE	Output Sense. VOUT_SENSE is internally connected to VOUT with a 10 Ω resistor. Connect VOUT_SENSE as close to the load as possible.
4	3	BYP	Low Noise Bypass Capacitor. Connect a 1 µF or greater capacitor from the BYP pin to ground to reduce noise. Do not connect a load to this pin.
5	4	EN	Enable. Drive EN high to turn on the regulator, and drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
6	5	REF_SENSE	Reference Sense. This pin sets the output voltage with an external resistor divider. $V_{OUT} = V_{REF} \times (R1 + R2)/R2$, where $V_{REF} = 1.2$ V. Connect REF_SENSE to the REF pin. Do not connect REF_SENSE to VOUT or ground.
7	6	REF	Low Noise Reference Voltage Output. Bypass REF to ground with a 1 µF or greater capacitor. Short REF_SENSE to REF for fixed output voltages. Do not connect a load to this pin.
8	7	VREG	Regulated Input Supply Voltage to the LDO Amplifier. Bypass VREG to ground with a 1 µF or greater capacitor.
9, 10	8	VIN	Regulator Input Supply Voltage. Bypass VIN to ground with a 10 µF or greater capacitor.
		EP	Exposed Pad. The exposed pad is located on the bottom of the package. The exposed pad enhances thermal performance, and it is electrically connected to ground inside the package. Connect the exposed pad to the ground plane on the board to ensure proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{OUT} + 0.5 V, or V_{IN} = 2.3 V, whichever is greater; V_{EN} = V_{IN}; I_{LOAD} = 10 mA; C_{IN} = C_{OUT} = 10 µF; C_{REG} = C_{REF} = C_{BYP} = 1 µF; T_A = 25°C, unless otherwise noted.

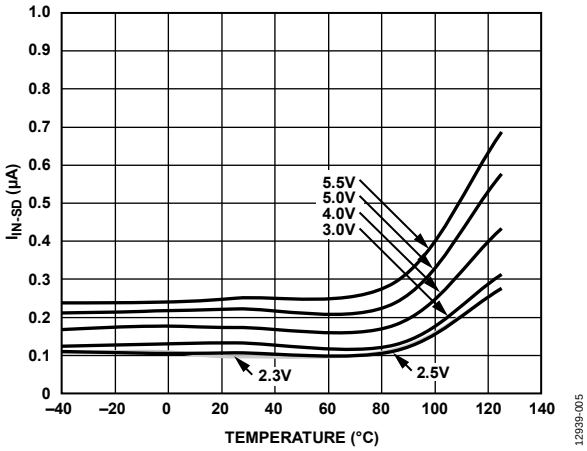

Figure 5. Shutdown Current (I_{IN-SD}) vs. Temperature at Various Input Voltages (V_{IN}), V_{OUT} = 1.8V

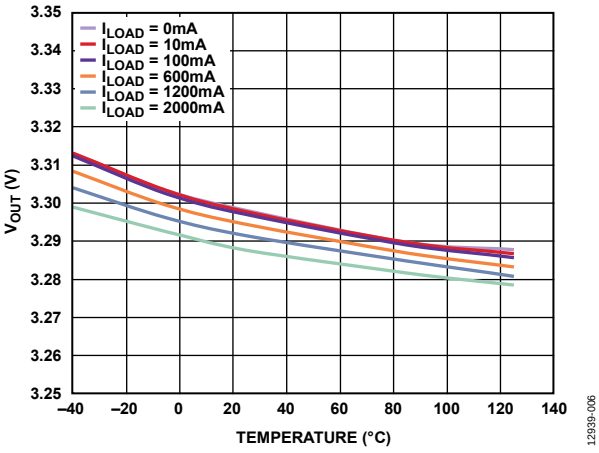

Figure 6. Output Voltage (V_{OUT}) vs. Temperature at Various Loads, V_{OUT} = 3.3 V

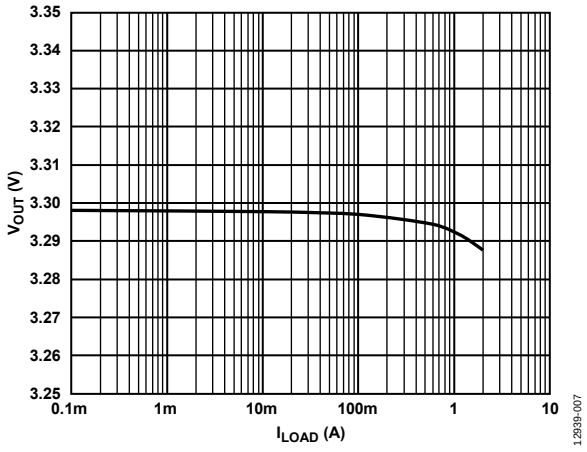

Figure 7. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

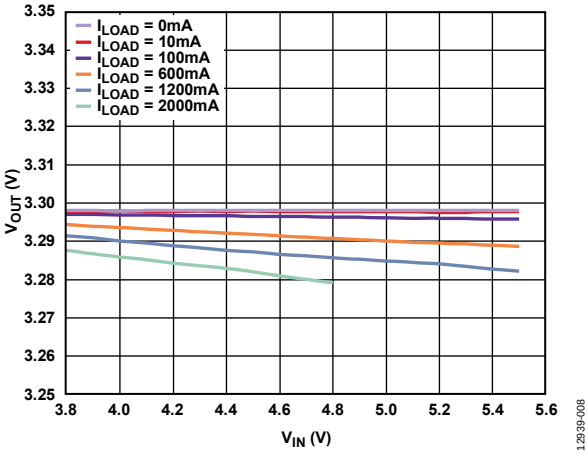

Figure 8. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 3.3 V

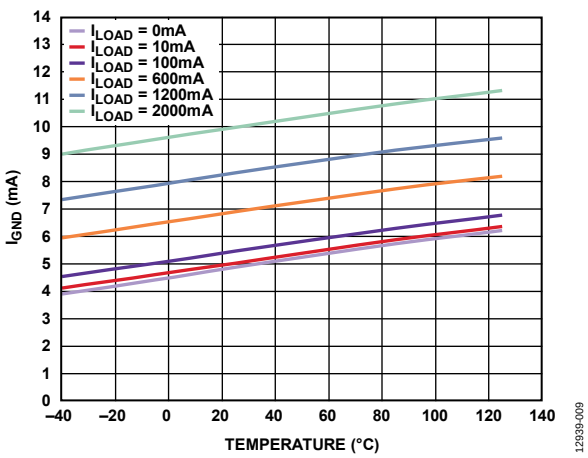

Figure 9. Ground Current (I_{GND}) vs. Temperature at Various Loads, V_{OUT} = 3.3 V

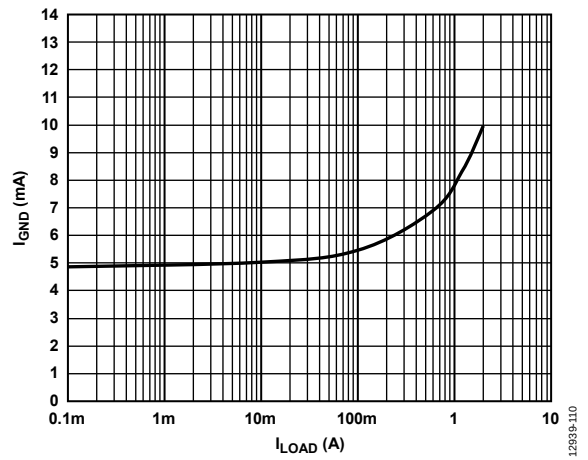

Figure 10. Ground Current (I_{GND}) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

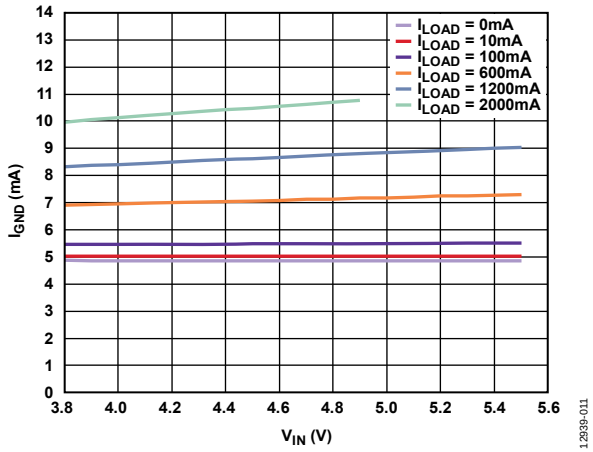

Figure 11. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 3.3 V

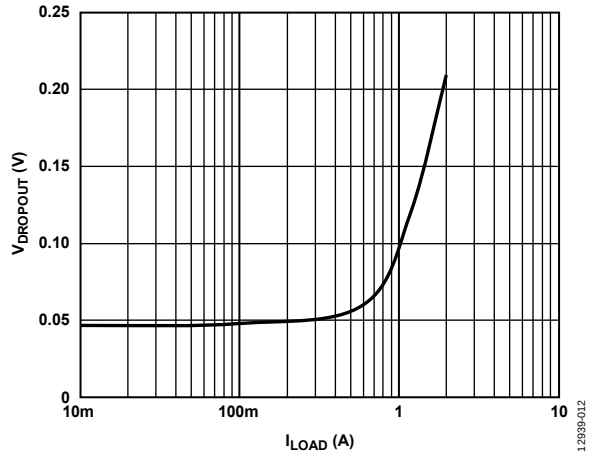

Figure 12. Dropout Voltage ($V_{DROPOUT}$) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

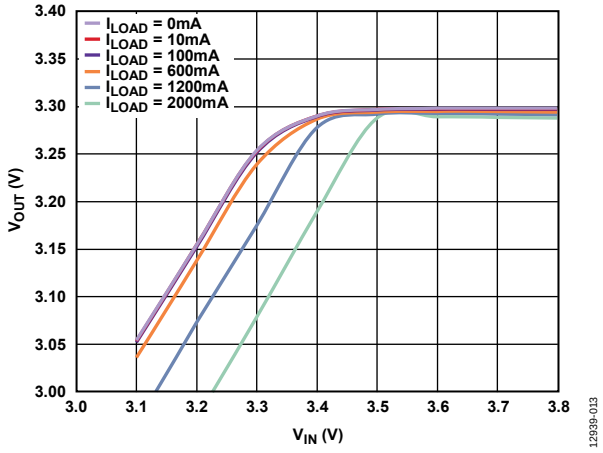

Figure 13. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3.3 V

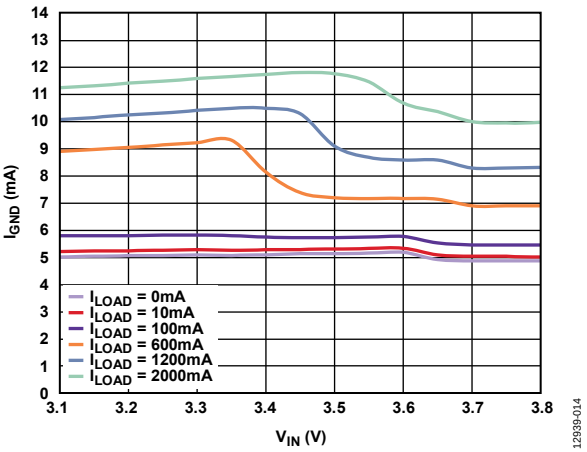

Figure 14. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3.3 V

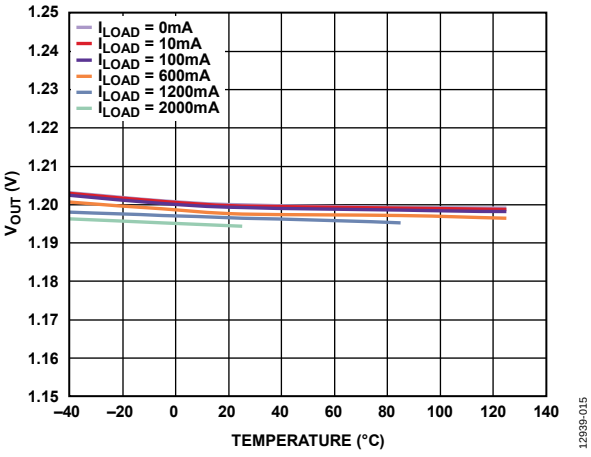

Figure 15. Output Voltage (V_{OUT}) vs. Temperature at Various Loads, V_{OUT} = 1.2 V

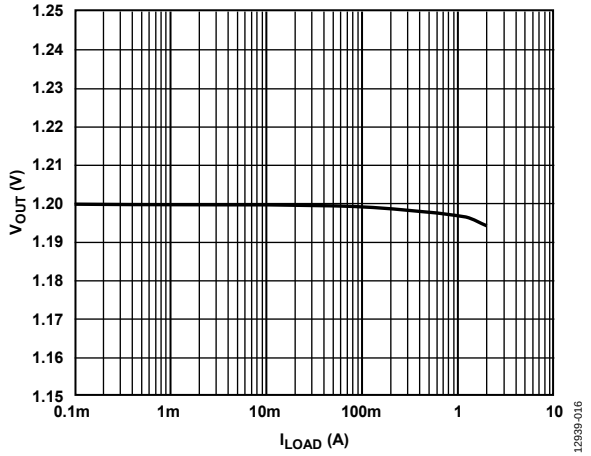

Figure 16. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 1.2 V

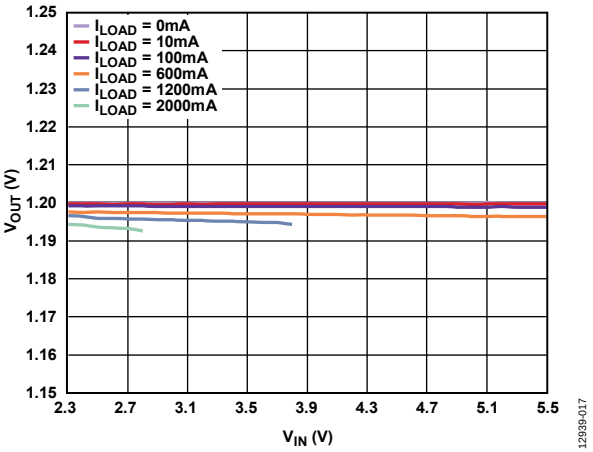

Figure 17. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 1.2 V

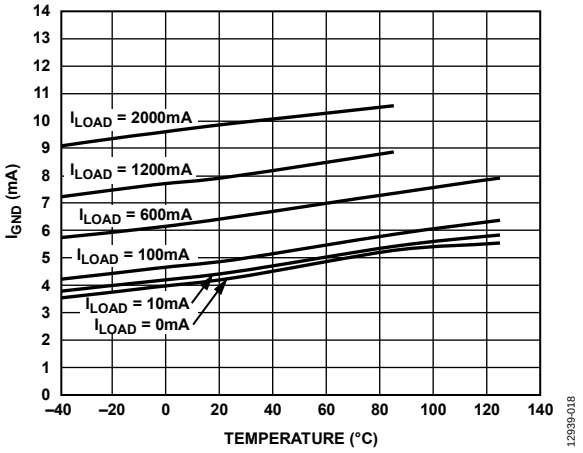

Figure 18. Ground Current (I_{GND}) vs. Temperature at Various Loads, V_{OUT} = 1.2 V

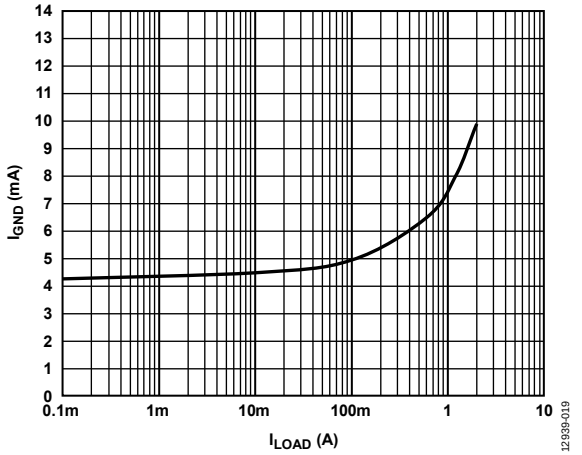

Figure 19. Ground Current (I_{GND}) vs. Load Current (I_{LOAD}), V_{OUT} = 1.2 V

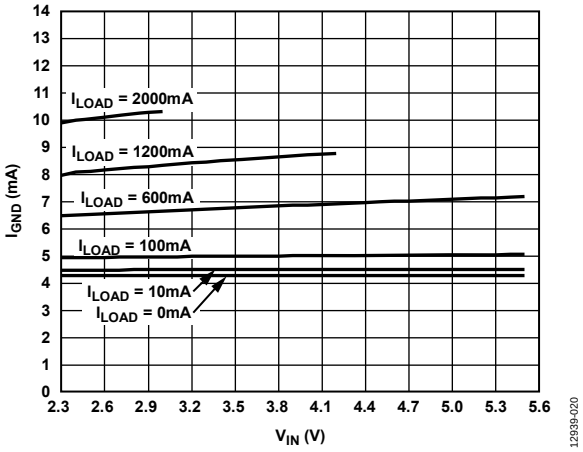

Figure 20. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 1.2 V

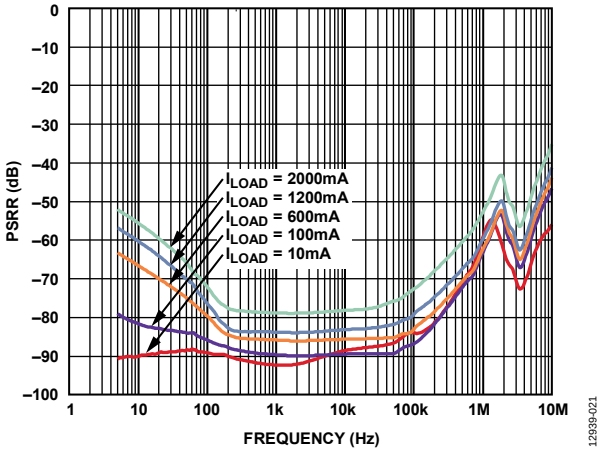

Figure 21. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = 3.3 V, V_{IN} = 4.0 V

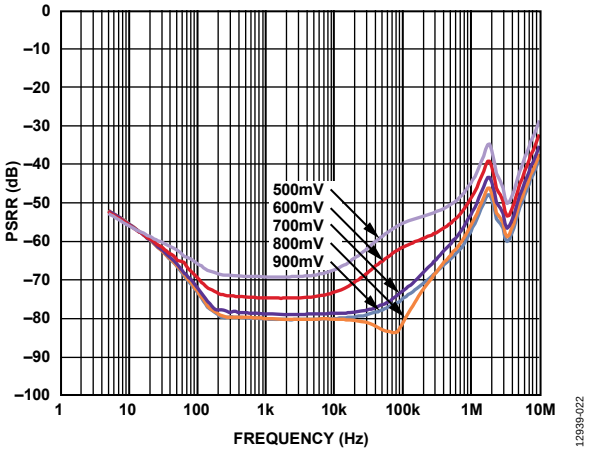

Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Headroom Voltages, V_{OUT} = 3.3 V, 2 A Load

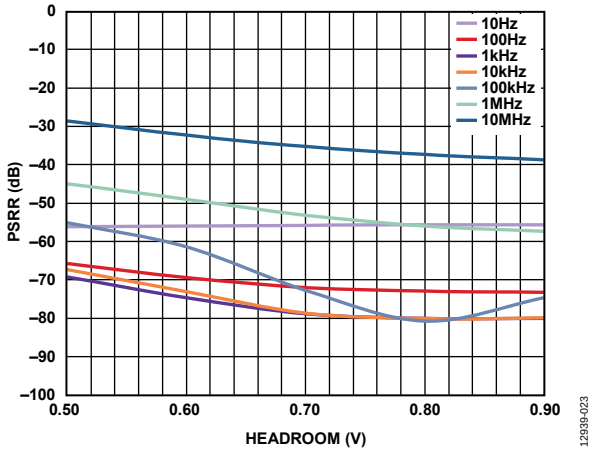

Figure 23. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage at Various Frequencies, V_{OUT} = 3.3 V, 2 A Load

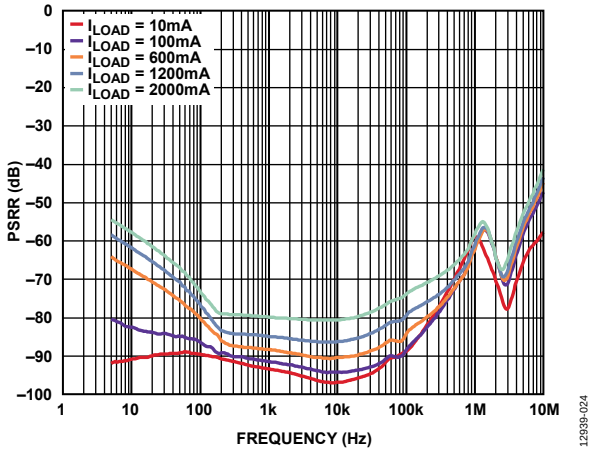

Figure 24. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = 1.2 V, V_{IN} = 2.4 V

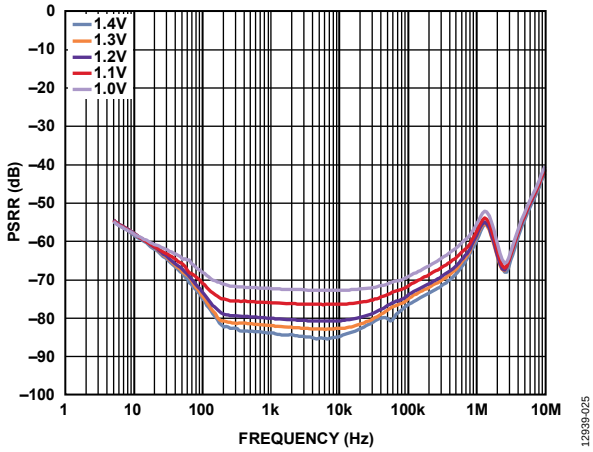

Figure 25. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Headroom Voltages, V_{OUT} = 1.2 V, 2 A Load

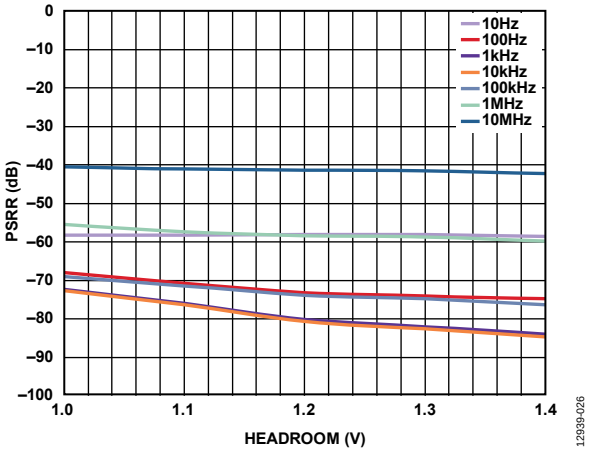

Figure 26. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage at Various Frequencies, V_{OUT} = 1.2 V, 2 A Load

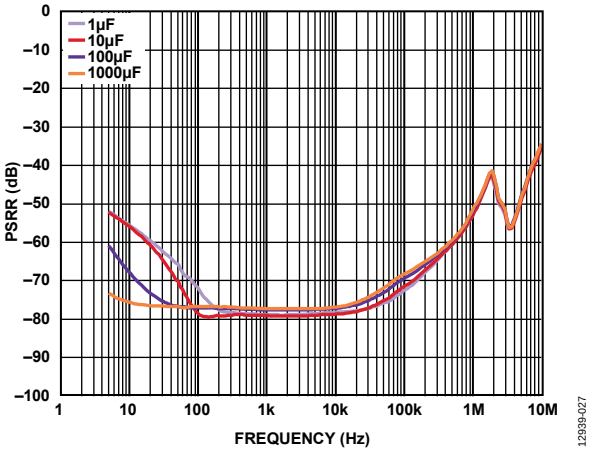

Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various C_{BYP} Values, V_{OUT} = 3.3 V, V_{IN} = 4.0 V, 2 A Load

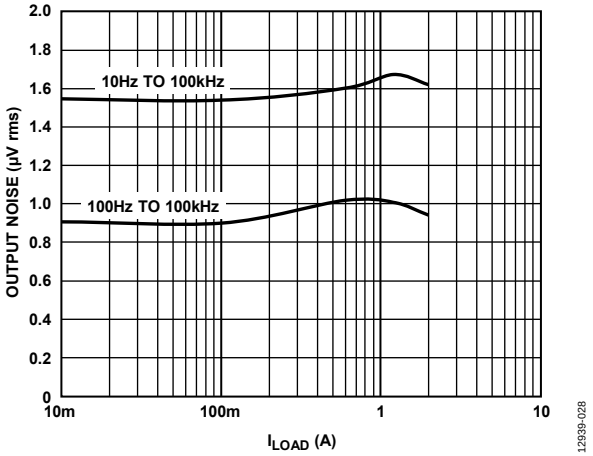

Figure 28. RMS Output Noise vs. Load Current (I_{LOAD})

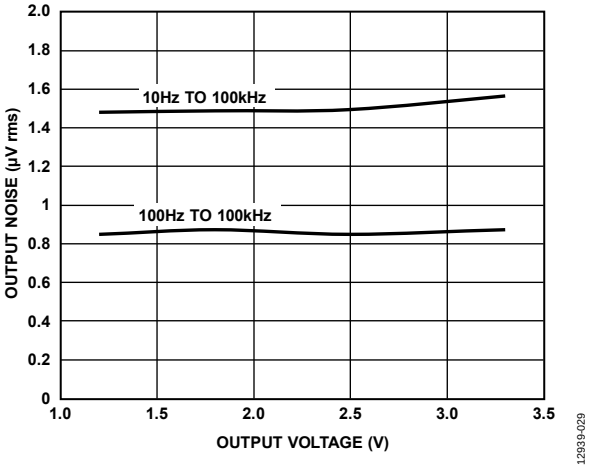

Figure 29. RMS Output Noise vs. Output Voltage

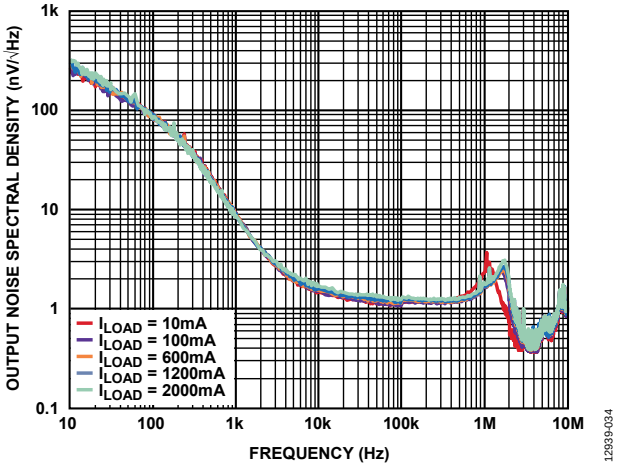

Figure 32. Output Noise Spectral Density vs. Frequency at Various Loads, 10 Hz to 10 MHz

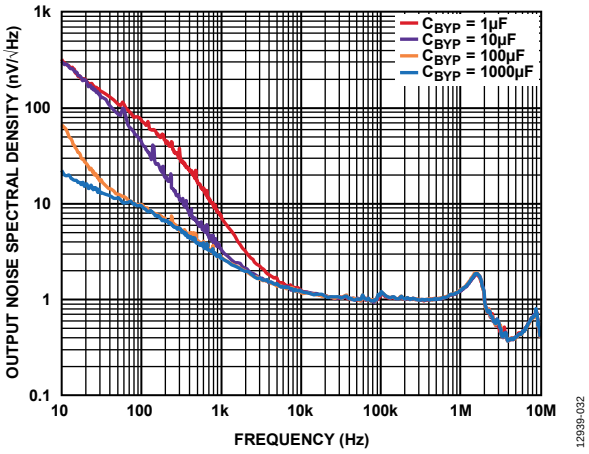

Figure 30. Output Noise Spectral Density vs. Frequency at Various Values of C_{BYP}

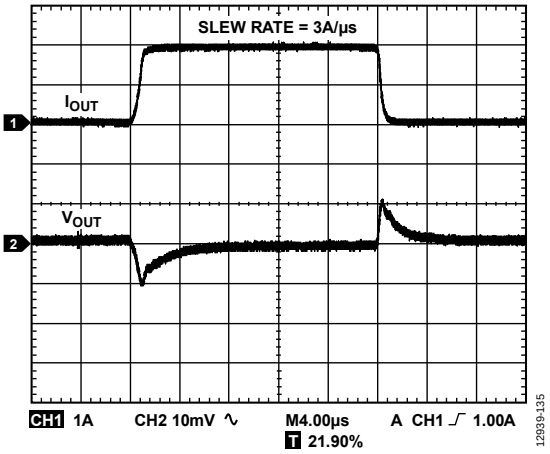

Figure 33. Load Transient Response, I_{LOAD} = 100 mA to 2 A, V_{OUT} = 3.3 V, V_{IN} = 4.0 V, Channel 1 = I_{OUT}, Channel 2 = V_{OUT}

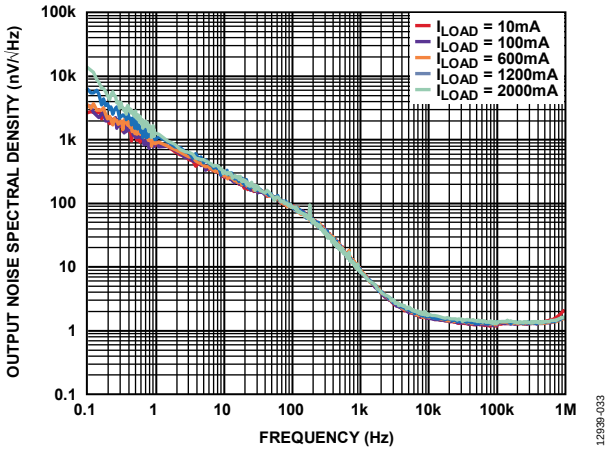

Figure 31. Output Noise Spectral Density vs. Frequency at Various Loads, 0.1 Hz to 1 MHz

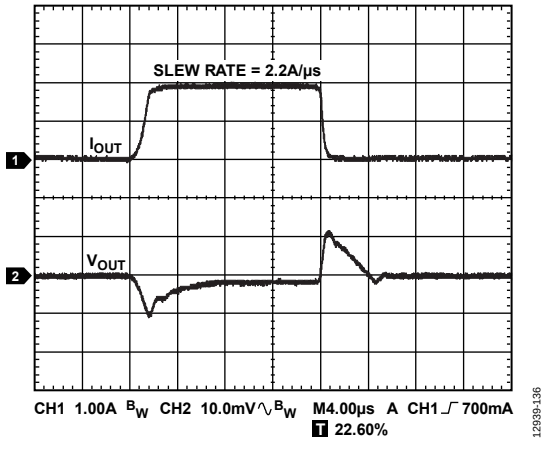

Figure 34. Load Transient Response, I_{LOAD} = 100 mA to 2 A, V_{OUT} = 3.3 V, V_{IN} = 4.0 V, C_{OUT} = 22 µF, Channel 1 = I_{OUT}, Channel 2 = V_{OUT}

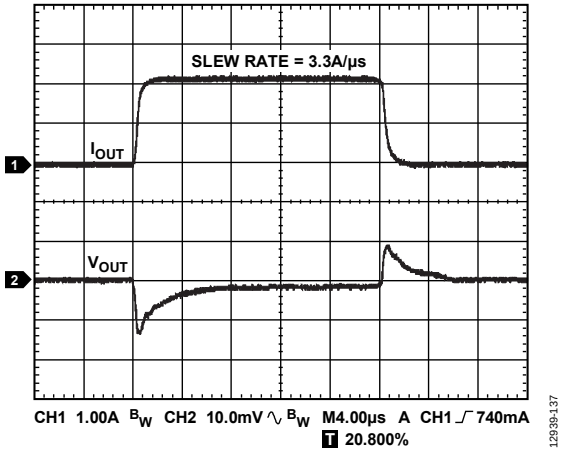

Figure 35. Load Transient Response, I_{LOAD} = 100 mA to 2 A, V_{OUT} = 1.8 V, V_{IN} = 2.5 V, Channel 1 = I_{OUT}, Channel 2 = V_{OUT}

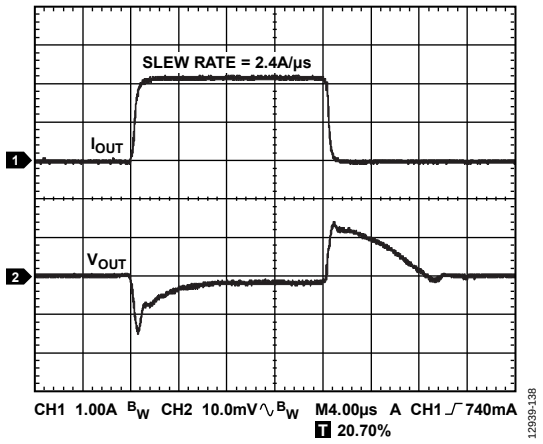

Figure 36. Load Transient Response, I_{LOAD} = 100 mA to 2 A, V_{OUT} = 1.8 V, V_{IN} = 2.5 V, C_{OUT} = 22 µF, Channel 1 = I_{OUT}, Channel 2 = V_{OUT}

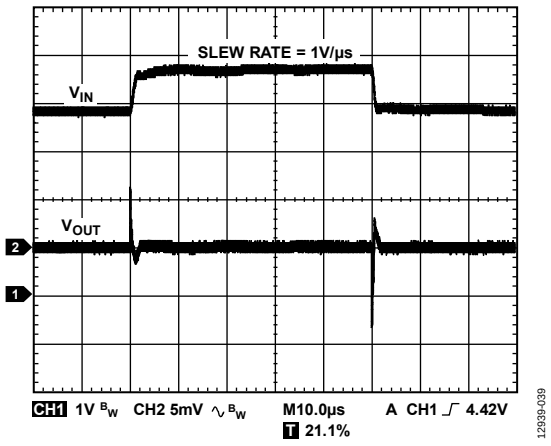

Figure 37. Line Transient Response, 1 V Input Step, I_{LOAD} = 2 A, V_{OUT} = 3.3 V, V_{IN} = 3.8 V, Channel 1 = V_{IN}, Channel 2 = V_{OUT}

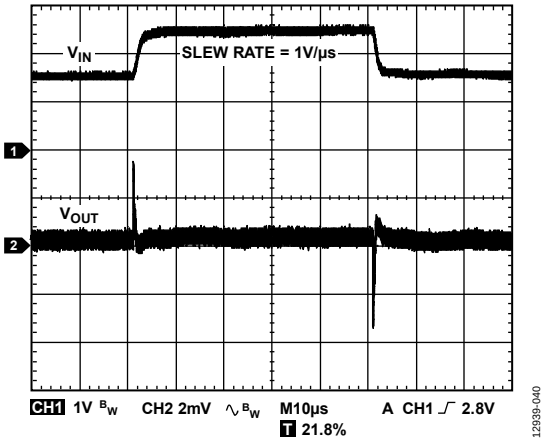

Figure 38. Line Transient Response, 1 V Input Step, I_{LOAD} = 2 A, V_{OUT} = 1.8 V, V_{IN} = 2.5 V, Channel 1 = V_{IN}, Channel 2 = V_{OUT}

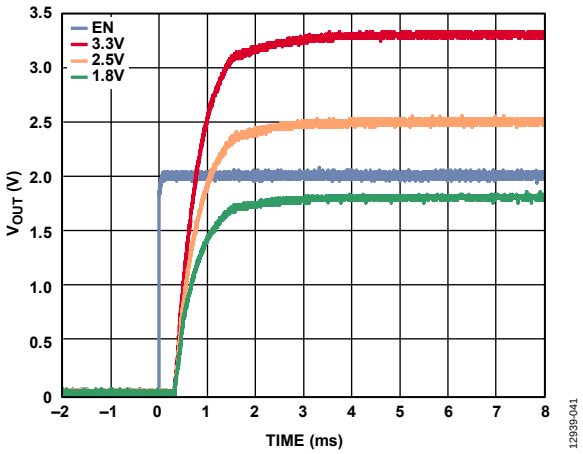

Figure 39. V_{OUT} Start-Up Time After V_{EN} Rising at Various Output Voltages, V_{IN} = 5.0 V, C_{BYP} = 1 µF

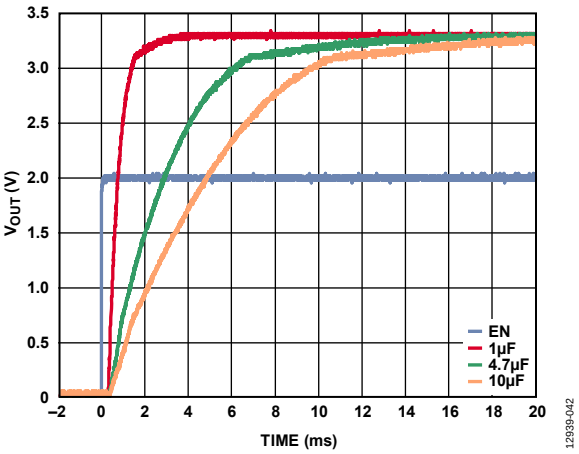

Figure 40. V_{OUT} Start-Up Time Behavior at Various Values of C_{BYP}, V_{OUT} = 3.3 V

THEORY OF OPERATION

The ADP7159 is an ultralow noise, high PSRR linear regulator targeting radio frequency (RF) applications. The input voltage range is 2.3 V to 5.5 V, and the device delivers up to 2 A of load current. The typical shutdown current consumption is 0.2 µA at room temperature.

Optimized for use with 10 µF ceramic capacitors, the ADP7159 provides excellent transient performance.

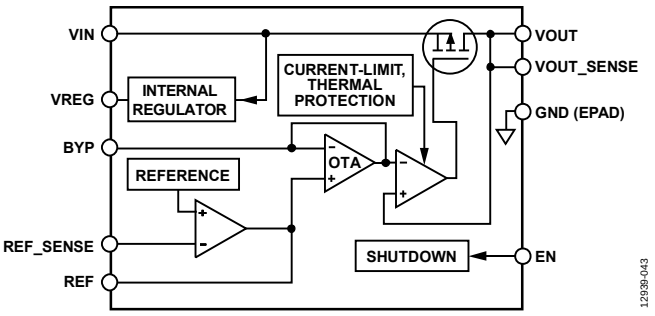

Figure 41. Simplified Internal Block Diagram

Internally, the ADP7159 consists of a reference, an error amplifier, and a P-channel MOSFET pass transistor. The output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device pulls lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device pulls higher, allowing less current to pass and decreasing the output voltage.

By heavily filtering the reference voltage, the ADP7159 achieves 1.7 nV/√Hz output typical from 10 kHz to 1 MHz. Because the error amplifier is always in unity gain, the output noise is independent of the output voltage.

The ADP7159 output voltage can be adjusted between 1.2 V and 3.3 V and is available in four models that optimize the input voltage and output voltage ranges to keep power dissipation as low as possible without compromising PSRR performance. The output voltage is determined by an external voltage divider according to the following equation:

$$V_{OUT} = 1.2\ V \times (1 + R1/R2)$$

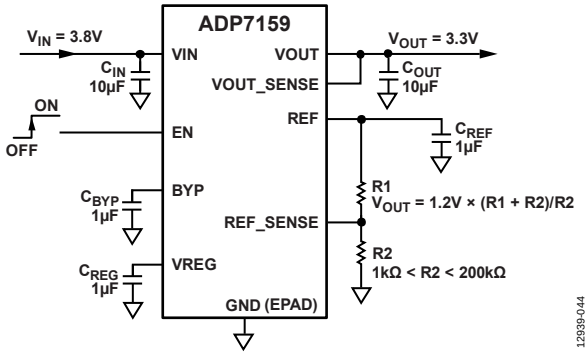

Figure 42. Typical Adjustable Output Voltage Application Schematic

The R2 value must be greater than 1 kΩ to prevent excessive loading of the reference voltage appearing on the REF pin. To minimize errors in the output voltage caused by the REF_SENSE pin input current, the R2 value must be less than 200 kΩ. For example, when R1 and R2 each equal 100 kΩ, the output voltage is 2.4 V. The output voltage error introduced by the REF_SENSE pin input current is 10 mV or 0.33%, assuming a maximum REF_SENSE pin input current of 100 nA at T_A = 125°C.

The ADP7159 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, and when EN is low, VOUT turns off. For automatic startup, tie EN to VIN.

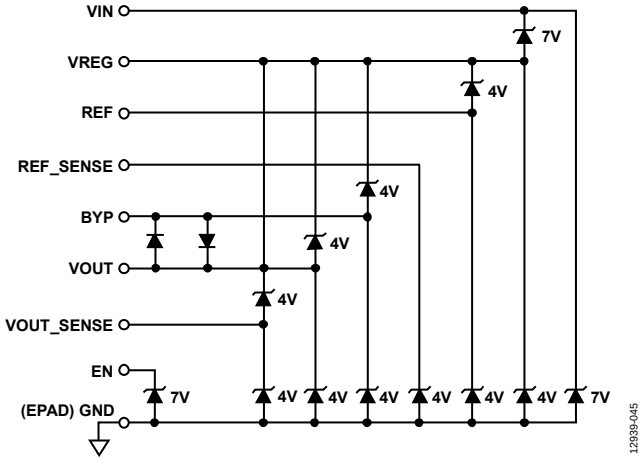

Figure 43. Simplified ESD Protection Block Diagram

The ESD protection devices are shown in the block diagram as Zener diodes (see Figure 43).

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP7159 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produces complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance within minutes. ADIsimPower can optimize designs for cost, area, efficiency, and device count, taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

CAPACITOR SELECTION

Multilayer ceramic capacitors (MLCCs) combine small size, low ESR, low effective series inductance (ESL), and wide operating temperature range, making them an ideal choice for bypass capacitors. They are not without faults, however. Depending on the dielectric material, the capacitance can vary dramatically with temperature, dc bias, and ac signal level. Therefore, selecting the proper capacitor results in the best circuit performance.

Output Capacitor

The ADP7159 is designed for operation with ceramic capacitors but functions with most commonly used capacitors when care is taken with regard to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 10 µF capacitance with an ESR of 0.2 Ω or less is recommended to ensure the stability of the ADP7159. Output capacitance also affects transient response to changes in load current. Using a larger value of output capacitance improves the transient response of the ADP7159 to large changes in load current. Figure 44 shows the transient responses for an output capacitance value of 10 µF.

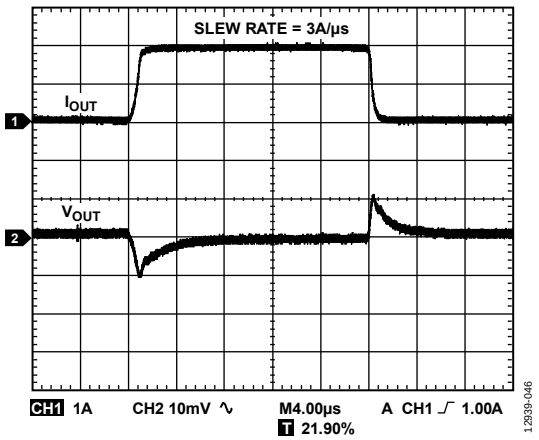

Figure 44. Output Transient Response, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, Channel 1 = Load Current, Channel 2 = V_{OUT}

Input and VREG Capacitor

Connecting a 10 µF or greater capacitor from VIN to ground reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered.

To maintain the best possible stability and PSRR performance, connect a 1 µF or greater capacitor from VREG to ground.

REF Capacitor

The REF capacitor, C_{REF}, is necessary to stabilize the reference amplifier. Connect a 1 µF or greater capacitor between REF and ground.

BYP Capacitor

The BYP capacitor, C_{BYP}, is necessary to filter the reference buffer. A 1 µF capacitor is typically connected between BYP and ground. Capacitors as small as 0.1 µF can be used; however, the output noise voltage of the LDO increases as a result.

In addition, the BYP capacitor value can be increased to reduce the noise below 1 kHz at the expense of increasing the start-up time of the LDO. Very large values of C_{BYP} significantly reduce the noise below 10 Hz. Tantalum capacitors are recommended for capacitors larger than approximately 33 µF because solid tantalum capacitors are less prone to microphonic noise issues. A 1 µF ceramic capacitor in parallel with the larger tantalum capacitor is recommended to ensure good noise performance at higher frequencies.

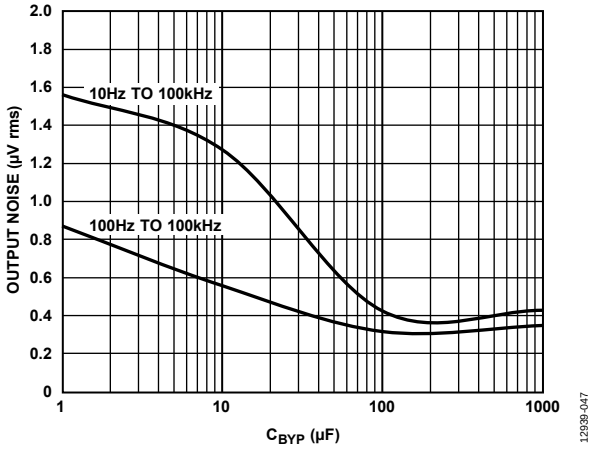

Figure 45. RMS Output Noise vs. Bypass Capacitance (C_{BYP})

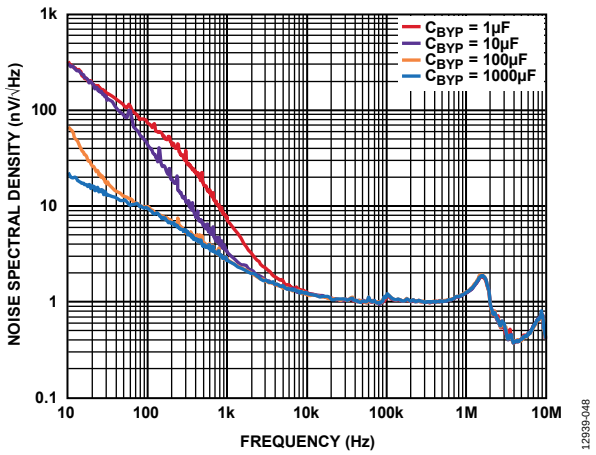

Figure 46. Noise Spectral Density vs. Frequency at Various C_{BYP} Values

Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP7159 if they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 50 V are recommended. However, Y5V and Z5U dielectrics are not recommended because of their poor temperature and dc bias characteristics.

Figure 47 depicts the capacitance vs. dc bias voltage of a 1206, 10 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

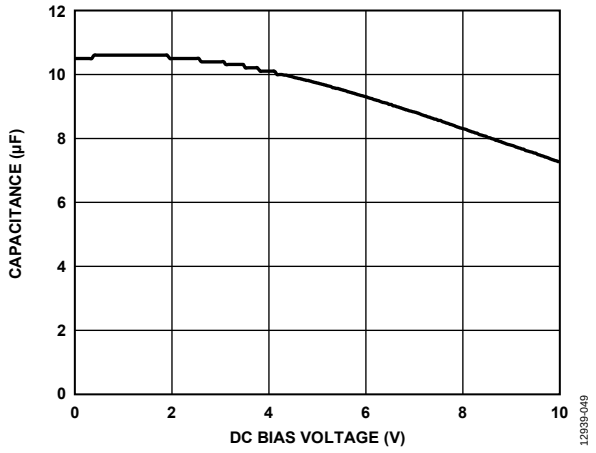

Figure 47. Capacitance vs. DC Bias Voltage

Use Equation 1 to determine the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - Tempco) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
Tempco is the worst case capacitor temperature coefficient.
TOL is the worst case component tolerance.

In this example, the worst case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 9.72 µF at 5 V, as shown in Figure 47.

Substituting these values in Equation 1 yields

$$C_{EFF} = 9.72\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.44\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP7159, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADP7159 also incorporates an internal UVLO circuit to disable the output voltage when the input voltage is less than the minimum input voltage rating of the regulator. The upper and lower thresholds are internally fixed with about 200 mV of hysteresis.

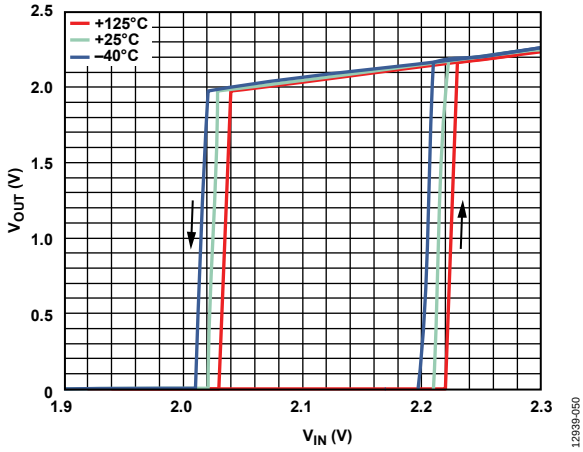

Figure 48. Typical UVLO Behavior at Various Temperatures, V_{OUT} = 3.3 V

Figure 48 shows the typical hysteresis of the UVLO function. This hysteresis prevents on/off oscillations that can occur when caused by noise on the input voltage as it passes through the threshold points.

PROGRAMMABLE PRECISION ENABLE

The ADP7159 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 49, when a rising voltage on EN crosses the upper threshold, nominally 1.22 V, V_{OUT} turns on. When a falling voltage on EN crosses the lower threshold, nominally 1.13 V, V_{OUT} turns off. The hysteresis of the EN threshold is approximately 90 mV.

The ADP7159 includes a discharge resistor on each VOUT, VREG, VREF, and BYP pin. These resistors are turned on when the device is disabled, helping to quickly discharge the associated capacitor.

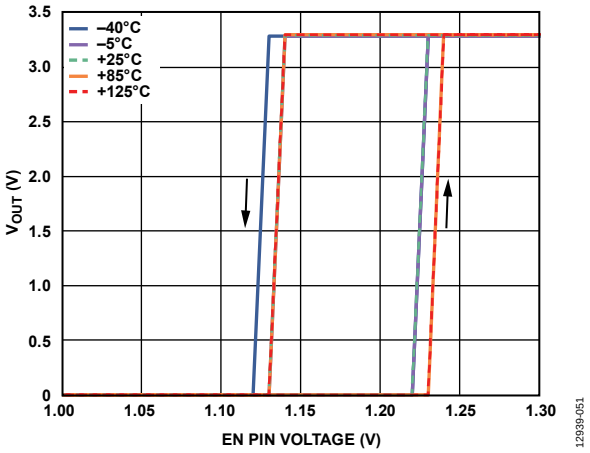

Figure 49. Typical V_{OUT} Response to EN Pin Operation

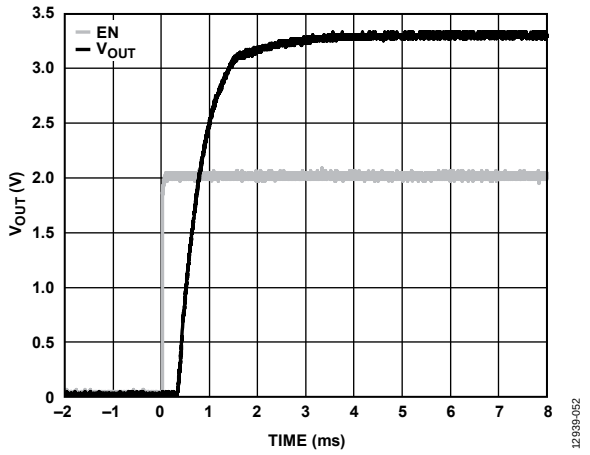

Figure 50. Typical V_{OUT} Response to EN Pin Operation (V_{EN}), V_{OUT} = 3.3 V, V_{IN} = 5 V, C_{BYP} = 1 µF

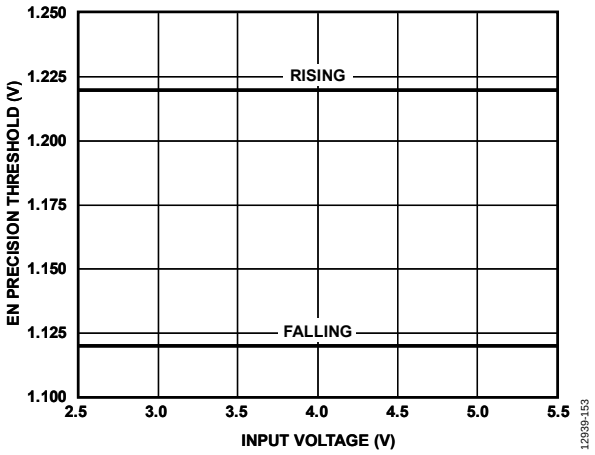

Figure 51. Typical EN Threshold vs. Input Voltage (V_{IN})

The upper and lower thresholds are user programmable and can be set higher than the nominal 1.22 V threshold by using two resistors. The resistance values, R_{EN1} and R_{EN2}, can be determined from

$$R_{EN1} = R_{EN2} \times (V_{EN} - 1.22\ V)/1.22\ V$$

where:

R_{EN2} typically ranges from 10 kΩ to 100 kΩ.
V_{EN} is the desired turn-on voltage.

The hysteresis voltage increases by the factor

$$(R_{EN1} + R_{EN2})/R_{EN2}$$

For the example shown in Figure 52, the EN threshold is 2.44 V with a hysteresis of 200 mV.

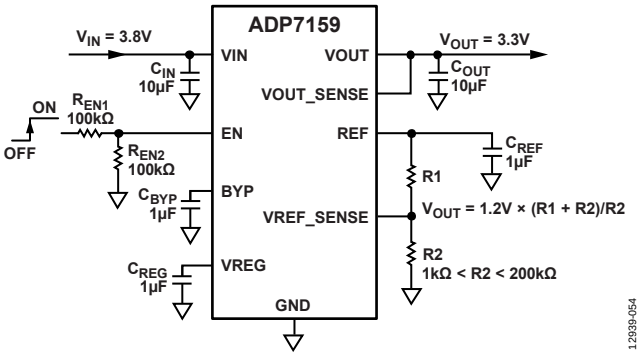

Figure 52. Typical EN Pin Voltage Divider

Figure 52 shows the typical hysteresis of the EN pin. This hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

START-UP TIME

The ADP7159 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for a 3.3 V output is approximately 1.2 ms from the time the EN active threshold is crossed to when the output reaches 90% of its final value.

The rise time in seconds of the output voltage (10% to 90%) is approximately 0.0012 × C_{BYP}, where C_{BYP} is in microfarads.

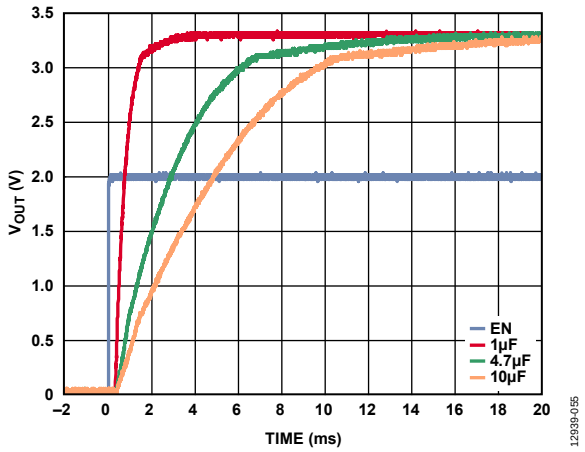

Figure 53. Typical Start-Up Behavior with C_{BYP} = 1 µF to 10 µF

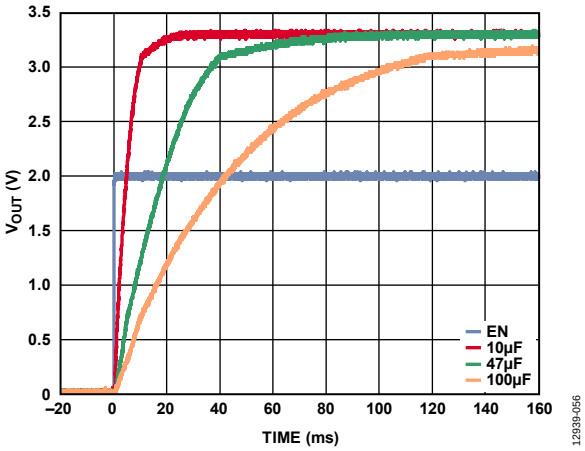

Figure 54. Typical Start-Up Behavior with C_{BYP} = 10 µF to 100 µF

REF, BYP, AND VREG PINS

REF, BYP, and VREG generate voltages internally (V_{REF}, V_{BYP}, and V_{REG}) that require external bypass capacitors for proper operation. Do not, under any circumstances, connect any loads to these pins, because doing so compromises the noise and PSRR performance of the ADP7159. Using larger values of C_{BYP}, C_{REF}, and C_{REG} is acceptable but can increase the start-up time, as described in the Start-Up Time section.

CURRENT-LIMIT AND THERMAL SHUTDOWN

The ADP7159 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP7159 is designed to current limit when the output load reaches 3 A (typical). When the output load exceeds 3 A, the output voltage is reduced to maintain a constant current limit.

When the ADP7159 junction temperature exceeds 150°C, the thermal shutdown circuit turns off the output voltage, reducing the output current to zero. Extreme junction temperature can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP7159 does not return to operation after thermal shutdown until the on-chip temperature falls below 135°C. When the device exits thermal shutdown, a soft start is initiated to reduce the inrush current.

Current limit and thermal shutdown protections are intended to protect the device against accidental overload conditions. Cases with a hard short from VOUT to ground or an extremely long soft-start timer typically cause the device to experience thermal oscillations between the current limit and thermal shutdown.

THERMAL CONSIDERATIONS

In applications with a low input to output voltage differential, the ADP7159 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 125°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2. To guarantee reliable operation, the junction temperature of the ADP7159 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction temperature and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds used, as well as the amount of copper used to solder the package ground and the exposed pad to the PCB.

Table 7 shows typical θ_{JA} values of the 8-lead SOIC and 10-lead LFCSP packages for various PCB copper sizes.

Table 8 shows the typical Ψ_{JB} values of the 8-lead SOIC and 10-lead LFCSP.

Table 7. Typical θ_{JA} Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**10-Lead LFCSP**	**8-Lead SOIC**
25[1]	130.2	123.8
100	93.0	90.4
500	65.8	66.0
1000	55.6	56.6
6400	44.1	45.5

[1] Device soldered to minimum size pin traces.

Table 8. Typical Ψ_{JB} Values

Package	**Ψ_{JB} (°C/W)**
10-Lead LFCSP	29.1
8-Lead SOIC	30.1

The junction temperature of the ADP7159 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{OUT}) \times I_{LOAD}) + (V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation caused by ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following equation:

$$T_J = T_A + (((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \theta_{JA}) \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C.

The heat dissipation from the package can be improved by increasing the amount of copper attached to the pins and exposed pad of the ADP7159. Adding thermal planes underneath the package also improves thermal performance. However, as shown in Table 7, a point of diminishing returns is eventually reached, beyond which an increase in the copper area does not yield significant reduction in the junction to ambient thermal resistance.

Figure 55 to Figure 60 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

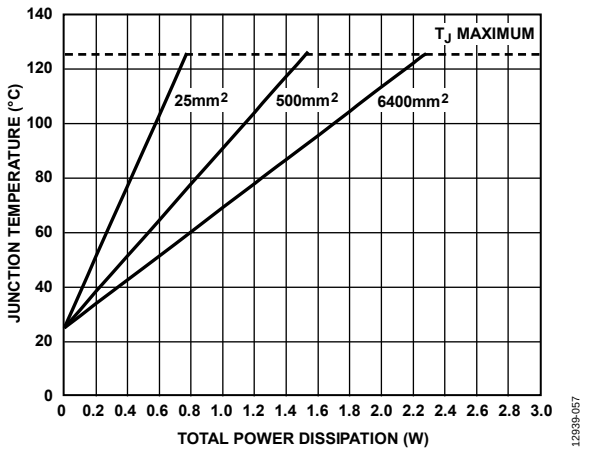

Figure 55. Junction Temperature vs. Total Power Dissipation for the 10-Lead LFCSP, T_A = 25°C

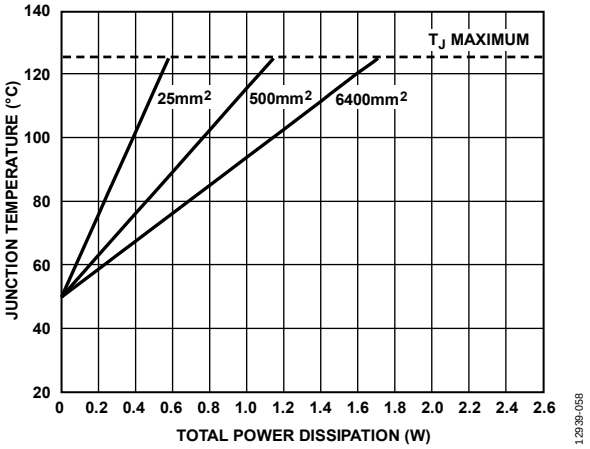

Figure 56. Junction Temperature vs. Total Power Dissipation for the 10-Lead LFCSP, T_A = 50°C

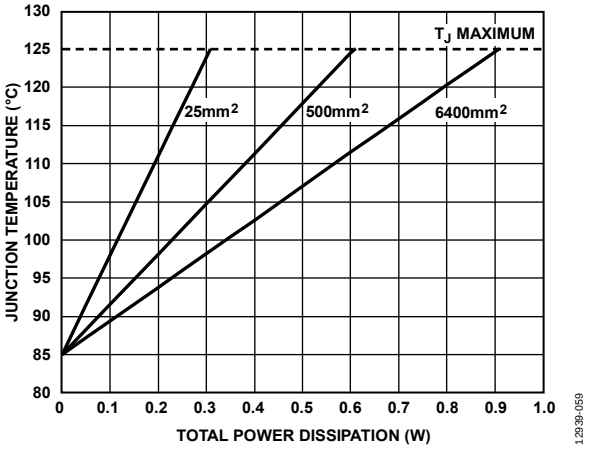

Figure 57. Junction Temperature vs. Total Power Dissipation for the 10-Lead LFCSP, T_A = 85°C

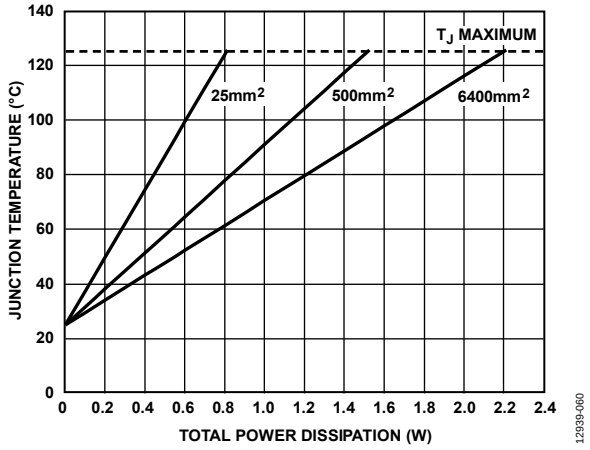

Figure 58. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 25°C

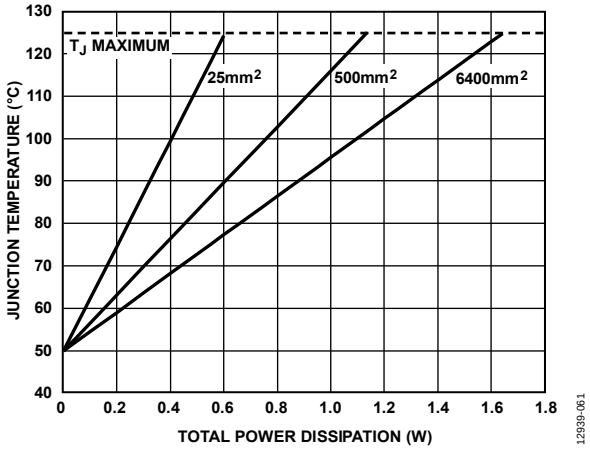

Figure 59. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 50°C

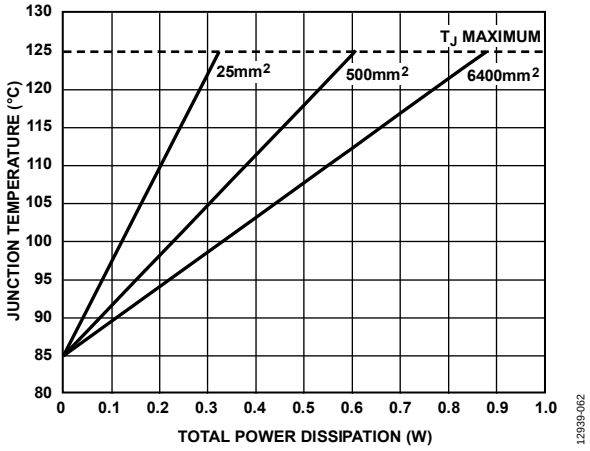

Figure 60. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 85°C

Thermal Characterization Parameter (Ψ_{JB})

When board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 61 and Figure 62). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 29.1°C/W for the 10-lead LFCSP package and 30.1°C/W for the 8-lead SOIC package.

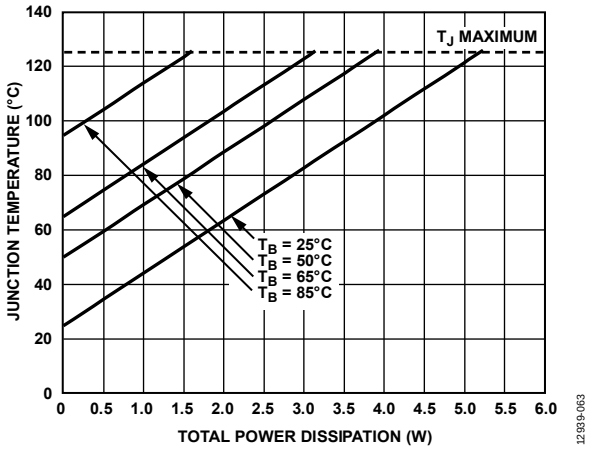

Figure 61. Junction Temperature vs. Total Power Dissipation for the 10-Lead LFCSP

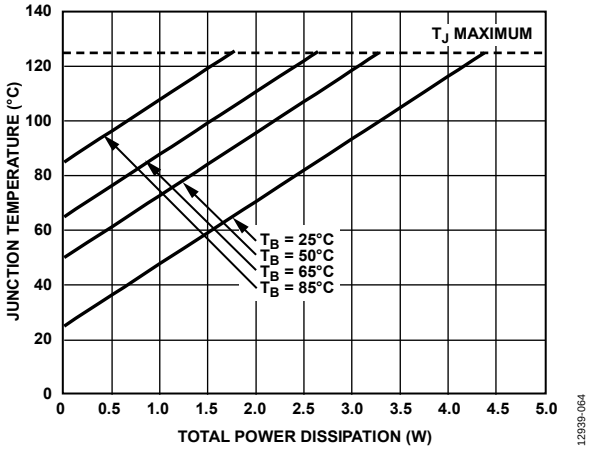

Figure 62. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC

PSRR PERFORMANCE

The ADP7159 is available in four models that optimize power dissipation and PSRR performance as a function of input and output voltage. See Table 9 and Table 10 for selection guides.

It is recommended to select the corresponding product model for a particular output voltage range to achieve optimized PSRR performance. For example, select the ADP7159-04 model for V_{OUT} = 3.3 V to achieve >65 dB PSRR (10 Hz to 100 kHz) with 500 mV headroom.

When considering a V_{OUT} = 1.8 V case, note that all four product models can generate a 1.8 V output, but the ADP7159-01 model provides the best PSRR performance, though other models, like the ADP7159-04, are still capable of generating a 1.8 V output for PSRR relaxed applications.

The ADP7159 supports a 2.3 V to 5.5 V input range. Typically, a minimum 500 mV headroom is required to achieve the best PSRR performance above the maximum output voltage (V_{OUT_MAX}) at 2 A. For example, the ADP7159-04 requires a minimum 3.8 V input voltage to achieve the best PSRR performance for a 3.3 V output at 2 A.

Table 9. Model Selection Guide for PSRR

		PSRR (dB) at 2 A; $V_{IN} = V_{OUT\_MAX} + 0.5$ V			PSRR (dB) at 1.2 A; $V_{IN} = V_{OUT\_MAX} + 0.5$ V		
Model	**V_{OUT_MAX} (V)**	**10 kHz**	**100 kHz**	**1 MHz**	**10 kHz**	**100 kHz**	**1 MHz**
ADP7159-01	1.8	55	55	40	70	78	52
ADP7159-02	2.3	61	55	45	72	70	53
ADP7159-03	2.9	65	65	45	75	78	55
ADP7159-04	3.3	68	70	45	82	72	55

Table 10. Model Selection Guide for Input Voltage

Model	**Adjustable V_{OUT} Range (V)**	**V_{OUT} Range (V) for Optimized PSRR**	**V_{REG} (V)**	**V_{IN} Range (V)**
ADP7159-01	1.2 to 1.8	1.2 to 1.8	2.1	2.3 to 5.5
ADP7159-02	1.2 to 2.3	1.8 to 2.3	2.6	2.8 to 5.5
ADP7159-03	1.2 to 2.9	2.3 to 2.9	3.2	3.4 to 5.5
ADP7159-04	1.2 to 3.3	2.9 to 3.3	3.6	3.8 to 5.5

PCB LAYOUT CONSIDERATIONS

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C_{REG}, C_{REF}, and C_{BYP}) for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins (VREG, REF, and BYP) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

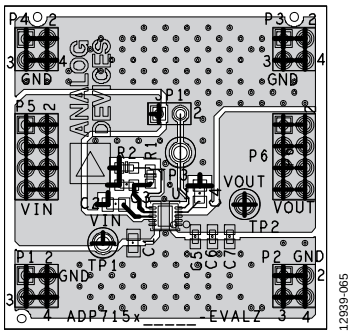

Figure 63. Sample 10-Lead LFCSP PCB Layout

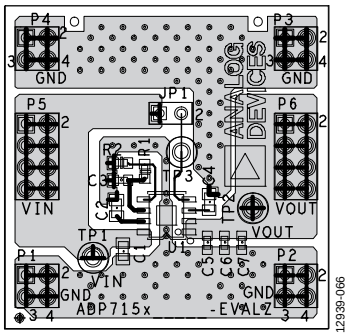

Figure 64. Sample 8-Lead SOIC PCB Layout

OUTLINE DIMENSIONS

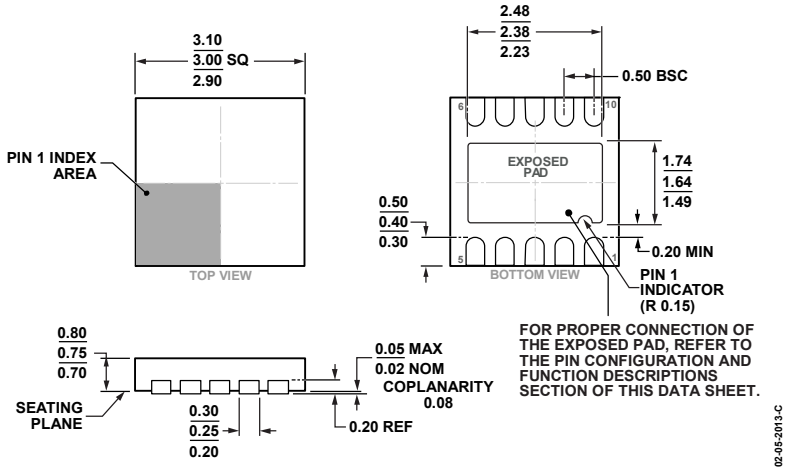

Figure 65. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-10-9)
Dimensions shown in millimeters

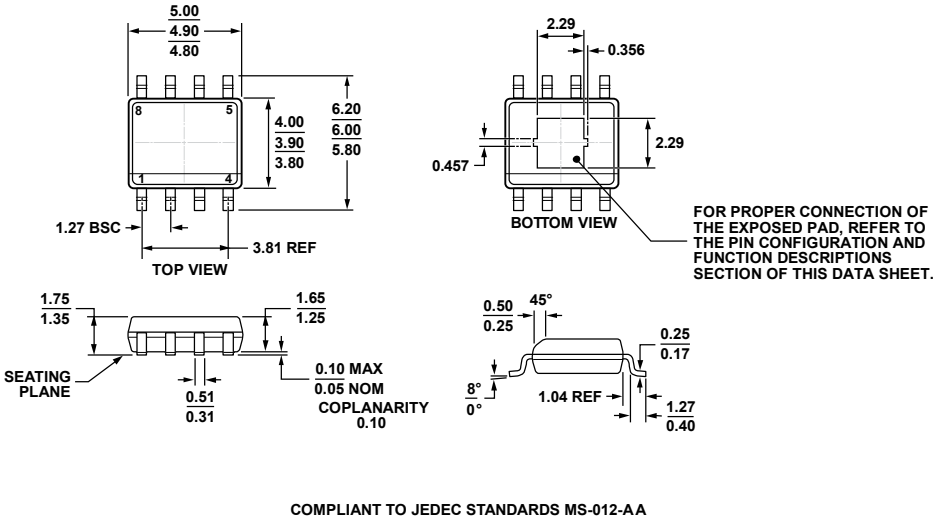

Figure 66. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Output Voltage Range (V)	Package Description	Package Option	Branding
ADP7159ACPZ-01-R7	−40°C to +125°C	1.2 to 1.8	10-Lead LFCSP	CP-10-9	LSG
ADP7159ACPZ-02-R7	−40°C to +125°C	1.2 to 2.3	10-Lead LFCSP	CP-10-9	LSH
ADP7159ACPZ-03-R7	−40°C to +125°C	1.2 to 2.9	10-Lead LFCSP	CP-10-9	LSJ
ADP7159ACPZ-04-R7	−40°C to +125°C	1.2 to 3.3	10-Lead LFCSP	CP-10-9	LSK
ADP7159ARDZ-01-R7	−40°C to +125°C	1.2 to 1.8	8-Lead SOIC_N_EP	RD-8-1	
ADP7159ARDZ-02-R7	−40°C to +125°C	1.2 to 2.3	8-Lead SOIC_N_EP	RD-8-1	
ADP7159ARDZ-03-R7	−40°C to +125°C	1.2 to 2.9	8-Lead SOIC_N_EP	RD-8-1	
ADP7159ARDZ-04-R7	−40°C to +125°C	1.2 to 3.3	8-Lead SOIC_N_EP	RD-8-1	
ADP7159CP-04-EVALZ			Evaluation Board		
ADP7159RD-04-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] To order a device with voltage options other than the listed options, contact your local Analog Devices sales or distribution representative.

D12939-0-5/16(A)

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