

### Product Summary

$V_{(BR)DSS}$	$R_{DS(ON) \max}$	$I_D \max$ $T_A = 25^\circ C$
30V	23mΩ @ $V_{GS} = 10V$	7.0A
	33mΩ @ $V_{GS} = 4.5V$	6.0A

### Features and Benefits

- 100% Unclamped Inductive Switch (UIS) test in production
- Low  $R_{DS(ON)}$  – ensures on state losses are minimized
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

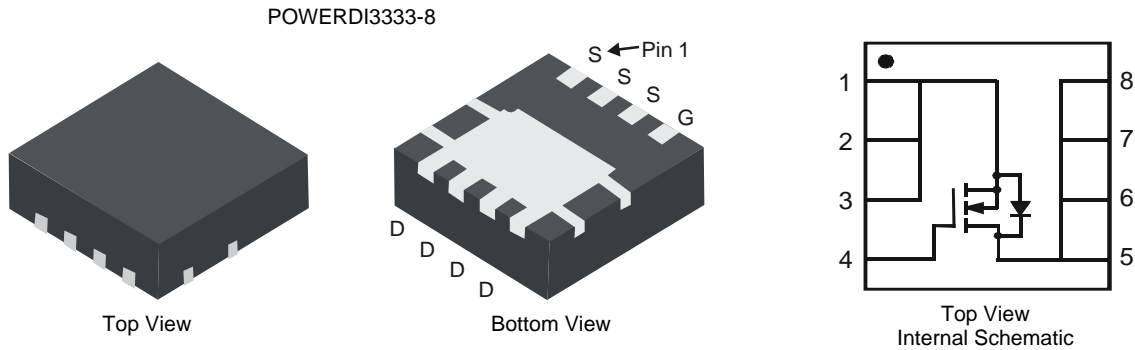
### Description and Applications

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Backlighting
- Power Management Functions
- DC-DC Converters

### Mechanical Data

- Case: POWERDI3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.008 grams (approximate)

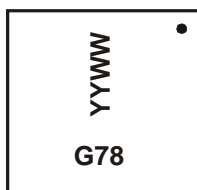


### Ordering Information (Note 4)

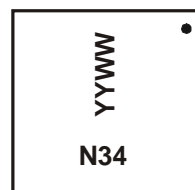
Part Number	Case	Packaging
DMG7408SFG-7	POWERDI3333-8	2000/Tape & Reel
DMG7408SFG-13	POWERDI3333-8	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com>.

### Marking Information



G78 = Product Type Marking Code  
YYWW = Date Code Marking  
YY = Last digit of year (ex: 11 = 2011)  
WW = Week code (01 ~ 53)



N34 = Product Type Marking Code  
YYWW = Date Code Marking  
YY = Last digit of year (ex: 11 = 2011)  
WW = Week code (01 ~ 53)

**Maximum Ratings** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V <sub>DSS</sub>	30	V
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	Steady State	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	7.0 5.5	A
	t < 10s	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	9.5 7.5	A
Continuous Drain Current (Note 6) V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	6.0 5.7	A
	t < 10s	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	8.0 6.3	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I <sub>DM</sub>	66	A
Maximum Continuous Body Diode Forward Current (Note 6)			I <sub>S</sub>	3.0	A
Avalanche Current (Note 7)			I <sub>AS</sub>	9	A
Avalanche Energy (Note 7)			E <sub>AS</sub>	12	mJ

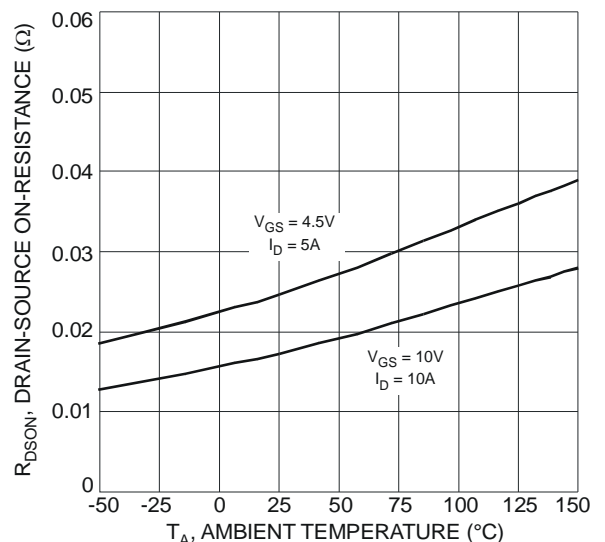
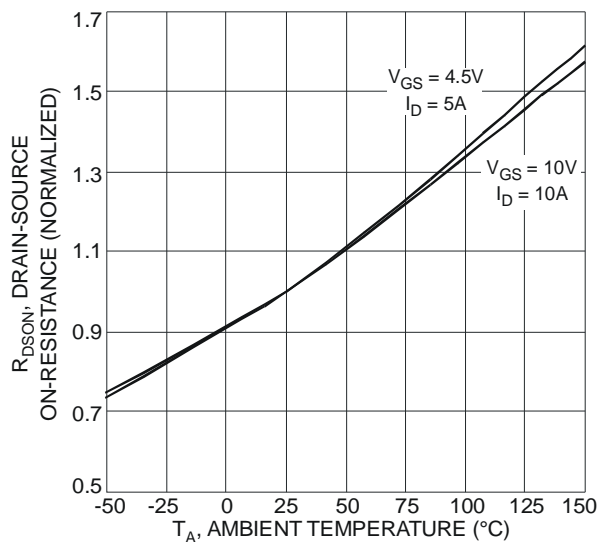
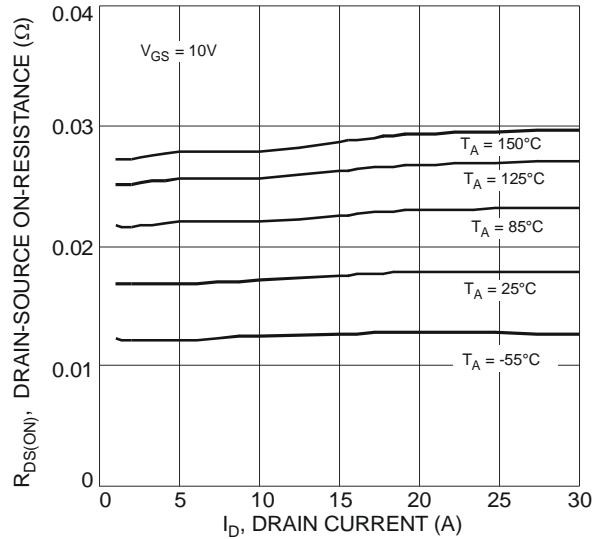
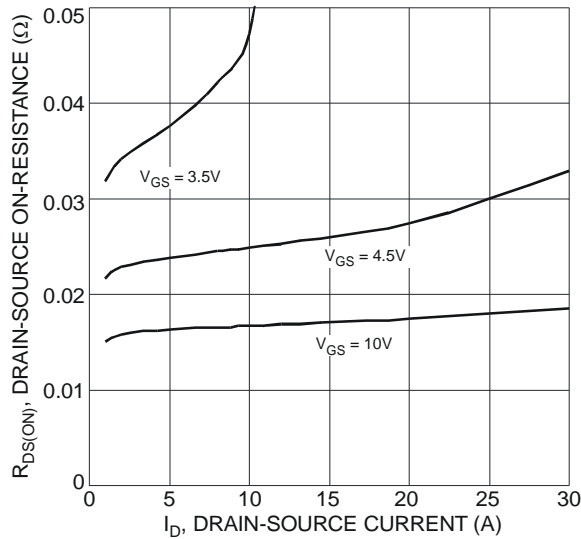
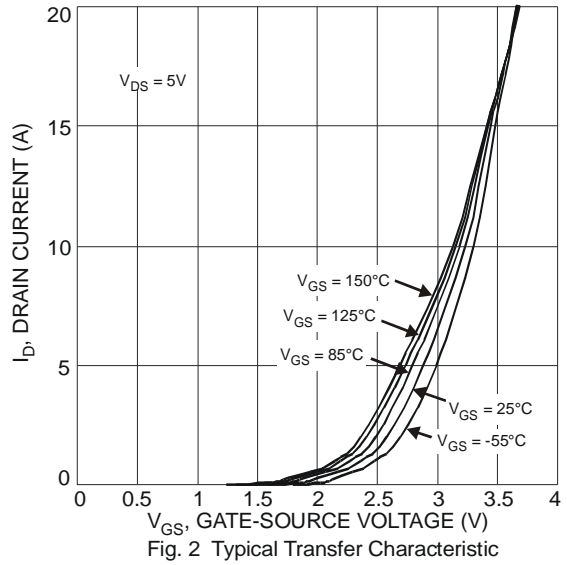
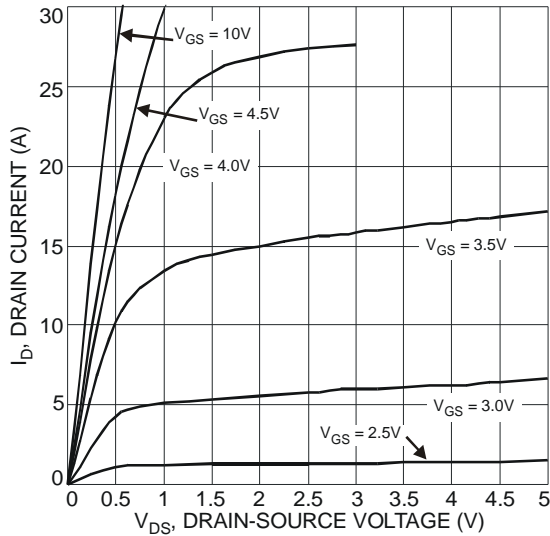
**Thermal Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		P <sub>D</sub>	1	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	R <sub>θJA</sub>	131	°C/W
	t < 10s		72	°C/W
Total Power Dissipation (Note 6)		P <sub>D</sub>	2.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	R <sub>θJA</sub>	63	°C/W
	t < 10s		35	°C/W
Thermal Resistance, Junction to Case (Note 6)		R <sub>θJC</sub>	7.1	°C/W
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	-	-	1	µA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	1.45	2.4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	15	23	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A
		-	25	33		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 7.5A
Forward Transfer Admittance	Y <sub>fs</sub>	-	11	-	S	V <sub>DS</sub> = 5V, I <sub>D</sub> = 10A
Diode Forward Voltage	V <sub>SD</sub>	-	0.72	1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	-	478.9	-	pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	-	96.7	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	61.4	-	pF	
Gate Resistance	R <sub>g</sub>	0.4	1.1	1.6	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	-	5.0	8	nC	V <sub>DS</sub> = 15V, I <sub>D</sub> = 10A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	-	10.5	17		
Gate-Source Charge	Q <sub>gs</sub>	-	1.8	-		
Gate-Drain Charge	Q <sub>gd</sub>	-	1.6	-		
Turn-On Delay Time	t <sub>D(on)</sub>	-	2.9	-	ns	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V, R <sub>G</sub> = 3Ω, R <sub>L</sub> = 1.5Ω
Turn-On Rise Time	t <sub>r</sub>	-	7.9	-	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	-	14.6	-	ns	
Turn-Off Fall Time	t <sub>f</sub>	-	3.1	-	ns	

- Notes:
5. R<sub>θJA</sub> is determined with the device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch square copper plate. R
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  7. .UIS in production with L = 0.3mH, T<sub>J</sub> = 25°C
  8. Short duration pulse test used to minimize self-heating effect.
  9. Guaranteed by design. Not subject to product testing.



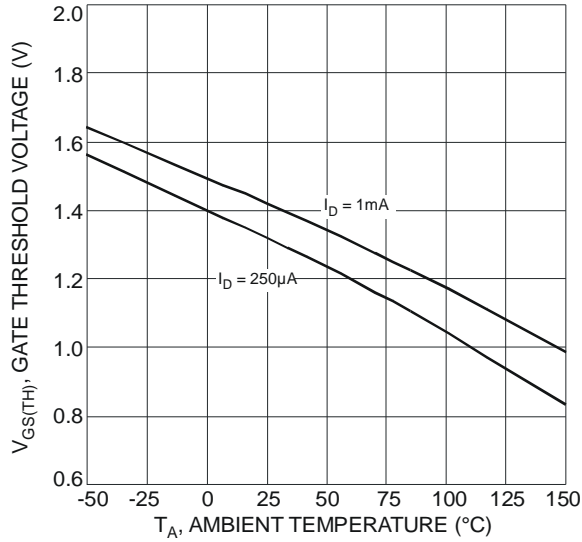


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

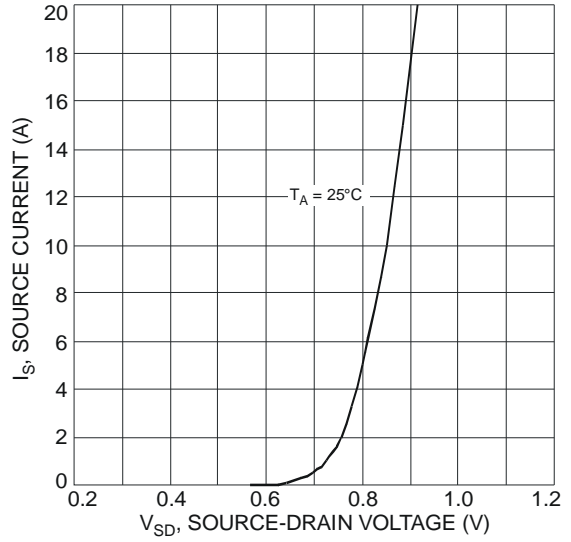


Fig. 8 Diode Forward Voltage vs. Current

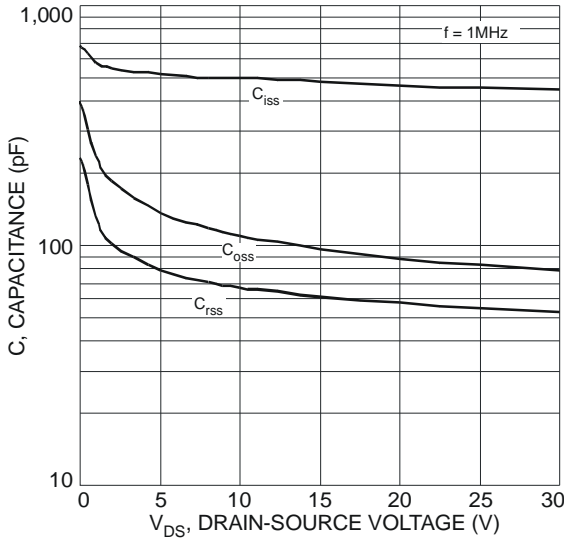


Fig. 9 Typical Total Capacitance

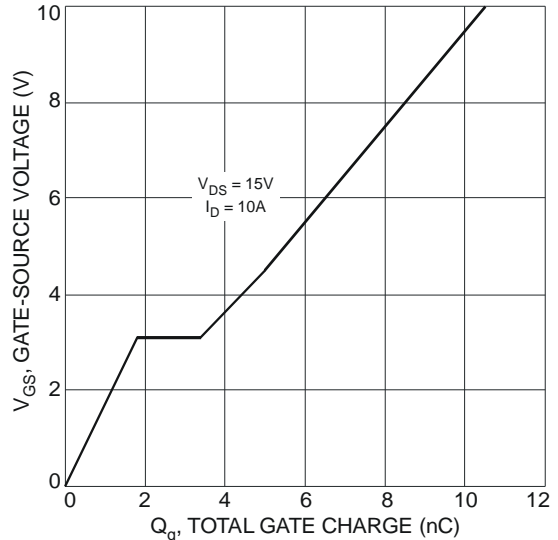


Fig. 10 Gate-Charge Characteristics

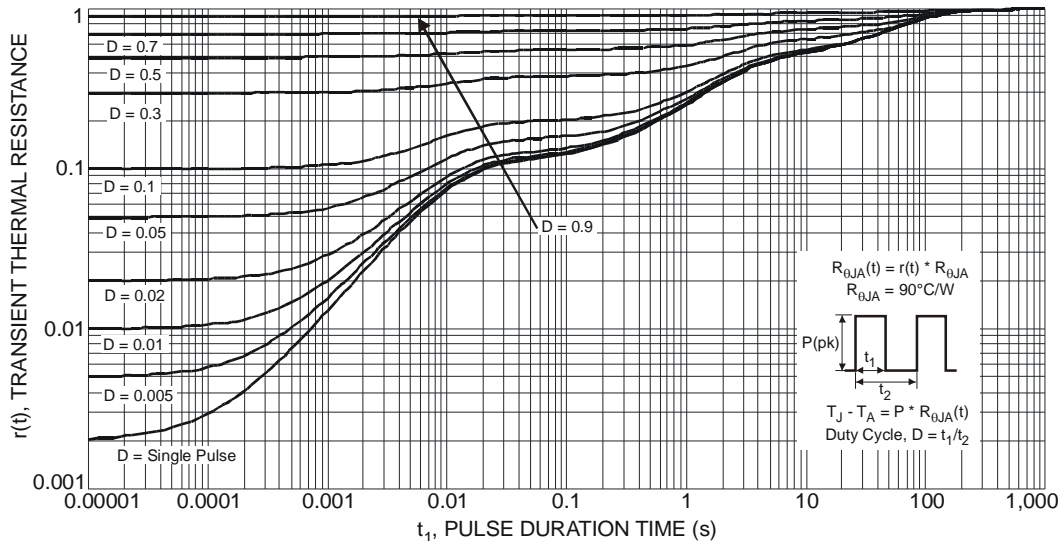
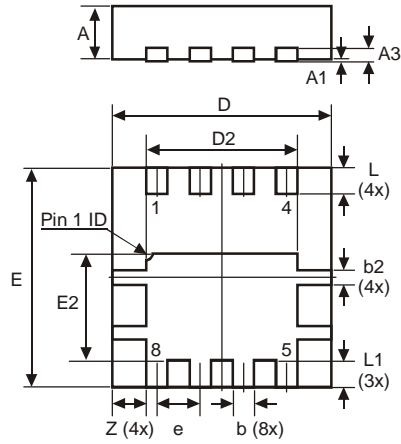


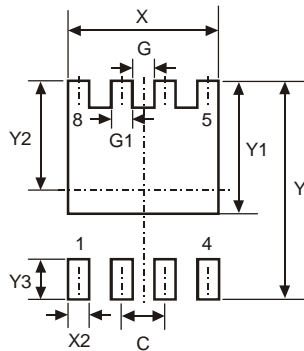
Fig. 11 Transient Thermal Response

**Package Outline Dimensions**



POWERDI3333-8			
Dim	Min	Max	Typ
D	3.25	3.35	3.30
E	3.25	3.35	3.30
D2	2.22	2.32	2.27
E2	1.56	1.66	1.61
A	0.75	0.85	0.80
A1	0	0.05	0.02
A3	-	-	0.203
b	0.27	0.37	0.32
b2	-	-	0.20
L	0.35	0.45	0.40
L1	-	-	0.39
e	-	-	0.65
Z	-	-	0.515
All Dimensions in mm			

**Suggested Pad Layout**



Dimensions	Value (in mm)
C	0.650
G	0.230
G1	0.420
Y	3.700
Y1	2.250
Y2	1.850
Y3	0.700
X	2.370
X2	0.420

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