

**Product Summary** (Typ. @  $V_{GS} = -4.5V$ ,  $T_A = +25^\circ C$ )

$V_{DSS}$	$R_{DS(on)}$	$Q_g$	$Q_{gd}$	$I_D$
-8V	8.2m $\Omega$	8.1nC	1.8nC	-10A

**Description**

This 3<sup>rd</sup> generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal  $R_{DS(on)}$  per footprint area.

**Applications**

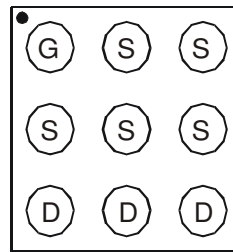
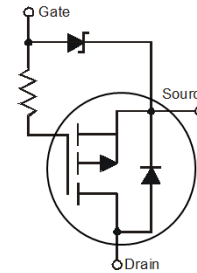
- DC-DC Converters
- Battery Management
- Load Switch

**Features**

- LD-MOS Technology with the Lowest Figure of Merit:  
 $R_{DS(on)} = 8.2m\Omega$  to Minimize On-State Losses  
 $Q_g = 8.1nC$  for Ultra-Fast Switching
- $V_{GS(th)} = -0.8V$  typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm x 1.5mm
- Height = 0.62mm for Low Profile
- ESD = 6kV HBM Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: U-WLB1515-9
- Terminal Connections: See Diagram Below

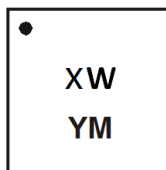
**U-WLB1515-9**

 Top-View  
Pin Configuration


Equivalent Circuit

**Ordering Information** (Note 4)

Part Number	Case	Packaging
DMP1012UCB9-7	U-WLB1515-9	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**
**U-WLB1515-9**


XW = Product Type Marking Code  
 YM = Date Code Marking  
 Y or  $\bar{Y}$  = Year (ex: B = 2014)  
 M or  $\bar{M}$  = Month (ex: 9 = September)

## Date Code Key

Year	2012	2013	2014	2015	2016	2017	2018
Code	Z	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	-8	V
Gate-Source Voltage	V <sub>GSS</sub>	-6	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	T <sub>A</sub> = +25°C	-10
		T <sub>A</sub> = +70°C	-8
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	T <sub>A</sub> = +25°C	-7.4
		T <sub>A</sub> = +70°C	-6.0
Pulsed Drain Current (Pulse duration 10μs, duty cycle ≤1%)	I <sub>DM</sub>	-50	A
Continuous Source Pin Current (Note 6)	I <sub>S</sub>	-2	—
Pulsed Source Pin Current (Pulse duration 10μs, duty cycle ≤1%)	I <sub>SM</sub>	-15	—
Continuous Gate Current	I <sub>G</sub>	-0.5	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	0.89	W
Total Power Dissipation (Note 6)	P <sub>D</sub>	1.57	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	+142.1	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	+80.5	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-8	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Gate to Source Voltage	BV <sub>GSS</sub>	-6	—	—	V	V <sub>DS</sub> = 0V, I <sub>G</sub> = -250μA
Zero Gate Voltage Drain Current @T <sub>C</sub> = +25°C	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -4.0V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	-100	nA	V <sub>GS</sub> = -4.0V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.4	-0.8	-1.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	8.2	10	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A
			10	13		
			11	14		
Forward Transfer Admittance	Y <sub>fs</sub>	—	16.8	—	S	V <sub>DS</sub> = -4V, I <sub>D</sub> = -2A
Diode Forward Voltage (Note 6)	V <sub>SD</sub>	—	-0.7	-1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -2A
Reverse Recovery Charge	Q <sub>rr</sub>	—	6.3	—	nC	V <sub>dd</sub> = -5V, I <sub>F</sub> = -2A,
Reverse Recovery Time	t <sub>rr</sub>	—	18.5	—	ns	di/dt = 200A/μs
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	817	1060	pF	V <sub>DS</sub> = -4V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	595	770	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	269	350	pF	
Series Gate Resistance	R <sub>G</sub>	—	1.9	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (4.5V)	Q <sub>g</sub>	—	8.1	10.5	nC	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -4V, I <sub>D</sub> = -2A
Gate-Source Charge	Q <sub>gs</sub>	—	0.9	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	1.8	—	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	—	6.2	10	ns	V <sub>DD</sub> = -4V, V <sub>GS</sub> = -4.5V, I <sub>DS</sub> = -2A, R <sub>G</sub> = 10Ω,
Turn-On Rise Time	t <sub>r</sub>	—	22.6	—	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	—	30.1	48	ns	
Turn-Off Fall Time	t <sub>f</sub>	—	22.7	—	ns	

- Notes:
- Device mounted on FR-4 PCB with minimum recommended pad layout.
  - Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45cm<sup>2</sup>), 2oz (0.071mm thick) Cu.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

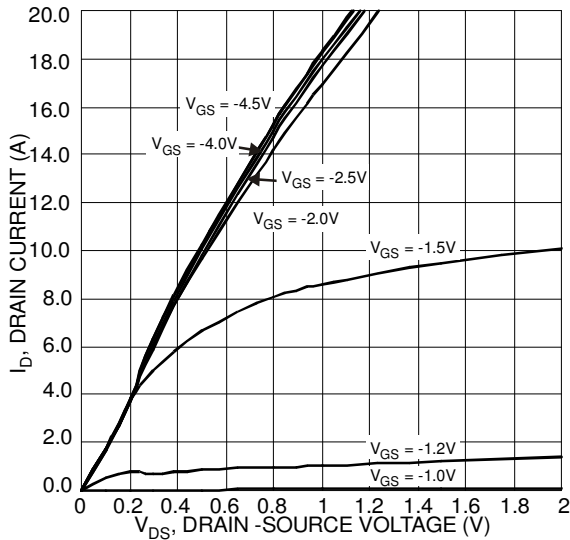


Figure 1 Typical Output Characteristics

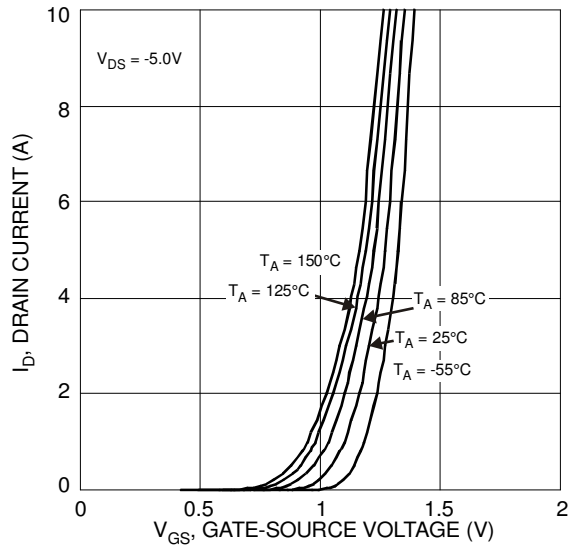


Figure 2 Typical Transfer Characteristics

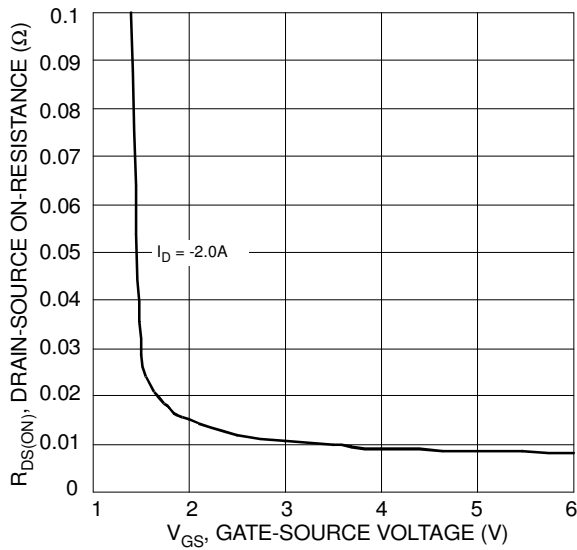


Figure 3 Typical Transfer Characteristic

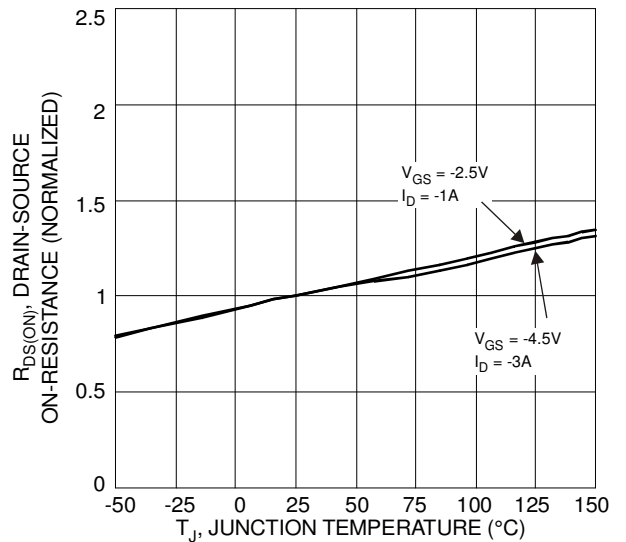


Figure 4 On-Resistance Variation with Temperature

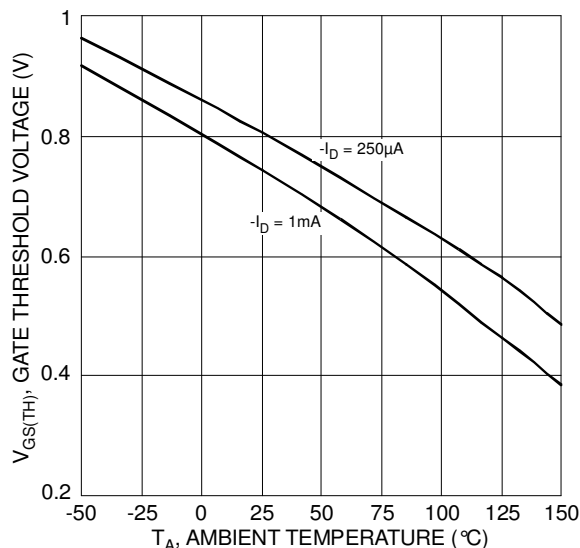


Figure 5 Gate Threshold Variation vs. Ambient Temperature

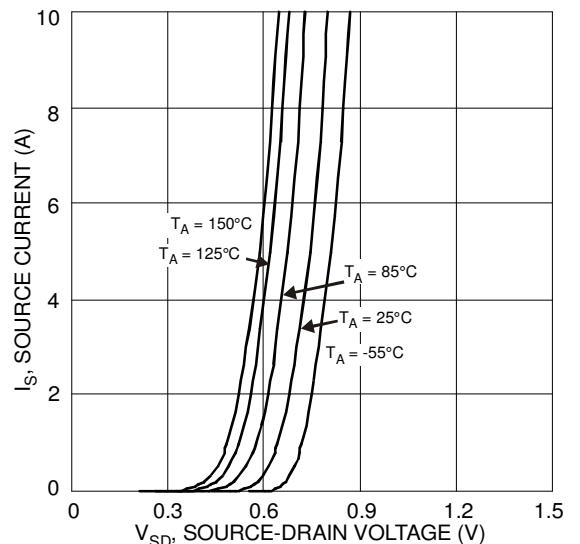


Figure 6 Diode Forward Voltage vs. Current

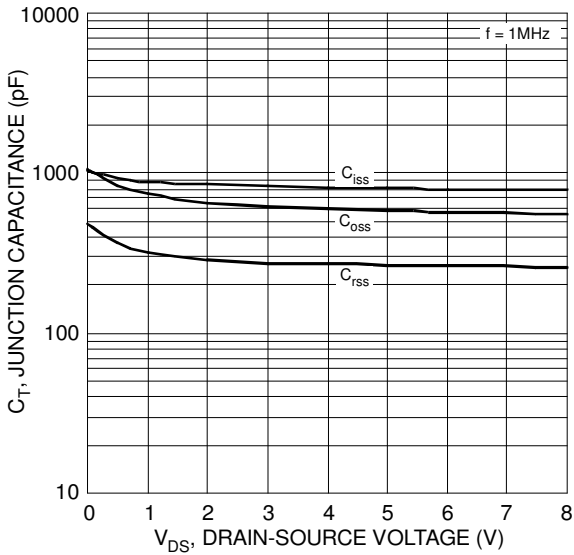


Figure 7 Typical Junction Capacitance

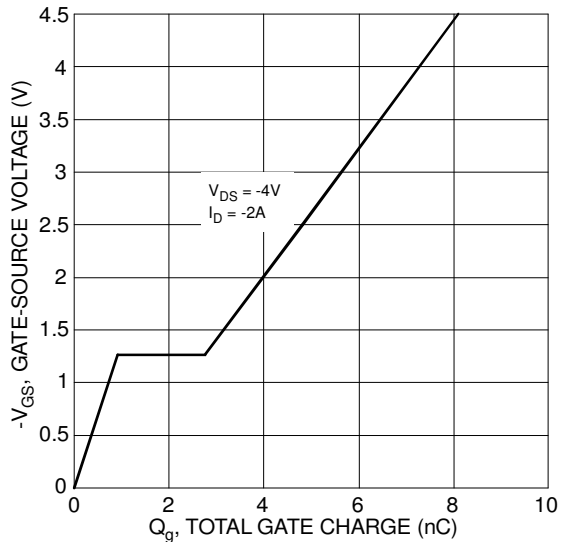


Figure 8 Gate-Charge Characteristics

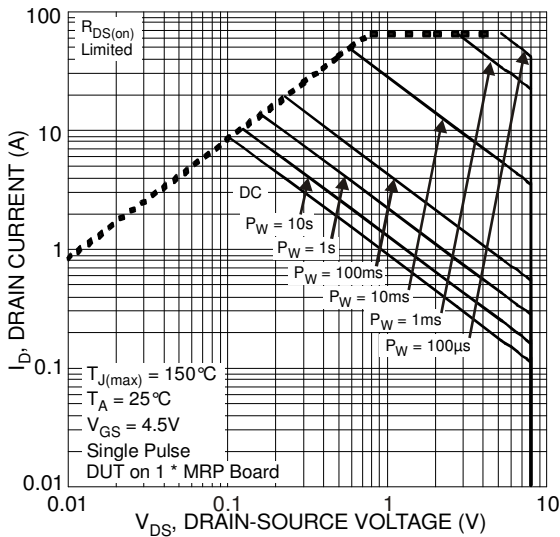


Figure 9 SOA, Safe Operation Area

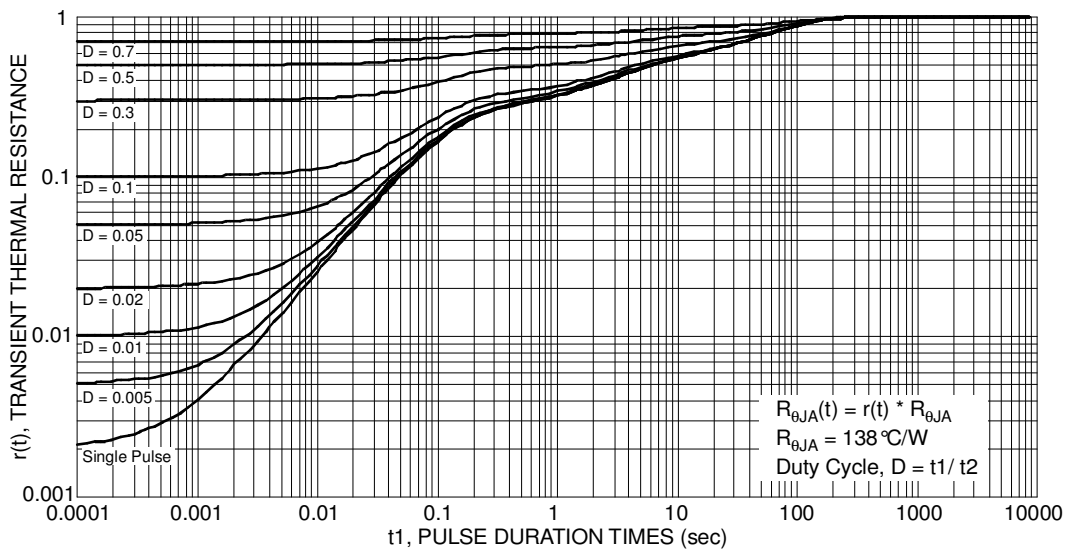
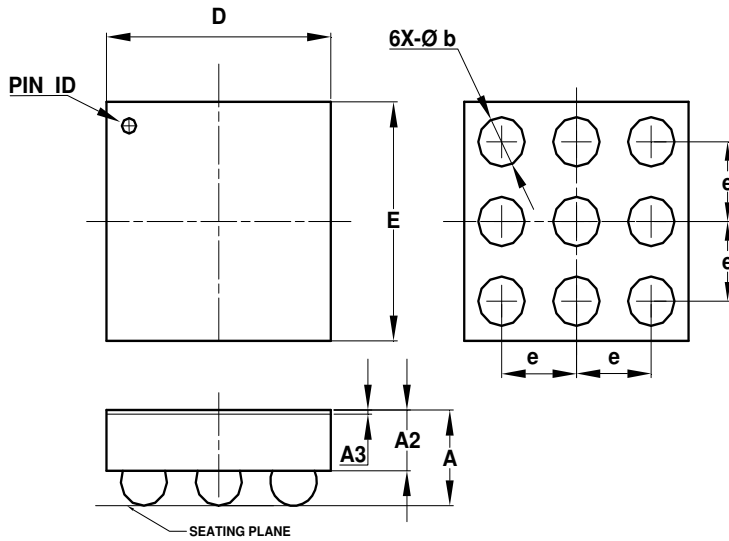


Figure 10 Transient Thermal Resistance

**Package Outline Dimensions**

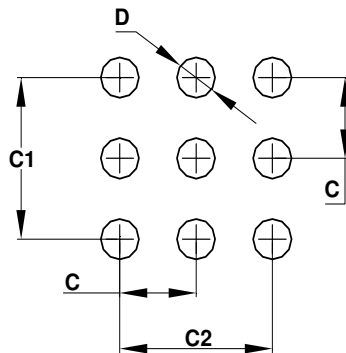
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



U-WLB1515-9			
Dim	Min	Max	Typ
A	-	0.62	-
A2	-	0.36	0.36
A3	0.020	0.030	0.025
b	0.27	0.37	0.32
D	1.47		1.49
E	1.47		1.49
e	-	-	0.50
All Dimensions in mm			

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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