



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

FAN6921MR

Integrated Critical Mode PFC and Quasi-Resonant Current Mode PWM Controller

Features

- Integrated PFC and Flyback Controller
- Critical Mode PFC Controller
- Zero-Current Detection for PFC Stage
- Quasi-Resonant Operation for PWM Stage
- Internal Minimum t_{OFF} 8 μ s for QR PWM Stage
- Internal 10 ms Soft-Start for PWM
- Brownout Protection
- High / Low Line Over-Power Compensation
- Auto-Recovery Over-Current Protection
- Auto-Recovery Open-Loop Protection
- Externally Latch Triggering (RT Pin)
- Adjustable Over-Temperature Latched (RT Pin)
- VDD Pin and Output Voltage OVP (Latched)
- Internal Over-Temperature Shutdown (140°C)

Applications

- AC/DC NB Adapters
- Open-Frame SMPS
- Battery Charger

Description

The highly integrated FAN6921MR combines Power Factor Correction (PFC) controller and Quasi-Resonant PWM controller. Integration provides cost effect design and allows for fewer external components.

For PFC, FAN6921MR uses a controlled on-time technique to provide a regulated DC output voltage and to perform natural power factor correction. With an innovative THD optimizer, FAN6921MR can reduce input current distortion at zero-crossing duration to improve THD performance.

For PWM, FAN6921MR provides several functions to enhance the power system performance: valley detection, green-mode operation, high / low line over power compensation. FAN6921MR provides many protection functions as well: secondary-side open-loop and over-current with auto recovery protection, external latch triggering, adjustable over-temperature protection by RT pin and external NTC resistor, internal over-temperature shutdown, V_{DD} pin OVP, and DET pin over-voltage for output OVP, and brown-in / out for AC input voltage UVP.

The FAN6921MR controller is available in a 16-pin small outline package (SOP).

Ordering Information

| Part Number | OLP Mode | Operating Temperature Range | Package | Packing Method |
|-------------|----------|-----------------------------|------------------------------------|----------------|
| FAN6921MRMY | Recovery | -40°C to +105°C | 16-Pin Small Outline Package (SOP) | Tape & Reel |

Application Diagram

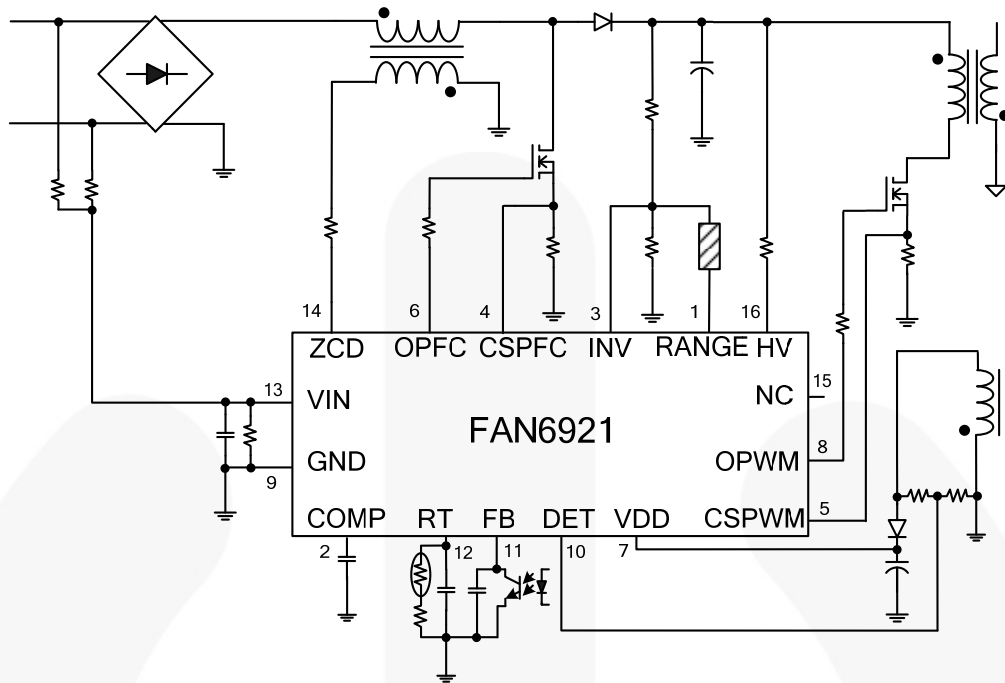


Figure 1. Typical Application

Internal Block Diagram

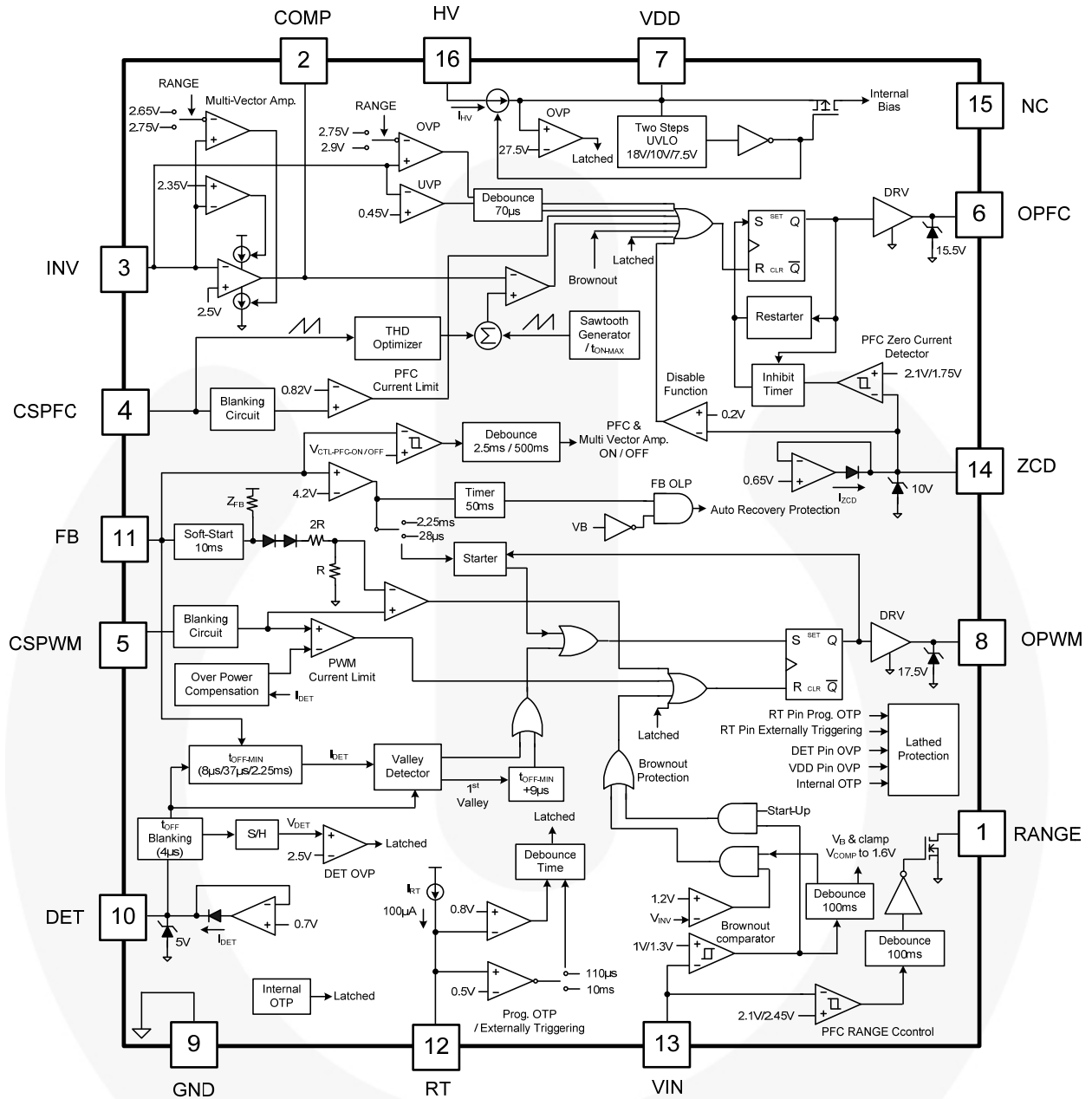


Figure 2. Functional Block Diagram

Marking Information

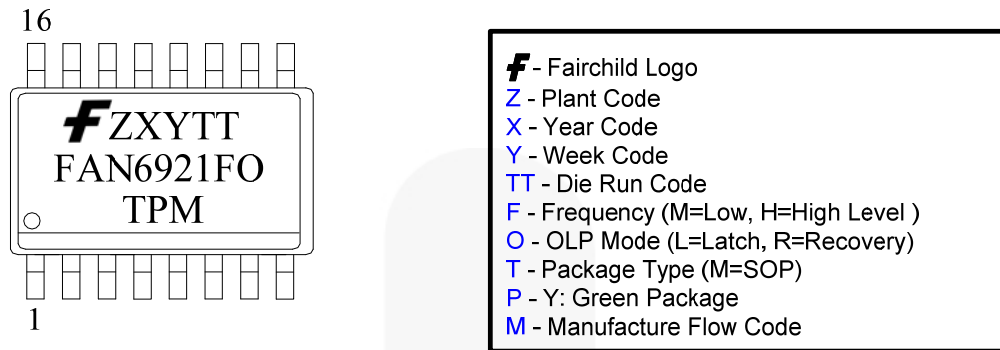


Figure 3. Marking Diagram

Pin Configuration

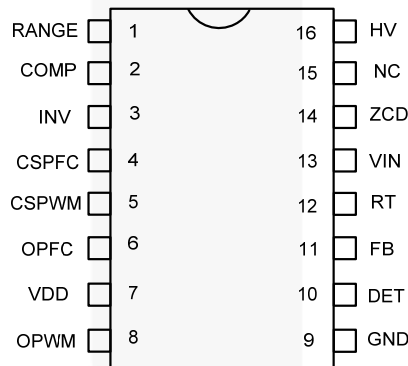


Figure 4. Pin Configuration

Pin Definitions

| Pin # | Name | Description |
|-------|-------|---|
| 1 | RANGE | RANGE pin's impedance changes according to VIN pin voltage level. When the input voltage detected by VIN pin is lower than a threshold voltage, it sets to high impedance; whereas it sets to low impedance if input voltage is high level. |
| 2 | COMP | Output pin of the error amplifier. It is a transconductance type error amplifier for PFC output voltage feedback. Proprietary multi-vector current is built-in to this amplifier. Therefore the compensation for PFC voltage feedback loop allows a simple compensation circuit between this pin and GND. |
| 3 | INV | Inverting input of the error amplifier. This pin is used to receive PFC voltage level by a voltage divider and provides PFC output over- and under-voltage protections. |
| 4 | CSPFC | Input to the PFC over-current protection comparator that provides cycle-by-cycle current limiting protection. When the sensed voltage across the PFC current sensing resistor reaches the internal threshold (0.82 V typical), the PFC switch is turned off to activate cycle-by-cycle current limiting. |
| 5 | CSPWM | Input to the comparator of the PWM over-current protection and performs PWM current-mode control with FB pin voltage. A resistor is used to sense the switching current of PWM switch and the sensing voltage is applied to the CSPWM pin for the cycle-by-cycle current limit, current-mode control, and high / low line over-power compensation according to DET pin source current during PWM t_{ON} time. |

Continued on the following page...

Pin Definitions (Continued)

| Pin # | Name | Description |
|-------|------|--|
| 6 | OPFC | Totem-pole driver output to drive the external power MOSFET. The clamped gate output voltage is 15.5 V. |
| 7 | VDD | Power supply. The threshold voltage for startup and turn-off is 18 V and 7.5 V, respectively. The startup current is less than 30 μ A and the operating current is lower than 10 mA. |
| 8 | OPWM | Totem-pole output generates the PWM signal to drive the external power MOSFET. The clamped gate output voltage is 17.5 V. |
| 9 | GND | The power ground and signal ground. |
| 10 | DET | This pin is connected to an auxiliary winding of the PWM transformer through a resistor divider for the following purposes: <ul style="list-style-type: none"> Producing an offset voltage to compensate the threshold voltage of PWM current limit for providing over-power compensation. The offset is generated in accordance with the input voltage when PWM switch is on. Detecting the valley voltage signal of drain voltage of the PWM switch to achieve the valley voltage switching and minimize the switching loss on PWM switch. Providing output over-voltage protection. A voltage comparator is built-in to the DET pin. The DET pin detects the flat voltage through a voltage divider paralleled with auxiliary winding. This flat voltage is reflected to the secondary winding during PWM inductor discharge time. If output OVP and this flat voltage is higher than 2.5 V, the controller enters latch mode and stops all PFC and PWM switching operation. |
| 11 | FB | Feedback voltage pin. This pin is used to receive output voltage level signal to determine PWM gate duty for regulating output voltage. The FB pin voltage can also activate open-loop, over-load protection, and output-short circuit protection if the FB pin voltage is higher than a threshold of around 4.2 V for more than 50 ms. The input impedance of this pin is a 5 k Ω equivalent resistance. A 1/3 attenuator is connected between the FB pin and the input of the CSPWM/FB comparator. |
| 12 | RT | Adjustable over-temperature protection and external latch triggering. A constant current is flowed out of the RT pin. When RT pin voltage is lower than 0.8 V (typical), latch mode protection is activated and stops all PFC and PWM switching operation until the AC plug is removed. |
| 13 | VIN | Line-voltage detection for brown-in / out protections. This pin can receive the AC input voltage level through a voltage divider. The voltage level of the VIN pin is not only used to control RANGE pin's status, but it can also perform brown-in / out protection for AC input voltage UVP. |
| 14 | ZCD | Zero-current detection for the PFC stage. This pin is connected to an auxiliary winding coupled to PFC inductor winding to detect the ZCD voltage signal once the PFC inductor current discharges to zero. When the ZCD voltage signal is detected, the controller starts a new PFC switching cycle. When the ZCD pin voltage is pulled to under 0.2 V (typical), it disables the PFC stage and the controller stops PFC switching. This can be realized with an external circuit if disabling the PFC stage is desired. |
| 15 | NC | No connection |
| 16 | HV | High-voltage startup. HV pin is connected to the AC line voltage through a resistor (100 k Ω typical) for providing a high charging current to V _{DD} capacitor. |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|---|------|------|------|
| V _{DD} | DC Supply Voltage | | 30 | V |
| V _{HV} | HV | | 500 | V |
| V _H | OPFC, OPWM | -0.3 | 25.0 | V |
| V _L | Others (INV, COMP, CSPFC, DET, FB, CSPWM, RT) | -0.3 | 7.0 | V |
| V _{ZCD} | Input Voltage to ZCD Pin | -0.3 | 12.0 | V |
| P _D | Power Dissipation | | 800 | mW |
| θ_{JA} | Thermal Resistance (Junction-to-Air) | | 104 | °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | | 41 | °C/W |
| T _J | Operating Junction Temperature | -40 | +150 | °C |
| T _{STG} | Storage Temperature Range | -55 | +150 | °C |
| T _L | Lead Temperature (Soldering 10 Seconds) | | +260 | °C |
| ESD | Human Body Model, JESD22-A114 (All Pins Except HV Pin) ⁽³⁾ | | 4500 | V |
| | Charged Device Model, JESD22-C101 (All Pins Except HV Pin) ⁽³⁾ | | 1250 | |

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.
3. All pins including HV pin: CDM=750 V, HBM 1000 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|----------------|-------------------------------|------|------|------|
| T _A | Operating Ambient Temperature | -40 | +105 | °C |

Electrical Characteristics

$V_{DD}=15\text{ V}$, $T_A=-40^{\circ}\text{C}\sim 105^{\circ}\text{C}$ ($T_A=T_J$), unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--|---|--|-------------------------------|-------------------------------|-------------------------------|---------------|
| V_{DD} Section | | | | | | |
| V_{OP} | Continuously Operating Voltage | | | | 25 | V |
| V_{DD-ON} | Turn-On Threshold Voltage | | 16.5 | 18.0 | 19.5 | V |
| $V_{DD-PWM-OFF}$ | PWM Off Threshold Voltage | | 9 | 10 | 11 | V |
| V_{DD-OFF} | Turn-Off Threshold Voltage | | 6.5 | 7.5 | 8.5 | V |
| I_{DD-ST} | Startup Current | $V_{DD}=V_{DD-ON} - 0.16\text{ V}$, Gate Open | | 20 | 30 | μA |
| I_{DD-OP} | Operating Current | $V_{DD}=15\text{ V}$, OPFC, OPWM=100 kHz, C_{L-PFC} , $C_{L-PWM}=2\text{ nF}$ | | | 10 | mA |
| $I_{DD-GREEN}$ | Green-Mode Operating Supply Current (Average) | $V_{DD}=15\text{ V}$, OPWM=450 Hz, $C_{L-PWM}=2\text{ nF}$ | | 5.5 | | mA |
| $I_{DD-PWM-OFF}$ | Operating Current at PWM-Off Phase | $V_{DD}=V_{DD-PWM-OFF} - 0.5\text{ V}$ | 70 | 120 | 170 | μA |
| V_{DD-OVP} | V_{DD} Over-Voltage Protection (Latch-Off) | | 26.5 | 27.5 | 28.5 | V |
| $t_{VDD-OVP}$ | V_{DD} OVP Debounce Time | | 100 | 150 | 200 | μs |
| $I_{DD-LATCH}$ | V_{DD} Over-Voltage Protection Latch-Up Holding Current | $V_{DD}=7.5\text{ V}$ | | 120 | | μA |
| HV Startup Current Source Section | | | | | | |
| V_{HV-MIN} | Minimum Startup Voltage on HV Pin | | | | 50 | V |
| I_{HV} | Supply Current Drawn from HV Pin | $V_{AC}=90\text{ V}$ ($V_{DC}=120\text{ V}$), $V_{DD}=0\text{ V}$ | 1.3 | | | mA |
| | | HV=500 V, $V_{DD}=V_{DD-OFF} + 1\text{ V}$ | | 1 | | μA |
| V_{IN} and RANGE Section | | | | | | |
| $V_{VIN-UVP}$ | Threshold Voltage for AC Input Under-Voltage Protection | | 0.95 | 1.00 | 1.05 | V |
| $V_{VIN-RE-UVP}$ | Under-Voltage Protection Reset Voltage (for Startup) | | $V_{VIN-UVP} + 0.25\text{ V}$ | $V_{VIN-UVP} + 0.30\text{ V}$ | $V_{VIN-UVP} + 0.35\text{ V}$ | V |
| $t_{VIN-UVP}$ | Under-Voltage Protection Debounce Time (No Need at Startup and Hiccup Mode) | | 70 | 100 | 130 | ms |
| $V_{VIN-RANGE-H}$ | High V_{VIN} Threshold for RANGE Comparator | | 2.40 | 2.45 | 2.50 | V |
| $V_{VIN-RANGE-L}$ | Low V_{VIN} Threshold for RANGE Comparator | | 2.05 | 2.10 | 2.15 | V |
| t_{RANGE} | Range-Enable/ Disable Debounce Time | | 70 | 100 | 130 | ms |
| $V_{RANGE-OL}$ | Output Low Voltage of RANGE Pin | $I_O=1\text{ mA}$ | | | 0.5 | V |
| $I_{RANGE-OH}$ | Output High Leakage Current of RANGE Pin | RANGE=5 V | | | 50 | nA |
| $t_{ON-MAX-PFC}$ | PFC Maximum On Time | $R_{MOT}=24\text{ k}\Omega$ | 22 | 25 | 28 | μs |

Continued on the following page...

Electrical Characteristics (Continued)

$V_{DD}=15\text{ V}$, $T_A=-40^\circ\text{C} \sim 105^\circ\text{C}$ ($T_A=T_J$), unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--|---|--|-------|-------|-------|-----------------|
| PFC Stage | | | | | | |
| Voltage Error Amplifier Section | | | | | | |
| G_m | Transconductance ⁽⁴⁾ | | 100 | 125 | 150 | μmho |
| V_{REF} | Feedback Comparator Reference Voltage | | 2.465 | 2.500 | 2.535 | V |
| V_{INV-H} | Clamp High Feedback Voltage | RANGE=Open | 2.70 | 2.75 | 2.80 | V |
| | | RANGE=Ground | 2.60 | 2.65 | 2.70 | |
| V_{RATIO} | Clamp High Output Voltage Ratio ⁽⁴⁾ | V_{INVH} / V_{REF} , RANGE=Open | 1.06 | | 1.14 | V/V |
| | | V_{INVH} / V_{REF} , RANGE=Ground | 1.04 | | 1.08 | |
| V_{INV-L} | Clamp Low Feedback Voltage | | 2.25 | 2.35 | 2.45 | V |
| $V_{INV-OVP}$ | Over-Voltage Protection for INV Input | RANGE=Open | | 2.90 | 2.95 | V |
| | | RANGE=Ground | | 2.75 | 2.80 | |
| $t_{INV-OVP}$ | Over-Voltage Protection Debounce Time | | 50 | 70 | 90 | μs |
| $V_{INV-UVP}$ | Under-Voltage Protection for INV Input | | 0.35 | 0.45 | 0.55 | V |
| $t_{INV-UVP}$ | Under-Voltage Protection Debounce Time | | 50 | 70 | 90 | μs |
| V_{INV-BO} | PWM and PFC Off Threshold for Brownout Protection | | 1.15 | 1.20 | 1.25 | V |
| $V_{COMP-BO}$ | Limited Voltage on COMP Pin for Brownout Protection | | 1.55 | 1.60 | 1.65 | V |
| V_{COMP} | Comparator Output High Voltage | | 4.8 | | 6.0 | V |
| V_{OZ} | Zero Duty Cycle Voltage on COMP Pin | | 1.10 | 1.25 | 1.40 | V |
| I_{COMP} | Comparator Output Source Current | $V_{INV}=2.3\text{ V}$, $V_{COMP}=1.5\text{ V}$ | 15 | 30 | 45 | μA |
| | | $V_{INV}=1.5\text{ V}$ | 0.50 | 0.75 | 1.00 | mA |
| | Comparator Output Sink Current | RANGE=Open, $V_{INV}=2.75\text{ V}$, $V_{COMP}=5\text{ V}$ | 20 | 30 | 40 | μA |
| | | RANGE=Ground, $V_{INV}=2.65\text{ V}$, $V_{COMP}=5\text{ V}$ | 20 | 30 | 40 | |
| PFC Current Sense Section | | | | | | |
| V_{CSPFC} | Threshold Voltage for Peak Current Cycle-by-Cycle Limit | $V_{COMP}=5\text{ V}$ | | 0.82 | | V |
| t_{PD} | Propagation Delay | | | 110 | 200 | ns |
| t_{BNK} | Leading-Edge Blanking Time | | 110 | 180 | 250 | ns |
| A_V | CSPFC Compensation Ratio for THD | | 0.90 | 0.95 | 1.00 | V/V |

Continued on the following page...

Electrical Characteristics (Continued)

$V_{DD}=15\text{ V}$, $T_A=-40^\circ\text{C} \sim 105^\circ\text{C}$ ($T_A=T_J$), unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|--|--|------|------|------|---------------|
| PFC Output Section | | | | | | |
| V_Z | PFC Gate Output Clamping Voltage | $V_{DD}=25\text{ V}$ | 14.0 | 15.5 | 17.0 | V |
| V_{OL} | PFC Gate Output Voltage Low | $V_{DD}=15\text{ V}$, $I_O=100\text{ mA}$ | | | 1.5 | V |
| V_{OH} | PFC Gate Output Voltage High | $V_{DD}=15\text{ V}$, $I_O=100\text{ mA}$ | 8 | | | V |
| t_R | PFC Gate Output Rising Time | $V_{DD}=12\text{ V}$, $C_L=3\text{ nF}$, 20~80% | 30 | 65 | 100 | ns |
| t_F | PFC Gate Output Falling Time | $V_{DD}=12\text{ V}$, $C_L=3\text{ nF}$, 80~20% | 30 | 50 | 70 | ns |
| PFC Zero Current Detection Section | | | | | | |
| V_{ZCD} | Input Threshold Voltage Rising Edge | V_{ZCD} Increasing | 1.9 | 2.1 | 2.3 | V |
| $V_{ZCD-HYST}$ | Threshold Voltage Hysteresis | V_{ZCD} Decreasing | 0.25 | 0.35 | 0.45 | V |
| $V_{ZCD-HIGH}$ | Upper Clamp Voltage | $I_{ZCD}=3\text{ mA}$ | 8 | 10 | | V |
| $V_{ZCD-LOW}$ | Lower Clamp Voltage | | 0.40 | 0.65 | 0.90 | V |
| $V_{ZCD-SSC}$ | Starting Source Current Threshold Voltage | | 1.3 | 1.4 | 1.5 | V |
| t_{DELAY} | Maximum Delay from ZCD to Output Turn-On | $V_{COMP}=5\text{ V}$, $f_S=60\text{ kHz}$ | 100 | | 200 | ns |
| $t_{RESTART-PFC}$ | Restart Time | | 300 | 500 | 700 | μs |
| t_{INHIB} | Inhibit Time (Maximum Switching Frequency Limit) | $V_{COMP}=5\text{ V}$ | 1.5 | 2.5 | 3.5 | μs |
| $V_{ZCD-DIS}$ | PFC Enable/ Disable Function Threshold Voltage | | 0.15 | 0.2 | 0.25 | V |
| $t_{ZCD-DIS}$ | PFC Enable/ Disable Function Debounce Time | $V_{ZCD}=100\text{ mV}$ | 100 | 150 | 200 | μs |

Continued on the following page...

Electrical Characteristics (Continued)V_{DD}=15 V, T_A=-40°C ~105°C (T_A=T_J), unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|--|--|--------|--------|--------|-------|
| PWM STAGE | | | | | | |
| Feedback Input Section | | | | | | |
| A _V | Input-Voltage to Current Sense Attenuation ⁽⁴⁾ | $A_V = \Delta V_{CSPWM} / \Delta V_{FB}$, 0 < V _{CSPWM} < 0.9 | 1/2.75 | 1/3.00 | 1/3.25 | V/V |
| Z _{FB} | Input Impedance ⁽⁴⁾ | FB > V _G | 3 | 5 | 7 | kΩ |
| I _{OZ} | Bias Current | FB = V _{OZ} | | 1.2 | 2.0 | mA |
| V _{OZ} | Zero Duty-cycle Input Voltage | | 0.7 | 0.9 | 1.1 | V |
| V _{FB-OLP} | Open-Loop Protection Threshold Voltage | | 3.9 | 4.2 | 4.5 | V |
| t _{FB-OLP} | The Debounce Time for Open Loop Protection | | 40 | 50 | 60 | ms |
| t _{FB-SS} | Internal Soft-Start Time ⁽⁴⁾ | V _{FB} =0 V~3.6 V | 8.5 | 9.5 | 10.5 | ms |
| DET Pin OVP and Valley Detection Section | | | | | | |
| V _{DET-OVP} | Comparator Reference Voltage | | 2.45 | 2.50 | 2.55 | V |
| A _V | Open-Loop Gain ⁽⁴⁾ | | | 60 | | dB |
| BW | Gain Bandwidth ⁽⁴⁾ | | | 1 | | MHz |
| t _{DET-OVP} | Output OVP(Latched) Debounce Time | | 100 | 150 | 200 | μs |
| I _{DET-SOURCE} | Maximum Source Current | V _{DET} =0 V | | | 1 | mA |
| V _{DET-HIGH} | Upper Clamp Voltage | I _{DET} =-1 mA | | | 5 | V |
| V _{DET-LOW} | Lower Clamp Voltage | I _{DET} =1 mA | 0.5 | 0.7 | 0.9 | V |
| t _{VALLEY-DELAY} | Delay Time from Valley Signal Detected to Output Turn-on ⁽⁴⁾ | | 150 | 200 | 250 | ns |
| t _{OFF-BNK} | Leading-Edge Blanking Time for DET-OVP (2.5 V) and Valley Signal when PWM MOS Turns Off ⁽⁴⁾ | | 3 | 4 | 5 | μs |
| t _{TIME-OUT} | Time-Out After t _{OFF-MIN} | | 8 | 9 | 10 | μs |
| PWM Oscillator Section | | | | | | |
| t _{ON-MAX-PWM} | Maximum On Time | | 38 | 45 | 52 | μs |
| t _{OFF-MIN} | Minimum Off Time | V _{FB} ≥ V _N , T _A =25°C | 7 | 8 | 9 | μs |
| | | V _{FB} =V _G | 32 | 37 | 42 | |
| V _N | Beginning of Green-On Mode at FB Voltage Level | | 1.95 | 2.10 | 2.25 | V |
| V _G | Beginning of Green-Off Mode at FB Voltage Level | | 1.00 | 1.15 | 1.30 | V |
| ΔV _G | Hysteresis for Beginning of Green-Off Mode at FB Voltage Level | | | 0.1 | | V |

Continued on the following page...

Electrical Characteristics (Continued)

$V_{DD}=15\text{ V}$, $T_A=-40^\circ\text{C}\sim 105^\circ\text{C}$ ($T_A=T_J$), unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------------------|--|--|------|------|------|---------------|
| $V_{CTL-PFC-OFF}$ | Threshold Voltage on FB Pin for PFC Enable → Disable | RANGE Pin Internally Open | 1.70 | 1.75 | 1.80 | V |
| | | RANGE Pin Internally Ground | 1.60 | 1.65 | 1.70 | |
| $V_{CTL-PFC-ON}$ | Threshold Voltage on FB Pin for PFC Disable → Enable | RANGE Pin Internally Open | 1.85 | 1.90 | 1.95 | V |
| | | RANGE Pin Internally Ground | 1.70 | 1.75 | 1.80 | |
| $t_{PFC-OFF}$ | PFC Disable Debounce Time | PFC Enable → Disable | 400 | 500 | 600 | ms |
| t_{PFC-ON} | PFC Enable Debounce Time | PFC Disable → Enable | 2.0 | 2.5 | 3.0 | ms |
| $t_{STARTER-PWM}$ | Start Timer (Time-Out Timer) | $V_{FB} < V_G$ | 1.85 | 2.25 | 2.65 | ms |
| | | $V_{FB} > V_{FB-OLP}$ | 22 | 28 | 34 | μs |
| PWM Output Section | | | | | | |
| V_{CLAMP} | PWM Gate Output Clamping Voltage | $V_{DD}=25\text{ V}$ | 16.0 | 17.5 | 19.0 | V |
| V_{OL} | PWM Gate Output Voltage Low | $V_{DD}=15\text{ V}$, $I_O=100\text{ mA}$ | | | 1.5 | V |
| V_{OH} | PWM Gate Output Voltage High | $V_{DD}=15\text{ V}$, $I_O=100\text{ mA}$ | 8 | | | V |
| t_R | PWM Gate Output Rising Time | $C_L=3\text{ nF}$, $V_{DD}=12\text{ V}$, 20~80% | | 80 | 110 | ns |
| t_F | PWM Gate Output Falling Time | $C_L=3\text{ nF}$, $V_{DD}=12\text{ V}$, 20~80% | | 40 | 70 | ns |
| Current Sense Section | | | | | | |
| t_{PD} | Delay to Output | | | 150 | 200 | ns |
| V_{LIMIT} | The Limit Voltage on CSPWM Pin for Over Power Compensation | $I_{DET} < 75\text{ }\mu\text{A}$, $T_A=25^\circ\text{C}$ | 0.81 | 0.84 | 0.87 | V |
| | | $I_{DET}=185\text{ }\mu\text{A}$, $T_A=25^\circ\text{C}$ | 0.69 | 0.72 | 0.75 | |
| | | $I_{DET}=350\text{ }\mu\text{A}$, $T_A=25^\circ\text{C}$ | 0.55 | 0.58 | 0.61 | |
| | | $I_{DET}=550\text{ }\mu\text{A}$, $T_A=25^\circ\text{C}$ | 0.34 | 0.40 | 0.46 | |
| V_{SLOPE} | Slope Compensation ⁽⁴⁾ | $t_{ON}=45\text{ }\mu\text{s}$, RANGE=Open | 0.25 | 0.30 | 0.35 | V |
| | | $t_{ON}=0\text{ }\mu\text{s}$ | 0.05 | 0.10 | 0.15 | |
| t_{ON-BNK} | Leading-Edge Blanking Time | | | 300 | | ns |
| $V_{CS-FLOATING}$ | CSPWM Pin Floating V_{CSPWM} Clamped High Voltage | CSPWM Pin Floating | 4.5 | | 5.0 | V |
| t_{CS-H} | The Delay Time once CSPWM Pin Floating | CSPWM Pin Floating | | 150 | | μs |

Continued on the following page...

Electrical Characteristics (Continued)

$V_{DD}=15V$, $T_A=-40^{\circ}C\sim 105^{\circ}C$ ($T_A=T_J$), unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|--|-----------------------------|-----------------------|-----------------------|-----------------------|-------------|
| RT Pin Over-Temperature Protection Section | | | | | | |
| T_{OTP} | Internal Threshold Temperature for OTP ⁽⁴⁾ | | 125 | 140 | 155 | $^{\circ}C$ |
| $T_{OTP-HYST}$ | Hysteresis Temperature for Internal OTP ⁽⁴⁾ | | | 30 | | $^{\circ}C$ |
| I_{RT} | Internal Source Current of RT Pin | | 90 | 100 | 110 | μA |
| $V_{RT-LATCH}$ | Latch-Mode Triggering Voltage | | 0.75 | 0.80 | 0.85 | V |
| $V_{RT-RE-LATCH}$ | Latch-Mode Release Voltage | | $V_{RT-LATCH} + 0.15$ | $V_{RT-LATCH} + 0.20$ | $V_{RT-LATCH} + 0.25$ | V |
| $V_{RT-OTP-LEVEL}$ | Threshold Voltage for Two-level Debounce Time | | 0.45 | 0.50 | 0.55 | V |
| $t_{RT-OTP-H}$ | Debounce Time for OTP | | | 10 | | ms |
| $t_{RT-OTP-L}$ | Debounce Time for Externally Triggering | $V_{RT} < V_{RT-OTP-LEVEL}$ | 70 | 110 | 150 | μs |

Note:

- Guaranteed by design.

Typical Performance Characteristics

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

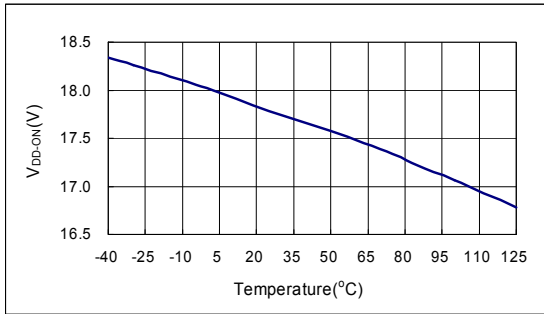


Figure 5. Turn-On Threshold Voltage

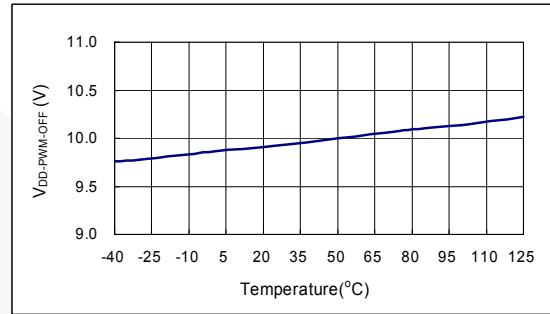


Figure 6. PWM Off Threshold Voltage

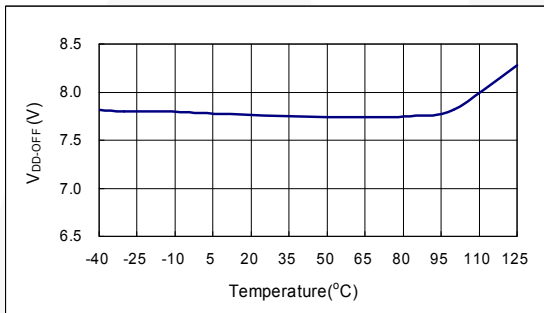


Figure 7. Turn-Off Threshold Voltage

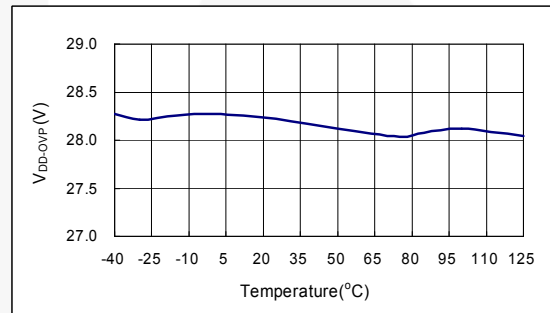


Figure 8. $V_{D_{on}}$ Over-Voltage Protection Threshold

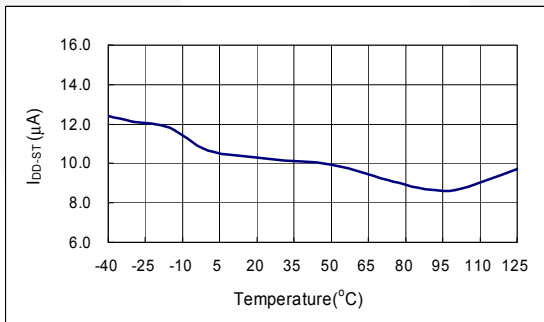


Figure 9. Startup Current

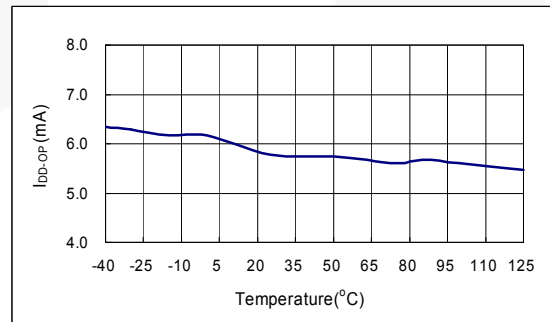


Figure 10. Operating Current

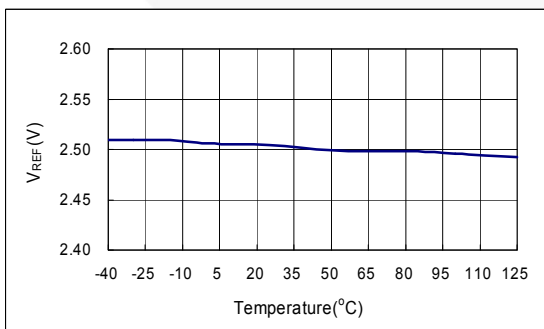


Figure 11. PFC Output Feedback Reference Voltage

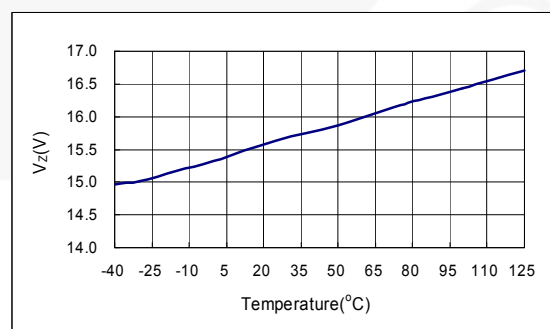


Figure 12. PFC Gate Output Clamping Voltage

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

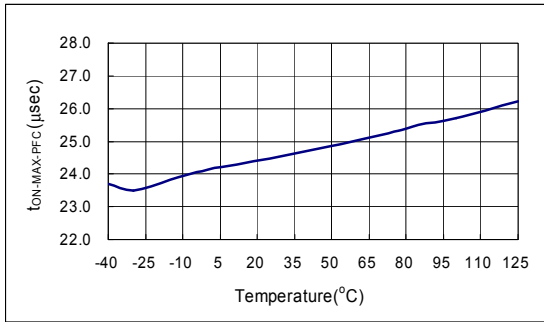


Figure 13. PFC Maximum On-Time

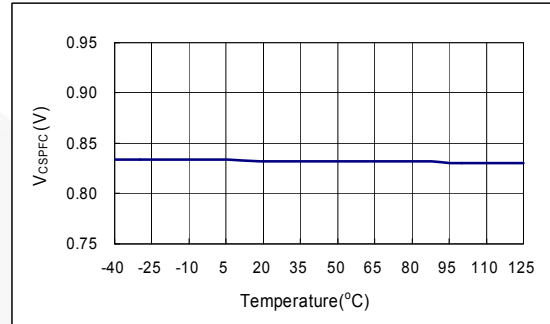


Figure 14. PFC Peak Current Limit Voltage

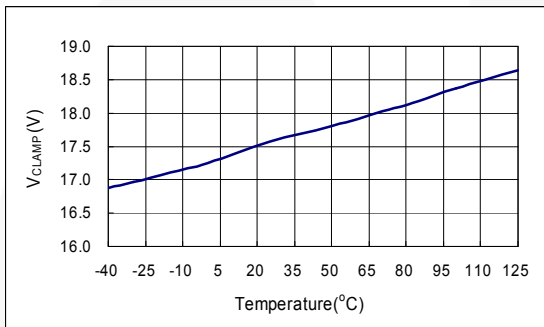


Figure 15. PWM Gate Output Clamping Voltage

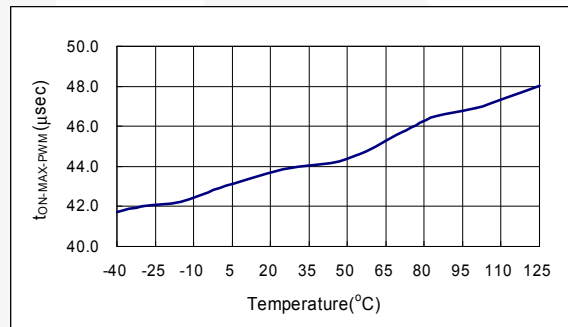


Figure 16. PWM Maximum On-Time

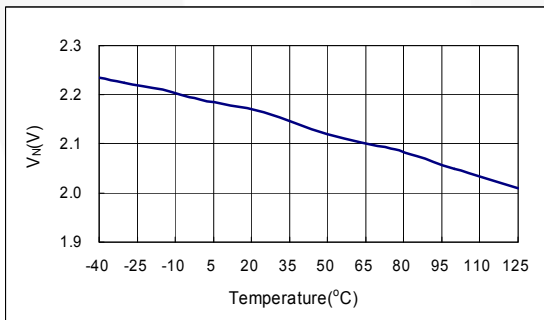


Figure 17. Beginning of Green-On Mode at V_{FB}

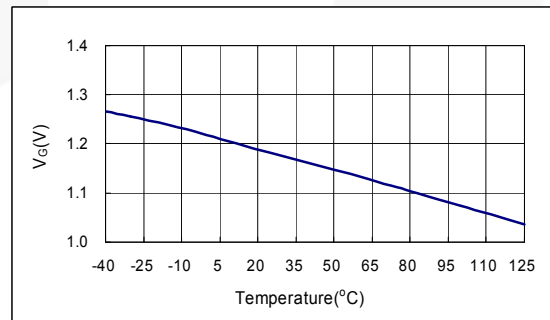


Figure 18. Beginning of Green-Off Mode at V_{FB}

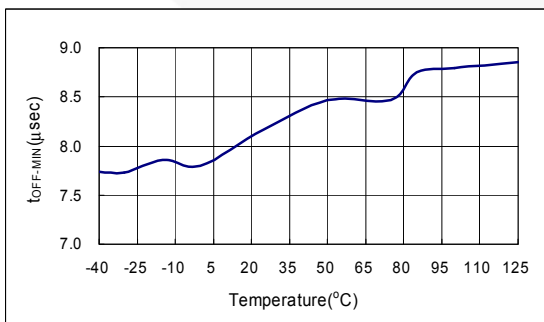


Figure 19. PWM Minimum Off-Time for $V_{FB} > V_N$

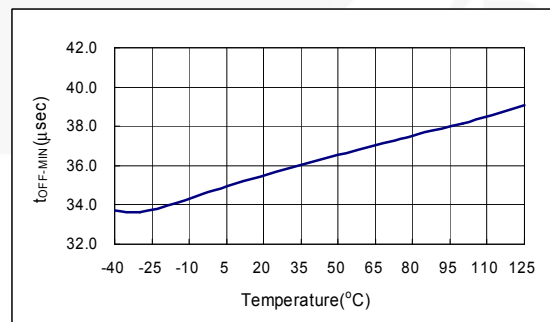


Figure 20. PWM Minimum Off-Time for $V_{FB} = V_G$

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

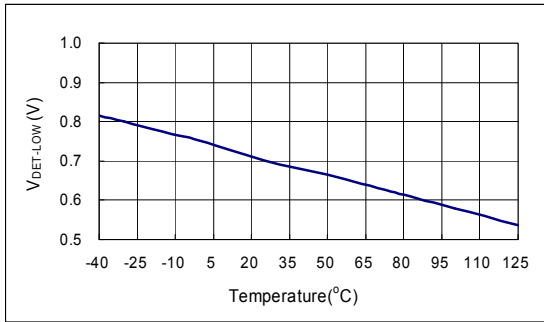


Figure 21. Lower Clamp Voltage of DET Pin

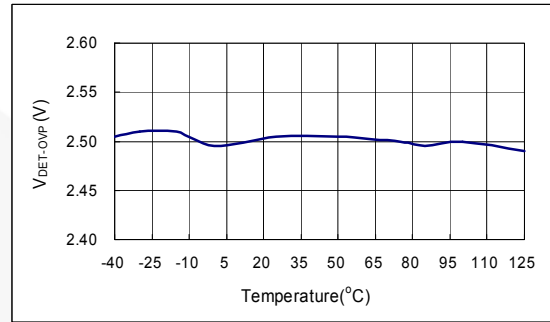


Figure 22. Reference Voltage for Output Over-Voltage Protection of DET Pin

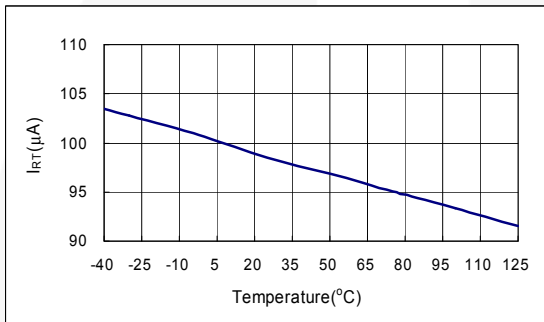


Figure 23. Internal Source Current of RT Pin

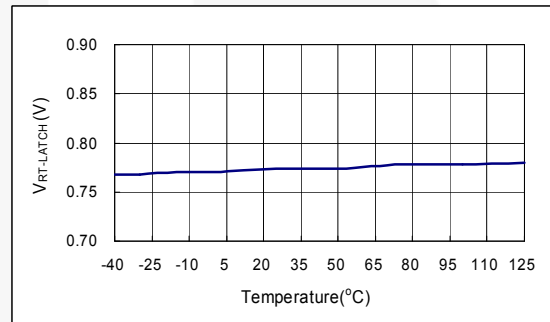


Figure 24. Over Temperature Protection Threshold Voltage of RT Pin

Functional Description

PFC Stage

Multi-Vector Error Amplifier and THD Optimizer

For better dynamic performance, faster transient response, and precise clamping on PFC output, FAN6921MR uses a trans-conductance type amplifier with proprietary innovative multi-vector error amplifier. The schematic diagram of this amplifier is shown in Figure 25. The PFC output voltage is detected from the INV pin by an external resistor divider circuit that consists of R_1 and R_2 . When PFC output variation voltage reaches 6% over or under the reference voltage 2.5 V, the multi-vector error amplifier adjusts its output sink or source current to increase the loop response to simplify the compensated circuit.

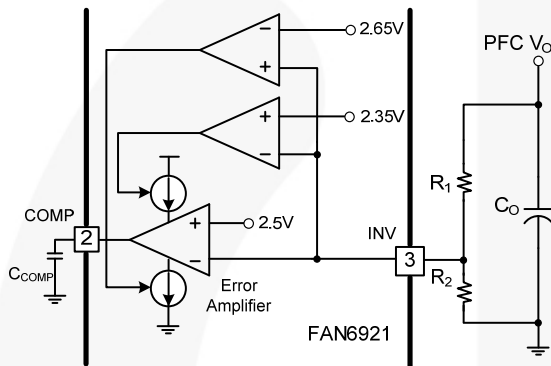


Figure 25. Multi-Vector Error Amplifier

The feedback voltage signal on the INV pin is compared with reference voltage 2.5 V, which makes the error amplifier source or sink current to charge or discharge its output capacitor C_{COMP} . The COMP voltage is compared with the internally generated sawtooth waveform to determine the on-time of PFC gate. Normally, with lower feedback loop bandwidth, the variation of the PFC gate on-time should be very small and almost constant within one input AC cycle. However, the power factor correction circuit operating at light load condition has a defect, zero crossing distortion; which distorts input current and makes the system's Total Harmonic Distortion (THD) worse. To improve the result of THD at light load condition, especially at high input voltage, an innovative THD Optimizer is inserted by sampling the voltage across the current-sense resistor. This sampling voltage on current-sense resistor is added into the sawtooth waveform to modulate the on-time of PFC gate, so it is not constant on-time within a half AC cycle. The method of operation block between THD Optimizer and PWM are shown in Figure 26. After THD Optimizer processes, around the valley of AC input voltage, the compensated on-time becomes wider than the original. The PFC on-time, which is around the peak voltage, is narrowed by the THD Optimizer. The timing sequences of the PFC MOS and the shape of the inductor current are shown in Figure 27. Figure 28 shows the difference between calculated fixed on-time mechanism and fixed on-time with THD Optimizer during a half AC cycle.

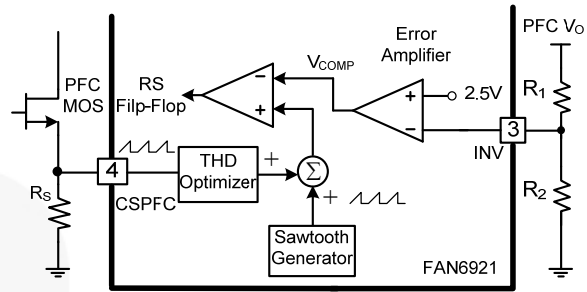


Figure 26. Multi-Vector Error Amplifier with THD Optimizer

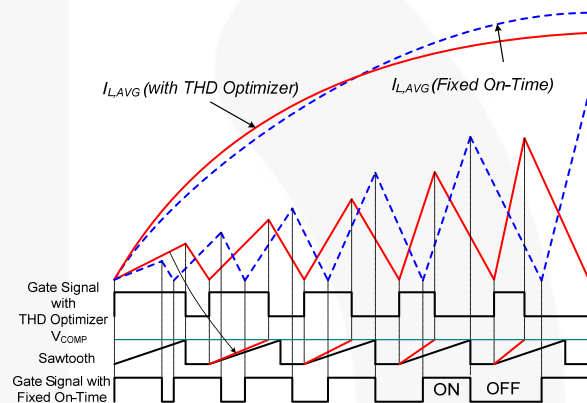


Figure 27. Operation Waveforms of Fixed On-Time with and without THD Optimizer

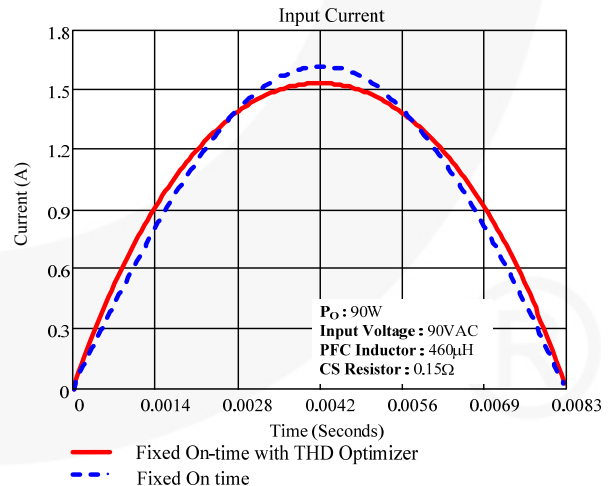


Figure 28. Calculated Waveforms of Fixed On-Time with and without THD Optimizer During a Half AC Cycle

RANGE Pin

A built-in low voltage MOSFET can be turned on or off according to V_{VIN} voltage level. The drain pin of this internal MOSFET is connected to the RANGE pin. Figure 29 shows the status curve of V_{VIN} voltage level and RANGE impedance (open or ground).

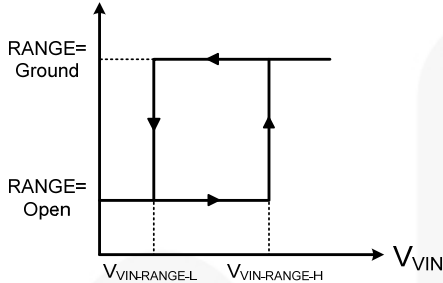


Figure 29. Hysteresis Behavior between RANGE Pin and VIN Pin Voltage

Zero Current Detection (ZCD Pin)

Figure 30 shows the internal block of zero-current detection. The detection function is performed by sensing the information on an auxiliary winding of the PFC inductor. Referring to Figure 31, when PFC MOS is off, the stored energy of the PFC inductor starts to release to the output load. Then the drain voltage of PFC MOS starts to decrease since the PFC inductor resonates with parasitic capacitance. Once the ZCD pin voltage is lower than the triggering voltage (1.75V typical), the PFC gate signal is sent again to start a new switching cycle.

If PFC operation needs to be shut down due to abnormal condition, it is suggested to pull the ZCD pin LOW, voltage under 0.2 V (typical), to activate the PFC disable function to stop PFC switching operation.

For preventing excessive high switching frequency at light load, a built-in inhibit timer is used to limit the minimum t_{OFF} time. Even if the ZCD signal has been detected, the PFC gate signal still would not be sent during the inhibit time (2.5 μ s typical).

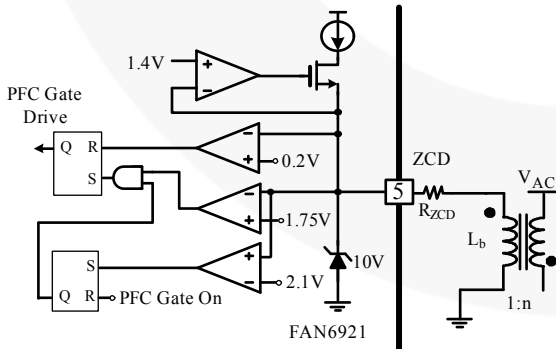


Figure 30. Internal Block of the Zero-Current Detection

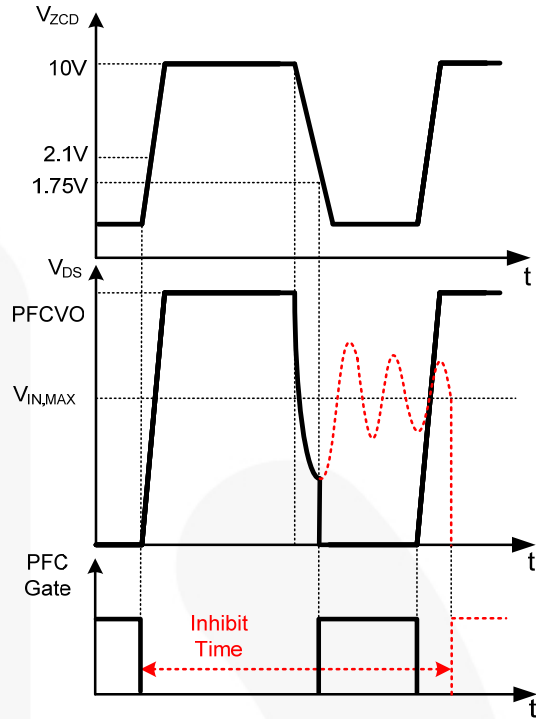


Figure 31. Operation Waveforms of PFC Zero-Current Detection

Protection for PFC Stage

PFC Output Voltage UVP and OVP (INV Pin)

FAN6921MR provides several kinds of protection for PFC stage. PFC output over- and under-voltage are essential for PFC stage. Both are detected and determined by INV pin voltage, as shown in Figure 32. When INV pin voltage is over 2.75 V or under 0.45 V, due to overshoot or abnormal conditions and lasts for a de-bounce time around 70 μ s, the OVP or UVP circuit is activated to stop PFC switching operation immediately.

The INV pin is not only used to receive and regulate PFC output voltage, but can also perform PFC output OVP/ UVP protection. For failure-mode test, this pin can shut down PFC switching if pin floating occurs.

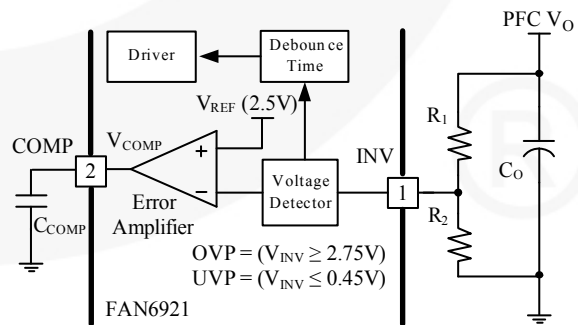


Figure 32. Internal Block of PFC Over-and Under-Voltage Protection

PFC Peak Current Limiting (CSPFC pin)

During PFC stage switching operation, the PFC switch current is detected by current-sense resistor on the CSPFC pin and the detected voltage on this resistor is delivered to input terminal of a comparator and compared with a threshold voltage 0.82 V (typical). Once the CSPFC pin voltage is higher than the threshold voltage, PFC gate is turned off immediately.

The PFC peak switching current is adjustable by the current-sense resistor. Figure 33 shows the measured waveform of PFC gate and CSPFC pin voltage.

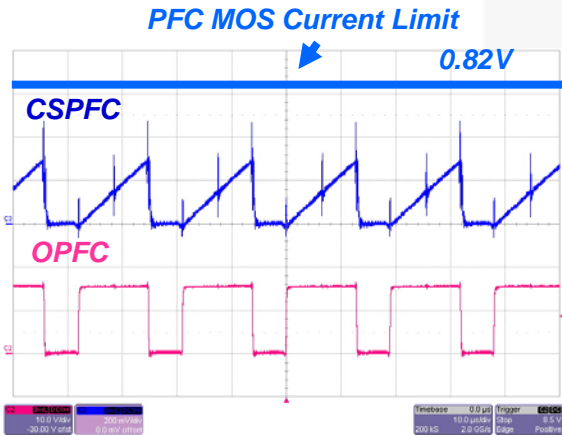


Figure 33. Cycle-by-Cycle Current Limiting

Brown-In / Out Protection (VIN Pin)

With AC voltage detection, FAN6921MR can perform brown-in/ out protection (AC voltage UVP). Figure 34 shows the key operation waveforms of brown-in / out protection. Both use the VIN pin to detect AC input voltage level and the VIN pin is connected to AC input by a resistor divider (refer to Figure 1); therefore, the V_{VIN} voltage is proportional to the AC input voltage. When the AC voltage drops, and V_{VIN} voltage is lower than 1 V for 100 ms, the UVP protection is activated and the COMP pin voltage is clamped to around 1.6 V. Because PFC gate duty is determined by comparing sawtooth waveform and COMP pin voltage, lower COMP voltage results in narrow PFC on-time, so that the energy converged is limited and the PFC output voltage decreases. When INV pin is lower than 1.2 V, FAN6921MR stops all PFC and PWM switching operation immediately until V_{DD} voltage drops to turn-off voltage then raises to turn-on voltage again (UVLO).

When the brownout protection is activated, all switching operation is turned off, V_{DD} voltage enters hiccup mode up and down continuously. Until V_{VIN} voltage is higher than 1.3 V (typical) and V_{DD} reaches turn-on voltage again, the PWM and PFC gate is sent out.

The measured waveforms of brown-in / out protection are shown in Figure 35.

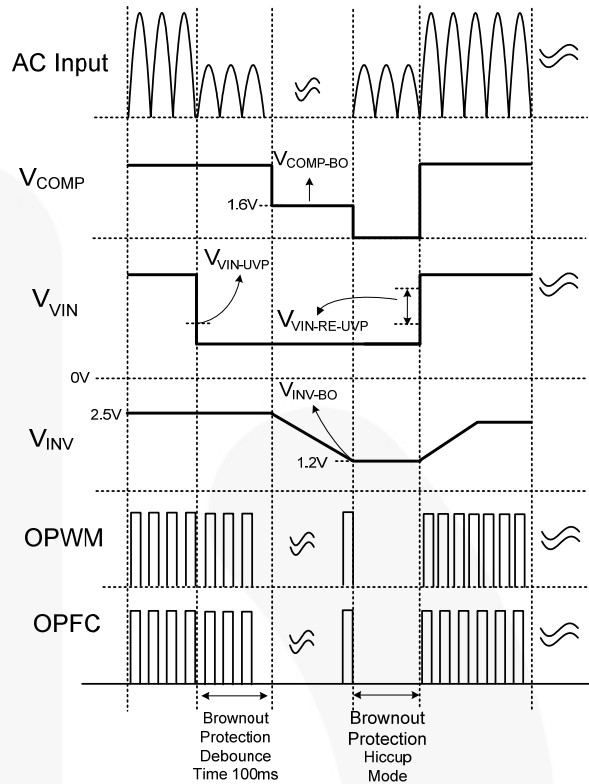


Figure 34. Operation Waveforms of Brown-In/ Out Protection

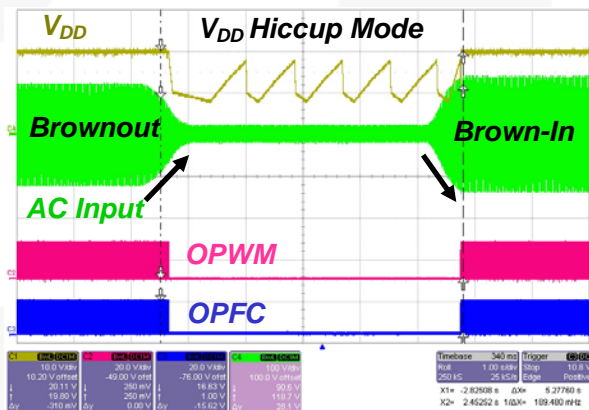


Figure 35. Measured Waveform of Brown-In/ Out Protection (Adapter Application)

PWM Stage

HV Startup and Operating Current (HV Pin)

The HV pin is connected to AC line through a resistor (refer to Figure 1). With a built-in high-voltage startup circuit, when AC voltage is applied to power system, FAN6921MR provides a high current to charge external V_{DD} capacitor to speed up controller's startup time and build up normal rated output voltage within three seconds. To save power consumption, after V_{DD} voltage exceeds turn-on voltage and enters normal operation; this high voltage startup circuit is shut down to avoid power loss from startup resistor.

Figure 36 shows the characteristic curve of V_{DD} voltage and operating current I_{DD} . When V_{DD} voltage is lower than $V_{DD-PWM-OFF}$, FAN6921MR stops all switching operation and turns off some internal unnecessary circuit to reduce operating current. By doing so, the period from $V_{DD-PWM-OFF}$ to V_{DD-OFF} can be extended and the hiccup mode frequency can be decreased to reduce the input power in case of output short circuit. Figure 37 shows the typical waveforms of V_{DD} voltage and gate signal at hiccup mode operation.

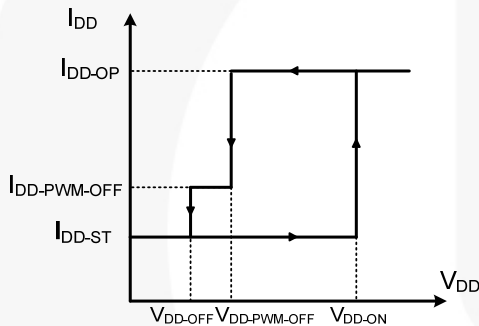


Figure 36. V_{DD} vs. I_{DD-OP} Characteristic Curve

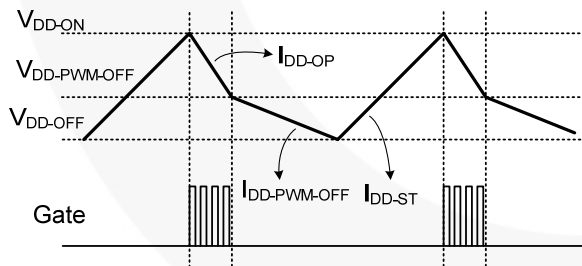


Figure 37. Typical Waveform of V_{DD} Voltage and Gate Signal at Hiccup Mode Operation

Green-Mode Operation and PFC-ON / OFF Control (FB Pin)

Green mode mechanism is used to further reduce power loss in the system (e.g. switching loss). It uses an off-time modulation technique to regulate switching frequency according to FB pin voltage. When output loading is decreased, FB voltage becomes lower due to secondary feedback movement and the $t_{OFF-MIN}$ is extended. After $t_{OFF-MIN}$ (determined by FB voltage), the internal valley detection circuit is activated to detect the

valley on the drain voltage of the PWM switch. When the valley signal is detected, FAN6921MR outputs PWM gate signal to turn on the switch and begin a new switching cycle.

With green mode operation and valley detection, at light load condition; power system can perform extended valley switching at DCM operation and can further reduce switching loss for getting better conversion efficiency. The FB pin voltage versus $t_{OFF-MIN}$ time characteristic curve is shown in Figure 38. As Figure 38 shows, FAN6921MR can narrow down to 2.25 ms t_{OFF} time, which is around 440 Hz switching frequency.

Referring to Figure 1 and Figure 2, FB pin voltage is not only used to receive secondary feedback signal to determine gate on-time, but also determines PFC stage on or off status. At no-load or light-load conditions, if PFC stage is set to be off; that can reduce power consumption from PFC stage switching device and increase conversion efficiency. When output loading is decreased, the FB pin voltage becomes lower and, therefore, the FAN6921MR can detect the output loading level according to the FB pin voltage to control the on / off status of the PFC part.

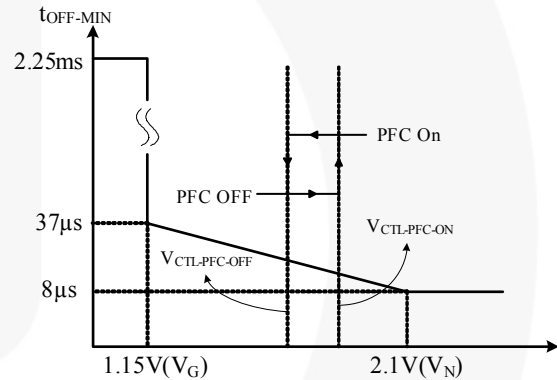


Figure 38. V_{FB} Voltage vs. $t_{OFF-MIN}$ Time Characteristic Curve

Valley Detection (DET Pin)

When FAN6921MR operates in green mode, $t_{OFF-MIN}$ time is determined by the green mode circuit according to FB pin voltage level. After $t_{OFF-MIN}$ time, the internal valley detection circuit is activated. During the t_{OFF} time of PWM switch, when transformer inductor current discharges to zero, the transformer inductor and parasitic capacitor of PWM switch start to resonate concurrently. When the drain voltage on the PWM switch falls, the voltage across on auxiliary winding V_{AUX} also decreases since auxiliary winding is coupled to primary winding. Once the V_{AUX} voltage resonates and falls to negative, V_{DET} voltage is clamped by the DET pin (refer to Figure 39) and FAN6921MR is forced to flow out a current I_{DET} . FAN6921MR reflects and compares this I_{DET} current. If this source current rises to a threshold current, PWM gate signal is sent out after a fixed delay time (200 ns typical).

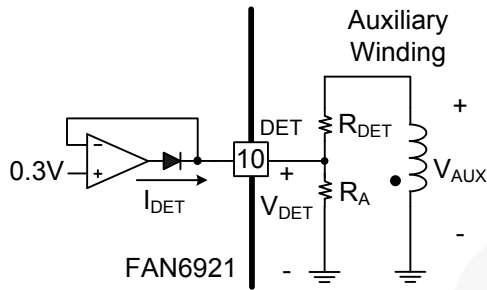


Figure 39. Valley Detection

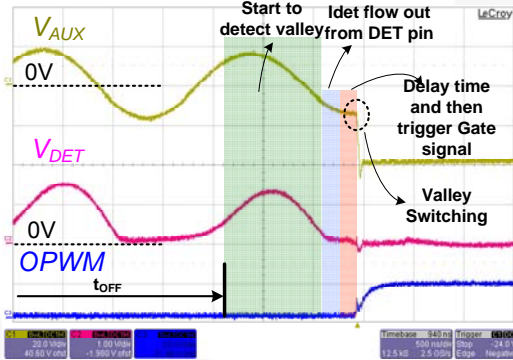


Figure 40. Measured Waveform of Valley Detection

High / Low Line Over-Power Compensation (DET Pin)

Generally, when the power switch turns off, there is a delay time from gate signal falling edge to power switch off. This delay is produced by an internal propagation delay of the controller and the turn-off delay time of PWM switch due to gate resistor and gate-source capacitor C_{ISS} of PWM switch. At different AC input voltage, this delay time produces different maximum output power under the same PWM current limit level. Higher input voltage generates higher maximum output power since applied voltage on primary winding is higher and causes higher rising slope inductor current. It results in higher peak inductor current at the same delay time. Furthermore, under the same output wattage, the peak switching current at high line is lower than that at low line. Therefore, to make the maximum output power close at different input voltages, the controller needs to regulate V_{LIMIT} voltage of the CSPWM pin to control the PWM switch current.

Referring to Figure 41, during t_{ON} time of the PWM switch, the input voltage is applied to primary winding and the voltage across on auxiliary winding V_{AUX} is proportional to primary winding voltage. So as the input voltage increases, the reflected voltage on auxiliary winding V_{AUX} becomes higher as well. FAN6921MR also clamps the DET pin voltage and flows out a current I_{DET} . Since the current I_{DET} is in accordance with V_{AUX} voltage, FAN6921MR can depend on this current I_{DET} during t_{ON} time period to regulate the current limit level of PWM switch to perform high / low line over-power compensation.

As the input voltage increases, the reflected voltage on the auxiliary winding V_{AUX} becomes higher as well as the current I_{DET} and the controller regulates the V_{LIMIT} to a lower level.

The R_{DET} resistor is connected from auxiliary winding to the DET pin. Engineers can adjust this R_{DET} resistor to get proper V_{LIMIT} voltage to fit power system needs. The characteristic curve of I_{DET} current vs. V_{LIMIT} voltage on CSPWM pin is shown in Figure 42.

$$I_{DET} = \left[V_{IN} \times \left(\frac{N_A}{N_P} \right) \right] / R_{DET} \quad (1)$$

where V_{IN} is input voltage; N_A is turn number of auxiliary winding; and N_P is turn number of primary winding.

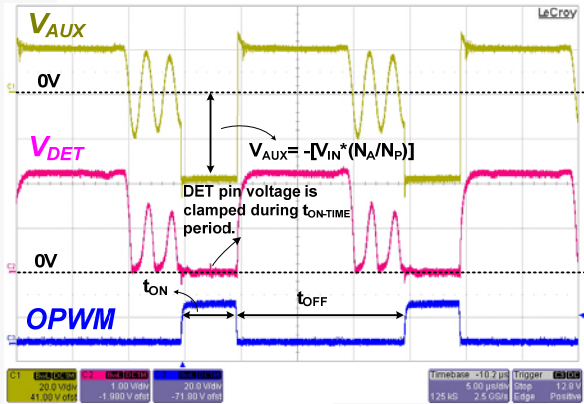


Figure 41. Relationship between V_{AUX} and V_{IN}

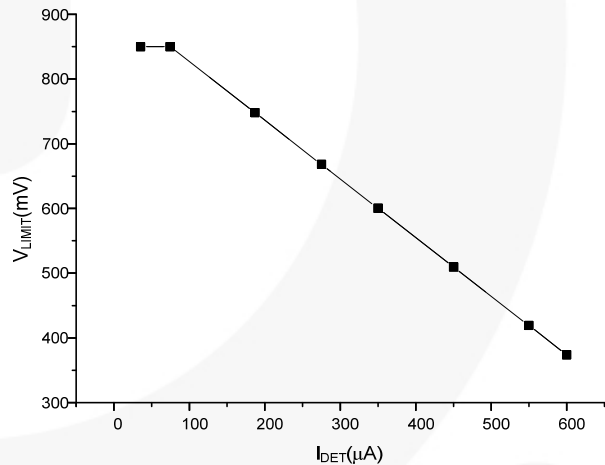


Figure 42. I_{DET} Current vs. V_{LIMIT} Voltage Characteristic Curve

Leading-Edge Blanking (LEB)

When the PFC or PWM switches are turned on, a voltage spike is induced on the current sense resistor due to the reciprocal effect by reverse recovery energy of the output diode and C_{OSS} of power MOSFET. To prevent this spike, a leading-edge blanking time is built-in to FAN6921MR and a small RC filter is also recommended between the CSPWM pin and GND (e.g. 100 Ω , 470 pF).

Protection for PWM Stage

VDD Pin Over-Voltage Protection (OVP)

V_{DD} over-voltage protection is used to prevent device damage once V_{DD} voltage is higher than device stress rating voltage. In case of V_{DD} OVP, the controller stops all switching operation immediately and enters latch-off mode until the AC plug is removed.

Adjustable Over-Temperature Protection and Externally Latch Triggering (RT Pin)

Figure 43 is a typical application circuit with an internal block of RT pin. As shown, a constant current I_{RT} flows out from the RT pin, so the voltage V_{RT} on RT pin can be obtained as I_{RT} current multiplied by the resistor, which consists of NTC resistor and R_A resistor. If the RT pin voltage is lower than 0.8 V and lasts for a de-bounce time, latch mode is activated and stops all PFC and PWM switching.

RT pin is usually used to achieve over-temperature protection with a NTC resistor and provides external latch triggering for additional protection. Engineers can use an external triggering circuit (e.g. transistor) to pull low the RT pin and activate controller latch mode.

Generally, the external latch triggering needs to activate rapidly since it is usually used to protect power system from abnormal conditions. Therefore, the protection debounce time of the RT pin is set to around 110 μs once RT pin voltage is lower than 0.5 V.

For over-temperature protection, because the temperature would not change immediately; the RT pin voltage is reduced slowly as well. The debounce time for adjustable OTP should not need a fast reaction. To prevent improper latch triggering on the RT pin due to exacting test condition (e.g. lightning test), when the RT pin triggering voltage is higher than 0.5 V, the protection debounce time is set to around 10 ms. To avoid improper triggering on the RT pin, it is recommended to add a small value capacitor (e.g. 1000 pF) paralleled with NTC and R_A resistor.

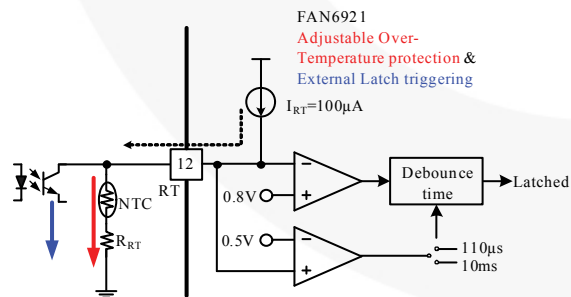


Figure 43. Adjustable Over-Temperature Protection

Output Over-Voltage Protection (DET Pin)

Referring to Figure 44, during the discharge time of PWM transformer inductor; the voltage across on auxiliary winding is reflected from secondary winding and therefore the flat voltage on the DET pin is proportional to the output voltage. FAN6921MR can sample this flat voltage level after a t_{OFF} blanking time to perform output over-voltage protection. This t_{OFF} blanking time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling flat voltage level is compared with internal threshold voltage 2.5 V and, once the protection is activated, FAN6921MR enters latch mode.

The controller can protect rapidly by this kind of cycle-by-cycle sampling method in the case of output over voltage. The protection voltage level can be determined by the ratio of external resistor divider R_A and R_{DET}. The flat voltage on DET pin can be expressed by the following equation:

$$V_{DET} = (N_A / N_S) \times V_O \times \frac{R_A}{R_{DET} + R_A} \quad (2)$$

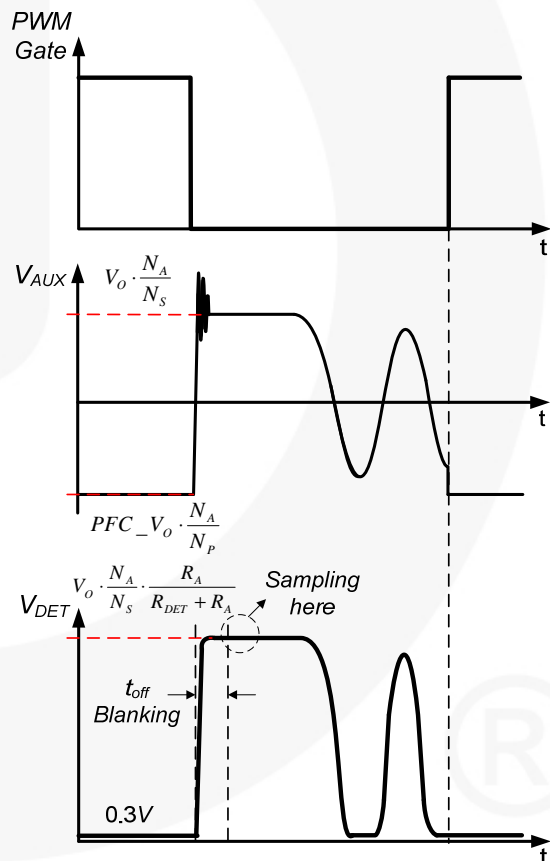


Figure 44. Operation Waveform of Output Over-Voltage Detection

Open-Loop, Short-Circuit, and Overload Protection (FB Pin)

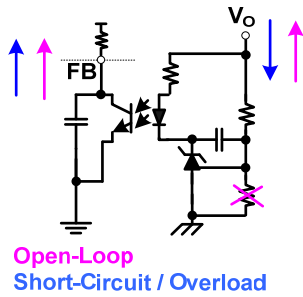


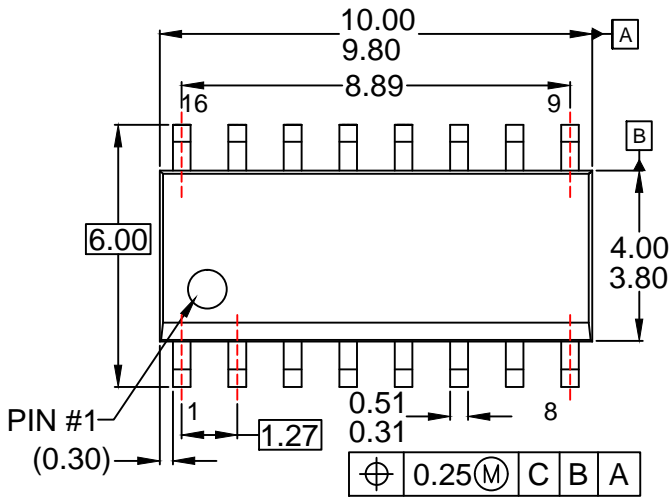
Figure 45. FB Pin Open-Loop, Short Circuit, and Overload Protection

Referring to Figure 45, outside of FAN6921MR, the FB pin is connected to the collector of transistor of an optocoupler. Inside of FAN6921MR, the FB pin is connected to an internal voltage bias through a resistor around 5 kΩ.

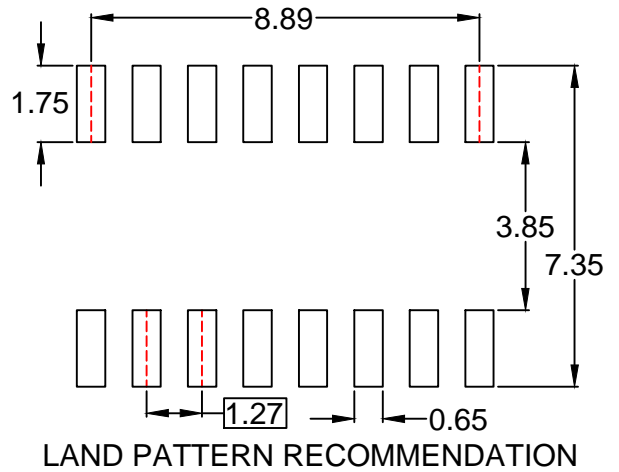
As the output loading is increased, the output voltage is decreased and the sink current of transistor of optocoupler on primary side is reduced. So the FB pin voltage is increased by internal voltage bias. In the case of an open loop, output short circuit, or overload conditions, this sink current is further reduced and the FB pin voltage is pulled to high level by internal bias voltage. When the FB pin voltage is higher than 4.2 V for 50 ms, the FB pin protection is activated.

Under-Voltage Lockout (UVLO, VDD Pin)

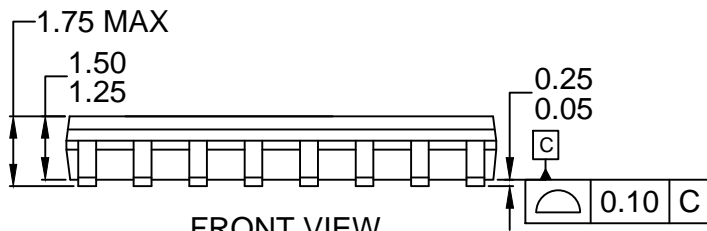
Referring to Figure 36 and Figure 37, the turn-on and turn-off V_{DD} threshold voltages of FAN6921MR are fixed at 18 V and 10 V, respectively. During startup, the hold-up capacitor (V_{DD} cap.) is charged by HV startup current until V_{DD} voltage reaches the turn-on voltage. Before the output voltage rises to rated voltage and delivers energy to the V_{DD} capacitor from auxiliary winding, this hold-up capacitor has to sustain the V_{DD} voltage energy for operation. When V_{DD} voltage reaches turn-on voltage, FAN6921MR starts all switching operation if no protection is triggered before V_{DD} voltage drops to turn-off voltage $V_{DD-PWM-OFF}$.



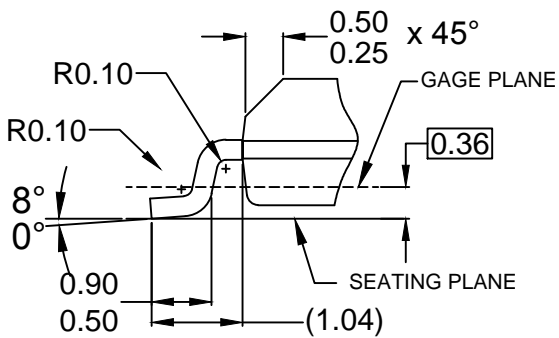
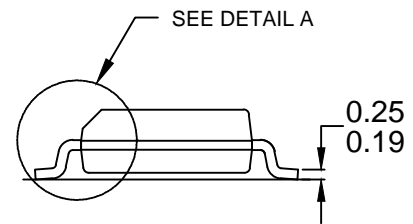
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW



DETAIL A

SCALE: 2:1

NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
- D) CONFORMS TO ASME Y14.5M-2009
- E) LANDPATTERN STANDARD:
SOIC127P600X175-16AM
- F) DRAWING FILE NAME: M16AREV13.





TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|--------------------------|--|---------------------------------------|------------------|
| AccuPower™ | F-PFS™ | OPTOPLANAR® | SYSTEM GENERAL® |
| AttitudeEngine™ | FRFET® | Power Supply WebDesigner™ | TinyBoost® |
| Awinda® | Global Power Resource SM | PowerTrench® | TinyBuck® |
| AX-CAP®* | GreenBridge™ | PowerXS™ | TinyCalc™ |
| BitSiC™ | Green FPS™ | Programmable Active Droop™ | TinyLogic® |
| Build it Now™ | Green FPS™ e-Series™ | QFET® | TINYOPTO™ |
| CorePLUS™ | Gmax™ | QS™ | TinyPower™ |
| CorePOWER™ | GTO™ | Quiet Series™ | TinyPWM™ |
| CROSSVOL™ | IntelliMAX™ | RapidConfigure™ | TinyWire™ |
| CTL™ | ISOPLANAR™ | Saving our world, 1mW/W/kW at a time™ | TranSiC™ |
| Current Transfer Logic™ | Making Small Speakers Sound Louder and Better™ | SignalWise™ | TriFault Detect™ |
| DEUXPEED® | MegaBuck™ | SmartMax™ | TRUECURRENT®* |
| Dual Cool™ | MICROCOUPLER™ | SMART START™ | μSerDes™ |
| EcoSPARK® | MicroFET™ | Solutions for Your Success™ | UHC® |
| EfficientMax™ | MicroPak™ | SPM® | Ultra FRFET™ |
| ESBC™ | MicroPak2™ | STEALTH™ | UniFET™ |
| F [®] | MillerDrive™ | SuperFET® | VCX™ |
| Fairchild® | MotionMax™ | SuperSOT™-3 | VisualMax™ |
| Fairchild Semiconductor® | MotionGrid® | SuperSOT™-6 | VoltagePlus™ |
| FACT Quiet Series™ | MTi® | SuperSOT™-8 | XST™ |
| FACT® | MTx® | SupreMOS® | Xsens™ |
| FastvCore™ | MVN® | SyncFET™ | 仙童® |
| FETBench™ | mWSaver® | Sync-Lock™ | |
| FPS™ | OptoHiT™ | | |
| | OPTOLOGIC® | | |

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

AUTHORIZED USE

Unless otherwise specified in this data sheet, this product is a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability. This product may not be used in the following applications, unless specifically approved in writing by a Fairchild officer: (1) automotive or other transportation, (2) military/aerospace, (3) any safety critical application – including life critical medical equipment – where the failure of the Fairchild product reasonably would be expected to result in personal injury, death or property damage. Customer's use of this product is subject to agreement of this Authorized Use policy. In the event of an unauthorized use of Fairchild's product, Fairchild accepts no liability in the event of product failure. In other respects, this product shall be subject to Fairchild's Worldwide Terms and Conditions of Sale, unless a separate agreement has been signed by both Parties.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Terms of Use

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor:](#)

[FAN6921MRMY](#)