



FCH041N65F_F085

N-Channel SuperFET II FRFET MOSFET

650 V, 76 A, 41 mΩ



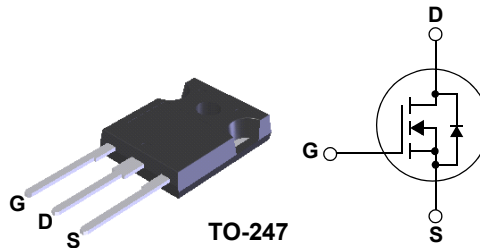
Features

- Typical $R_{DS(on)}$ = 34 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$
- Typical $Q_{g(tot)}$ = 234 nC at $V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$
- UIS Capability
- Qualified to AEC Q101
- RoHS Compliant

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SuperFETII is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



For current package drawing, please refer to the Fairchild website at <https://www.fairchildsemi.com/package-drawings/TO/TO247A03.pdf>

Application

- Automotive On Board Charger
- Automotive DC/DC converter for HEV



Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain to Source Voltage	650	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	$T_C = 25^\circ\text{C}$ 76 $T_C = 100^\circ\text{C}$ 24	A
	Pulsed Drain Current	See Fig 4	A
E_{AS}	Single Pulse Avalanche Rating (Note 2)	2025	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P_D	Power Dissipation	595	W
	Derate Above 25°C	4.76	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$
$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	0.21	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 4)	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH041N65F	FCH041N65F_F085	TO-247	-	-	30

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 18\text{ mH}$, $I_{AS} = 15\text{ A}$, $V_{DD} = 100\text{ V}$ during inductor charging and $V_{DD} = 0\text{ V}$ during time in avalanche.
- 3: $I_{SD} \leq 38\text{ A}$, $di/dt \leq 200\text{ A/us}$, $V_{DD} \leq 380\text{ V}$, starting $T_J = 25^\circ\text{C}$.
- 4: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

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Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	650	-	-	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 650\text{V}$, $T_J = 25^\circ\text{C}$	-	-	10	μA
		$V_{GS} = 0\text{V}$, $T_J = 150^\circ\text{C}$ (Note 5)	-	-	1	mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	3.0	-	5.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 38\text{A}$, $T_J = 25^\circ\text{C}$	-	34	41	$\text{m}\Omega$
		$V_{GS} = 10\text{V}$, $T_J = 150^\circ\text{C}$ (Note 5)	-	80	96	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	10200	13566	pF
C_{oss}	Output Capacitance		-	10529	14004	pF
C_{rss}	Reverse Transfer Capacitance		-	227	-	pF
$C_{oss(eff)}$	Effective Output Capacitance	$V_{DS} = 0\text{V}$ to 520V , $V_{GS} = 0\text{V}$	-	843	-	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	0.5	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	$V_{DD} = 380\text{V}$ $I_D = 38\text{A}$ $V_{GS} = 10\text{V}$	-	234	304	nC
$Q_{g(th)}$	Threshold Gate Charge		-	17	22	nC
Q_{gs}	Gate to Source Gate Charge		-	50	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	90	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 380\text{V}$, $I_D = 38\text{A}$, $V_{GS} = 10\text{V}$, $R_G = 4.7\Omega$	-	94	207	ns
$t_{d(on)}$	Turn-On Delay Time		-	55	-	ns
t_r	Rise Time		-	39	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	183	-	ns
t_f	Fall Time		-	8	-	ns
t_{off}	Turn-Off Time		-	191	402	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 38\text{A}$, $V_{GS} = 0\text{V}$	-	-	1.2	V
T_{rr}	Reverse Recovery Time	$I_F = 38\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	235	-	ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 480\text{V}$	-	2.0	-	μC

Notes:

5: The maximum value is specified by design at $T_J = 150^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

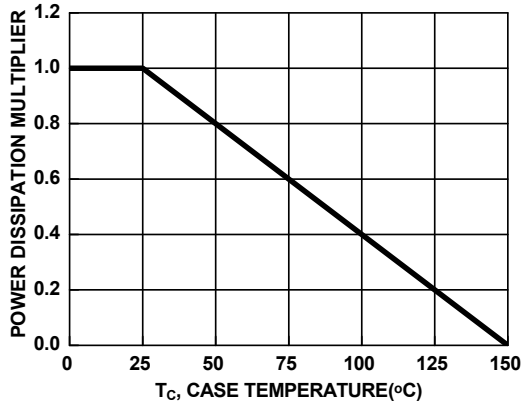


Figure 1. Normalized Power Dissipation vs. Case Temperature

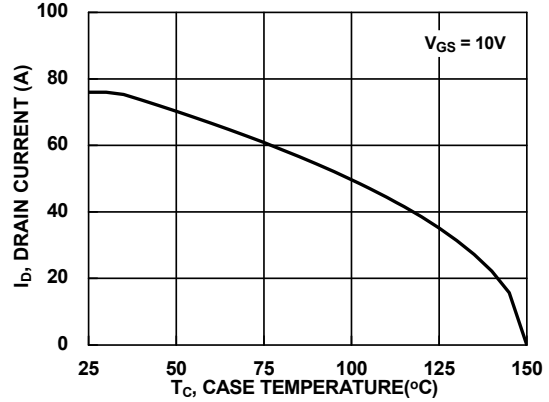


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

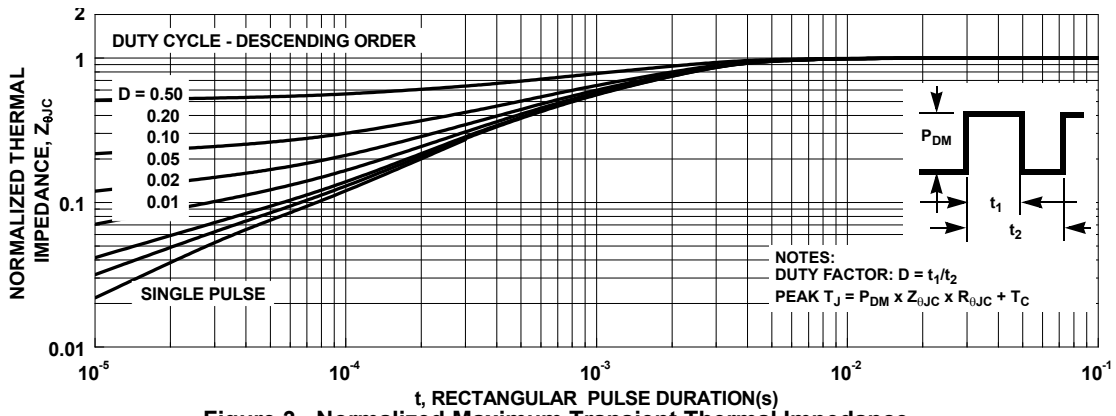


Figure 3. Normalized Maximum Transient Thermal Impedance

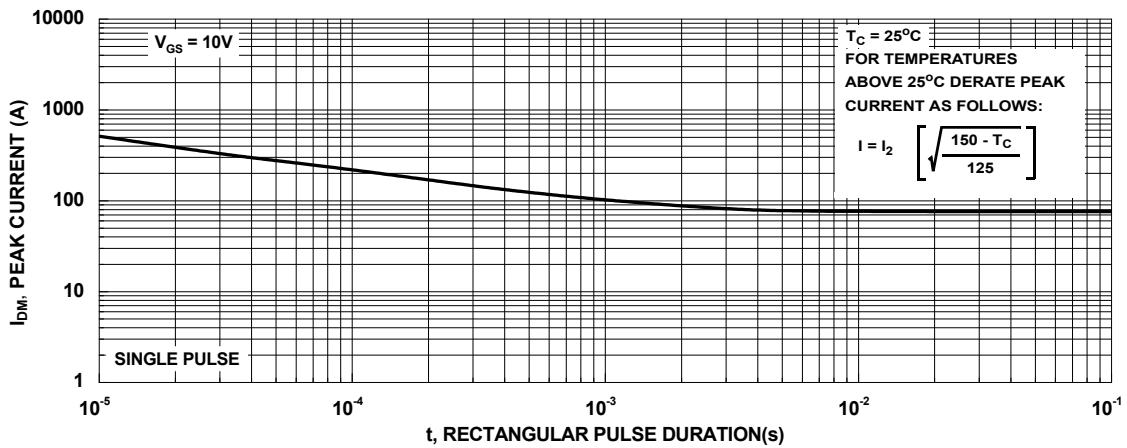


Figure 4. Peak Current Capability

Typical Characteristics

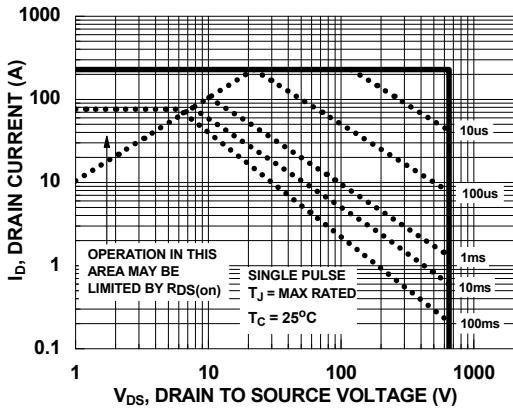


Figure 5. Forward Bias Safe Operating Area

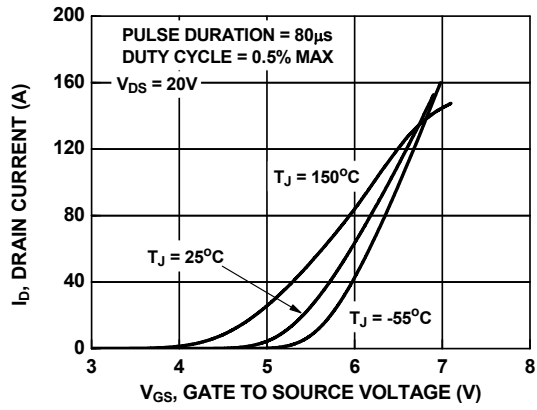


Figure 6. Transfer Characteristics

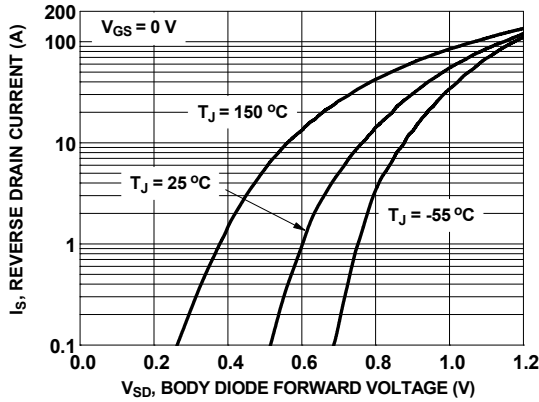


Figure 7. Forward Diode Characteristics

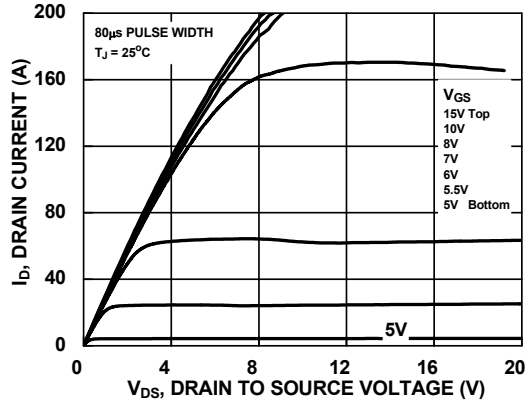


Figure 8. Saturation Characteristics

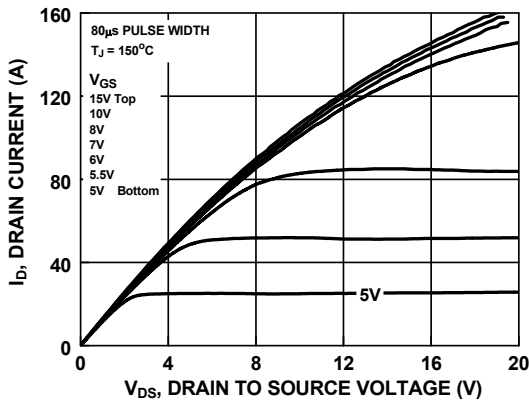


Figure 9. Saturation Characteristics

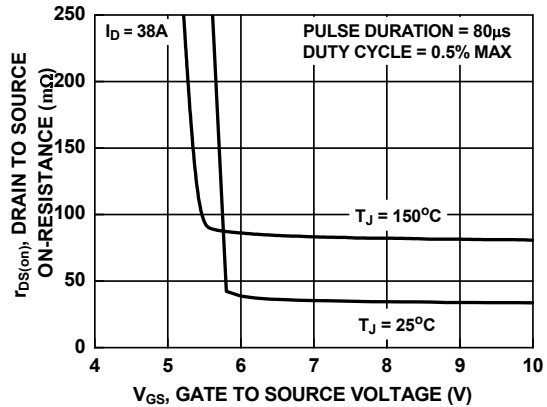


Figure 10. $R_{DS(on)}$ vs. Gate Voltage

Typical Characteristics

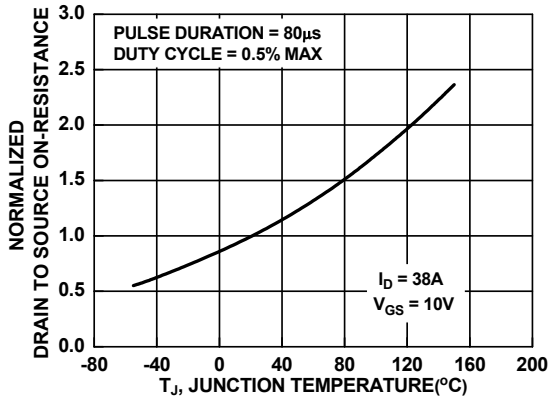


Figure 11. Normalized $R_{DS(on)}$ vs. Junction Temperature

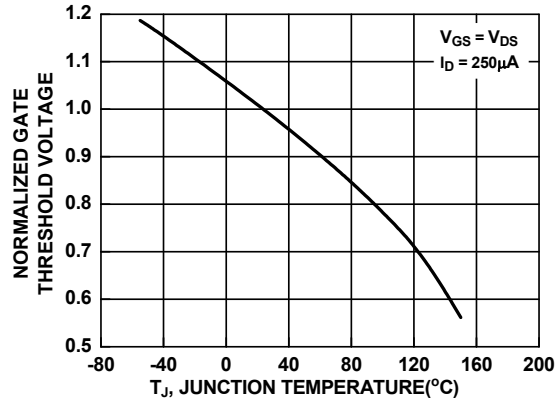


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

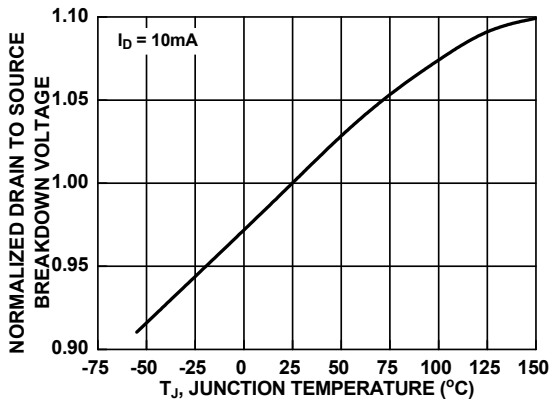


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

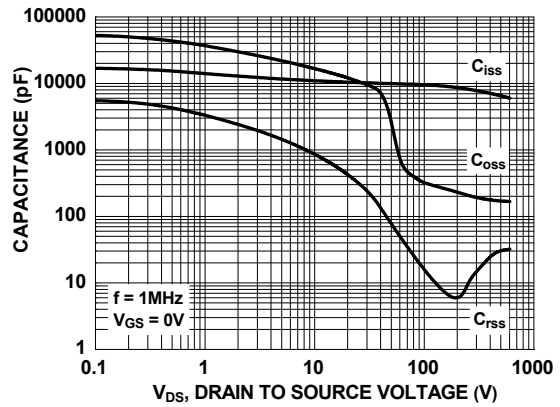


Figure 14. Capacitance vs. Drain to Source Voltage

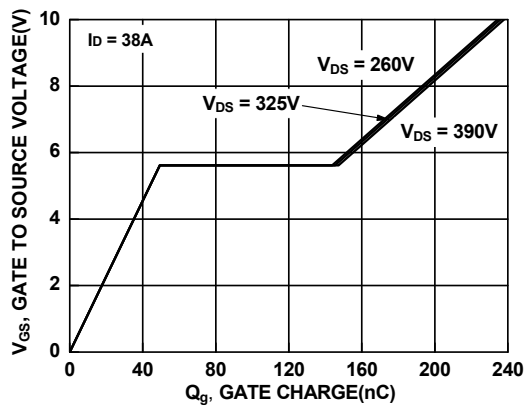


Figure 15. Gate Charge vs. Gate to Source Voltage

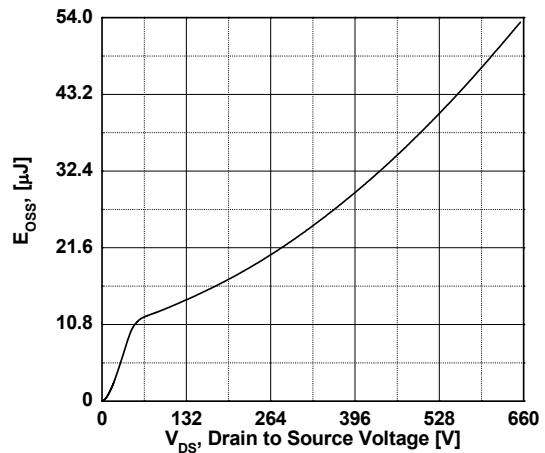


Figure 16. E_{oss} vs. Drain to Source Voltage

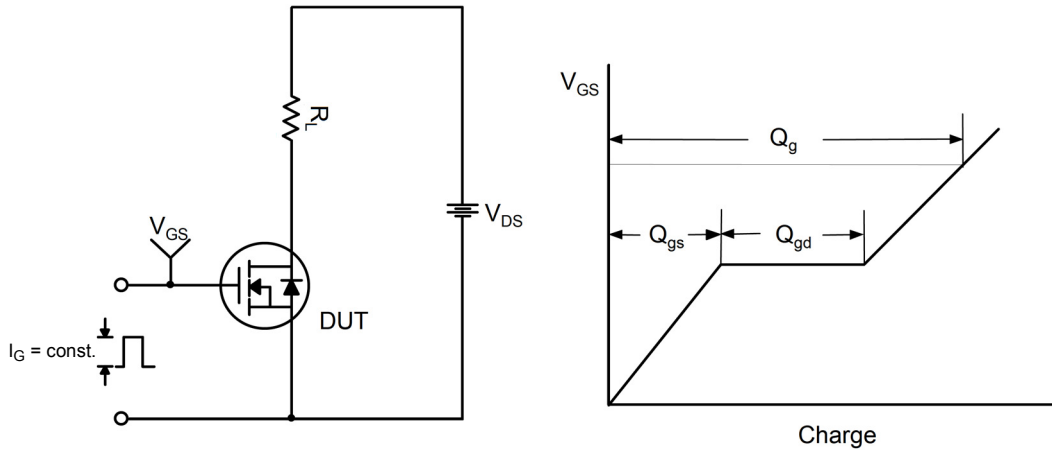


Figure 17. Gate Charge Test Circuit & Waveform

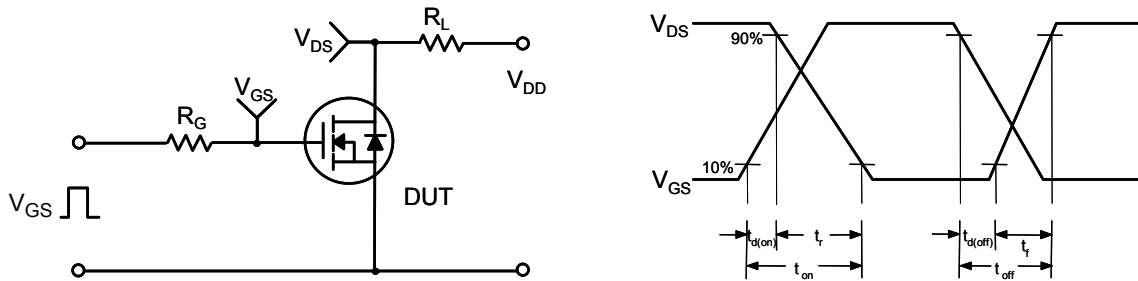


Figure 18. Resistive Switching Test Circuit & Waveforms

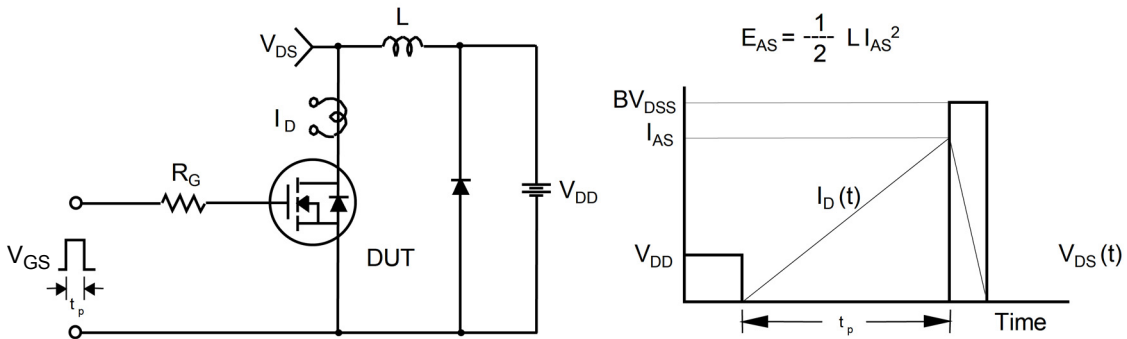
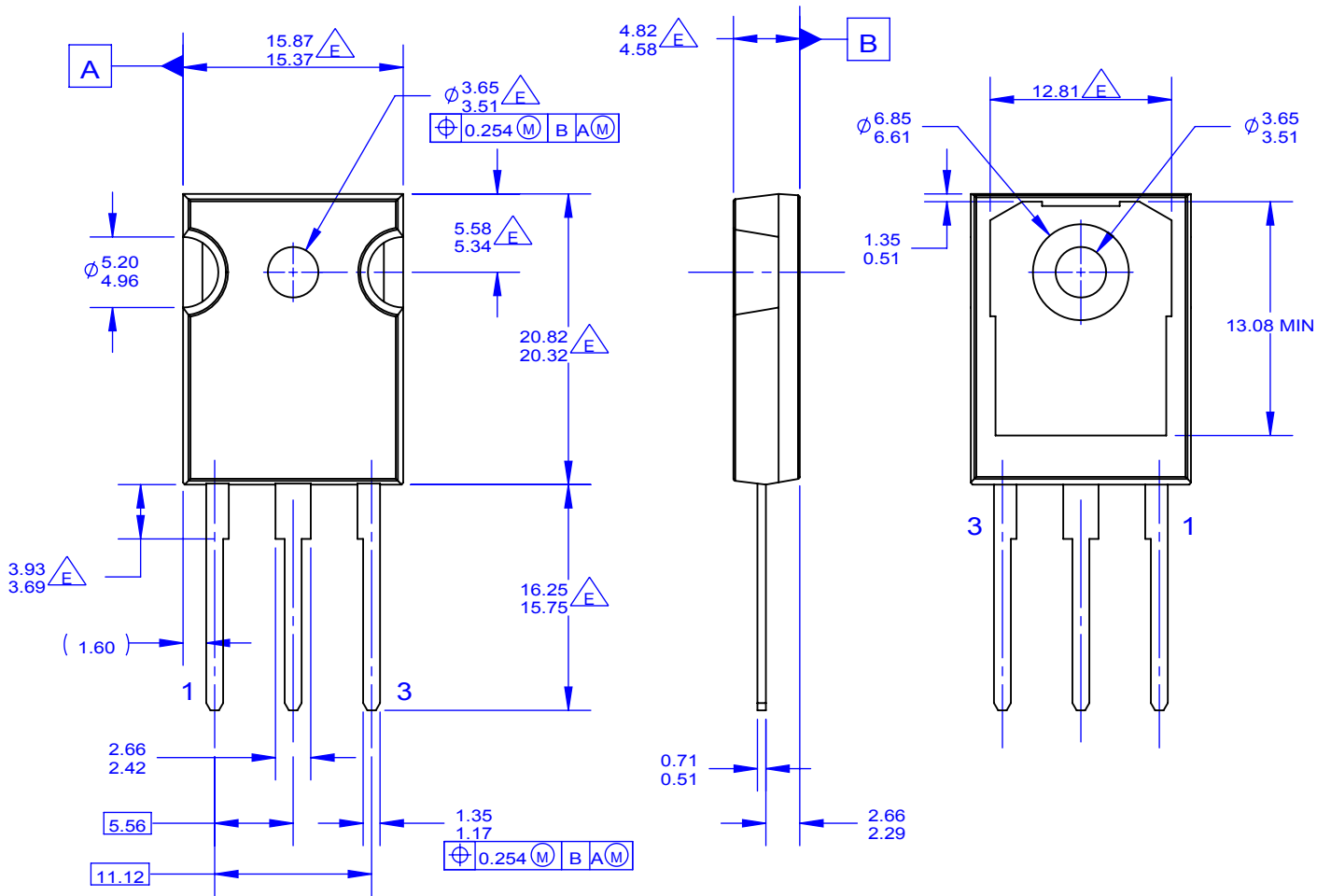


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES: UNLESS OTHERWISE SPECIFIED.






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