



# FDMC7200S

## Dual N-Channel PowerTrench<sup>®</sup> MOSFETs 30 V, 22 mΩ, 10 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 22 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 6\text{ A}$
- Max  $r_{DS(on)}$  = 34 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 5\text{ A}$

Q2: N-Channel

- Max  $r_{DS(on)}$  = 10 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 8.5\text{ A}$
- Max  $r_{DS(on)}$  = 13.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 7.2\text{ A}$
- RoHS Compliant

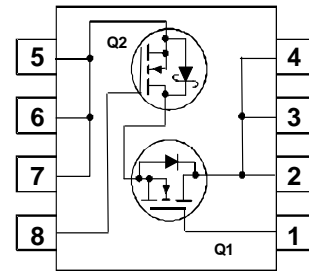
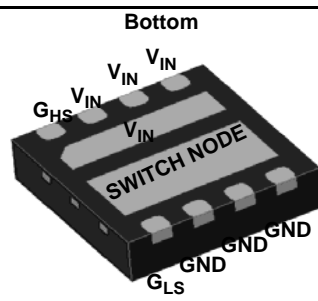
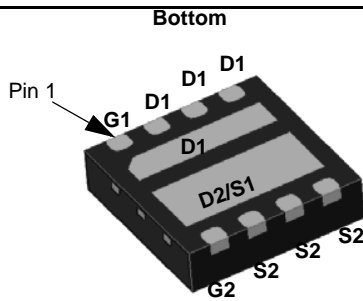


### General Description

This device includes two specialized N-Channel MOSFETs in a dual power33 (3mm X 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

### Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load



Power33

### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	18	13	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	23	46	
	-Continuous $T_A = 25^\circ\text{C}$	7 <sup>1a</sup>	13 <sup>1b</sup>	
	-Pulsed	40	27	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	12	32	
$P_D$	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	1.9 <sup>1a</sup>	2.5 <sup>1b</sup>	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	0.7 <sup>1c</sup>	1.0 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 <sup>1a</sup>	50 <sup>1b</sup>	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 <sup>1c</sup>	125 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	4.2	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7200S	FDMC7200S	Power 33	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = 1 \text{ mA}$ , referenced to $25^\circ\text{C}$	Q1 Q2		14 13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			100 100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = 1 \text{ mA}$	Q1 Q2	1.0 1.0	2.3 2.0	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = 1 \text{ mA}$ , referenced to $25^\circ\text{C}$	Q1 Q2		-5 -6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}, T_J = 125^\circ\text{C}$	Q1		17 25 23	22 34 30	m $\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 8.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 7.2 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 8.5 \text{ A}, T_J = 125^\circ\text{C}$	Q2		7.8 10.3 11.4	10.0 13.5 13.1	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 6 \text{ A}$ $V_{DD} = 5 \text{ V}, I_D = 8.5 \text{ A}$	Q1 Q2		29 43		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance		Q1 Q2		495 1080	660 1436	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Q1 Q2		145 373	195 495	pF
$C_{riss}$	Reverse Transfer Capacitance		Q1 Q2		20 35	30 52	pF
$R_g$	Gate Resistance		Q1 Q2	0.2 0.2	1.4 1.2	4.2 3.6	$\Omega$

**Switching Characteristics**

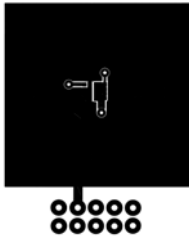
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 15 \text{ V}, I_D = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		11 7.6	20 15	ns
$t_r$	Rise Time		Q1 Q2		3.1 1.8	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = 15 \text{ V}, I_D = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		35 21	56 34	ns
$t_f$	Fall Time		Q1 Q2		1.3 8.5	10 17	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	Q1 Q2		7.3 15.7	10 22	nC
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$	Q1 Q2		3.1 7.2	4.3 10
$Q_{gs}$	Gate to Source Charge	Q2 $V_{DD} = 15 \text{ V}$ $I_D = 8.5 \text{ A}$	Q1 Q2		1.8 3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		1 1.9		nC

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 6\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 8.5\text{ A}$ (Note 2)	Q2		0.8	1.2	
		$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q2		0.6	0.8	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 6\text{ A}, di/dt = 100\text{ A/s}$	Q1		13	24	ns
		Q2		20	32		
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = 8.5\text{ A}, di/dt = 300\text{ A/s}$	Q1		2.3	10	nC
			Q2		15	24	

**Notes:**

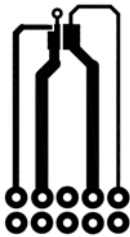
1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



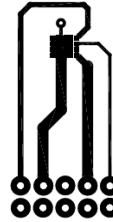
a.  $65\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



c.  $180\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper



d.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting Q1:  $T = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I = 5\text{ A}$ ,  $V_{gs} = 10\text{ V}$ ,  $V_{dd} = 27\text{ V}$ , 100% test at  $L = 3\text{ mH}$ ,  $I = 4\text{ A}$ ; Q2:  $T = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I = 8\text{ A}$ ,  $V_{gs} = 10\text{ V}$ ,  $V_{dd} = 27\text{ V}$ , 100% test at  $L = 3\text{ mH}$ ,  $I = 3.2\text{ A}$ .

4. As an N-ch device, the negative  $V_{gs}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

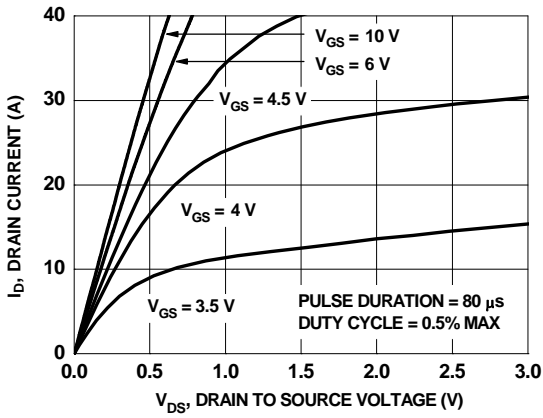


Figure 1. On Region Characteristics

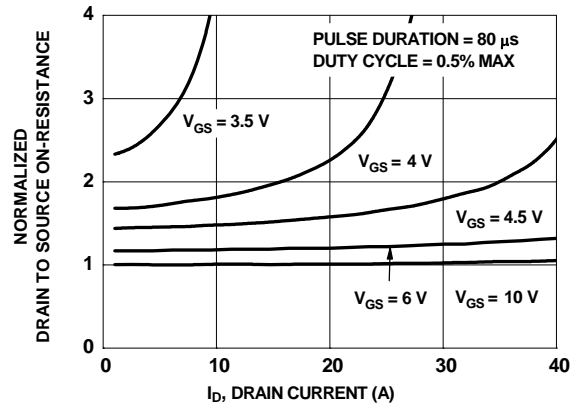


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

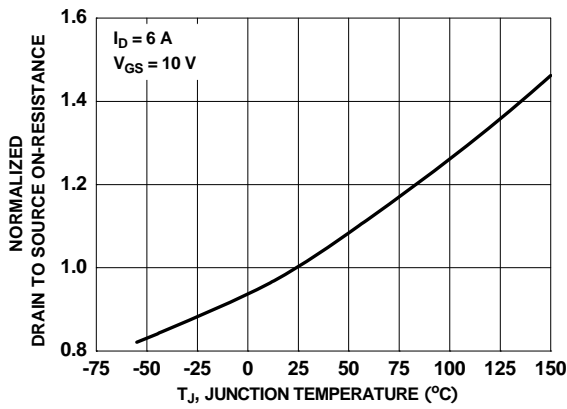


Figure 3. Normalized On Resistance vs. Junction Temperature

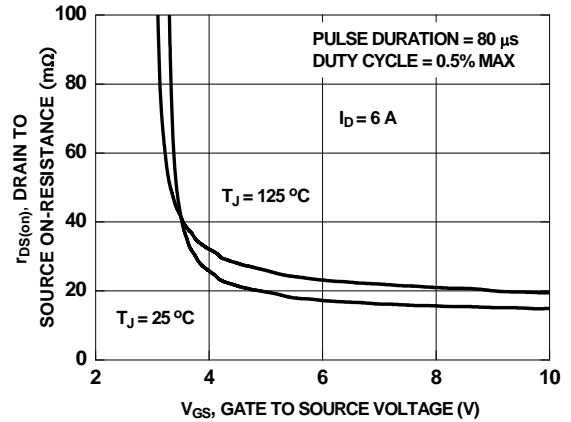


Figure 4. On-Resistance vs. Gate to Source Voltage

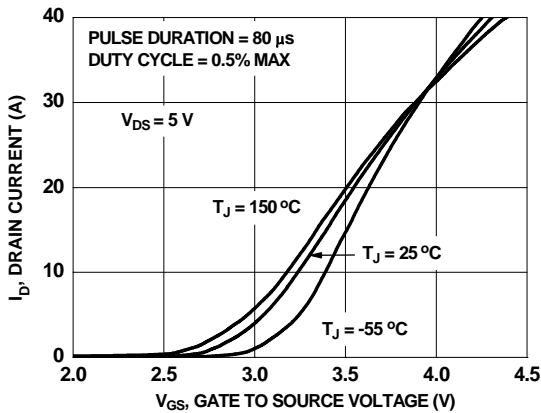


Figure 5. Transfer Characteristics

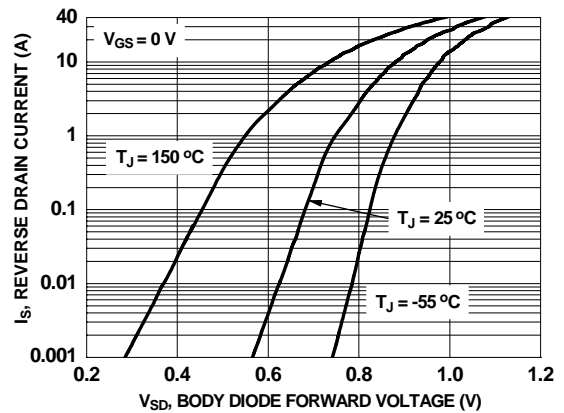
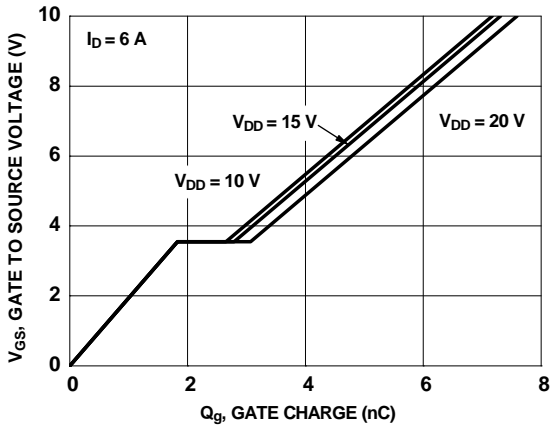
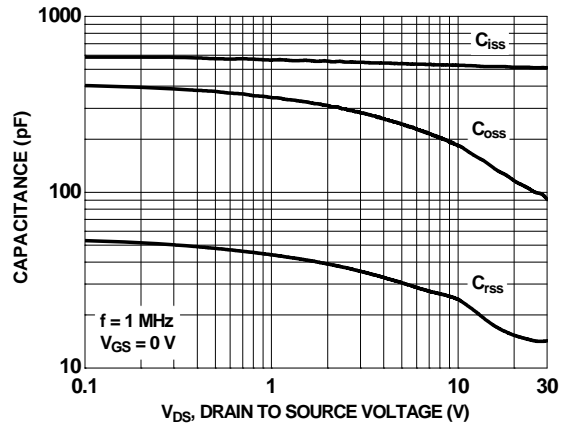


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

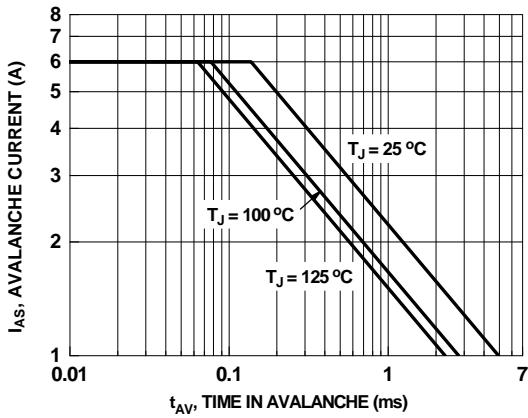
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



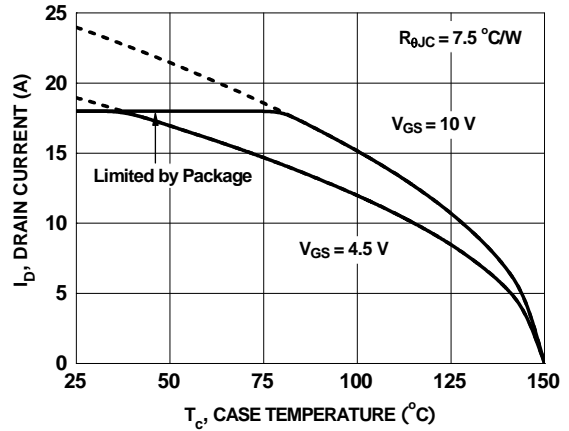
**Figure 7. Gate Charge Characteristics**



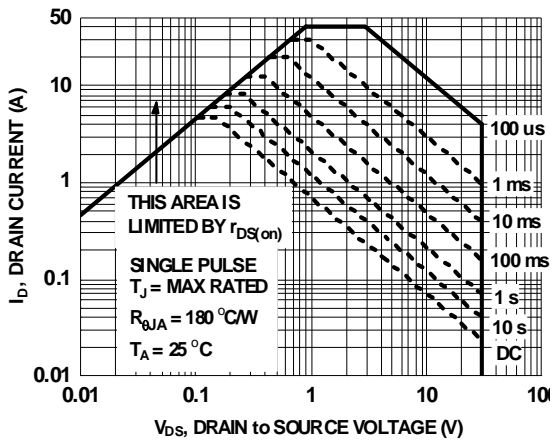
**Figure 8. Capacitance vs. Drain to Source Voltage**



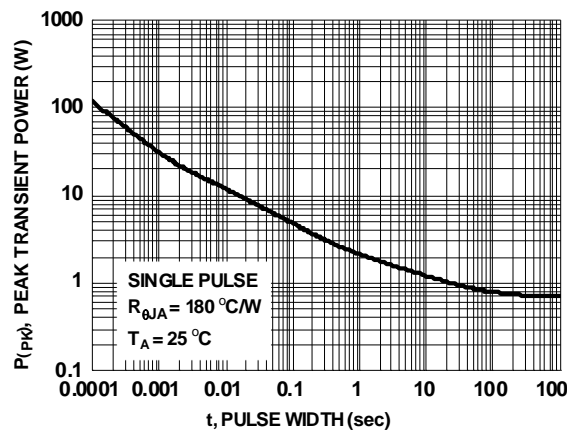
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

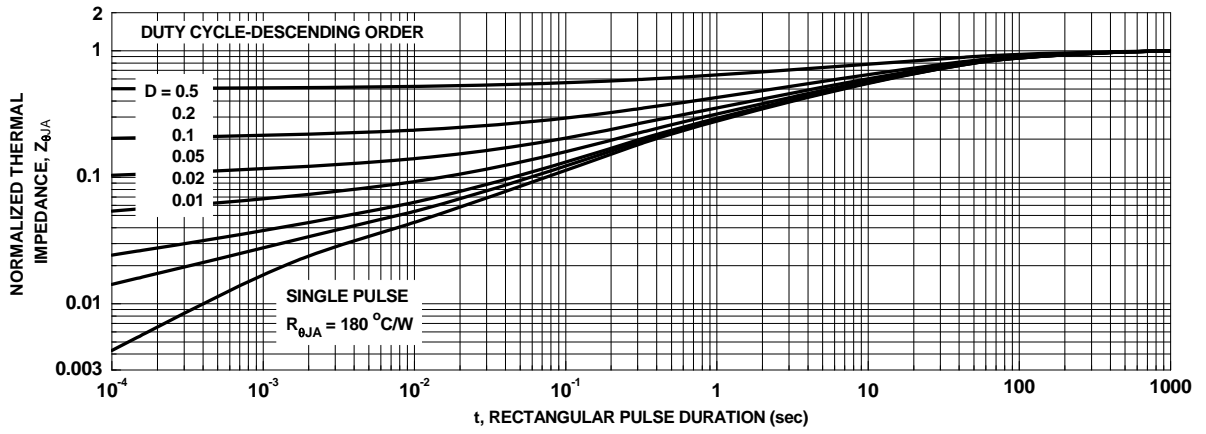


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

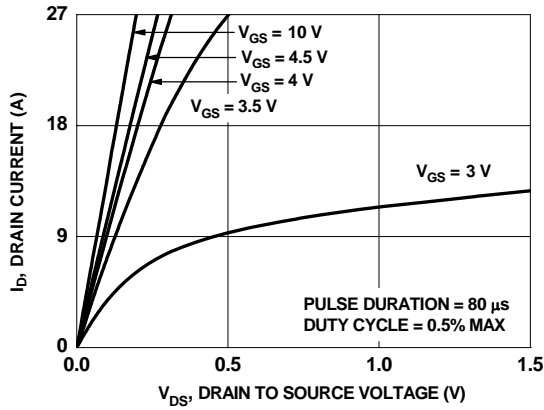


Figure 14. On-Region Characteristics

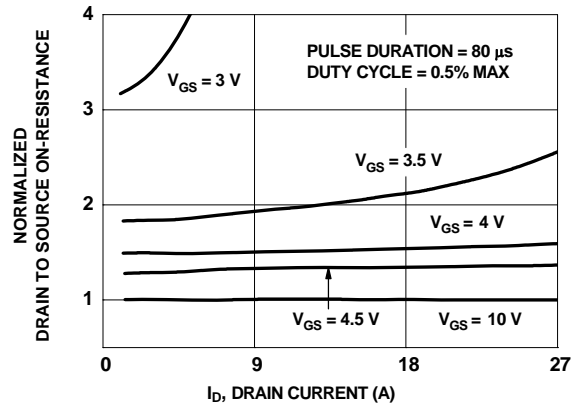


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

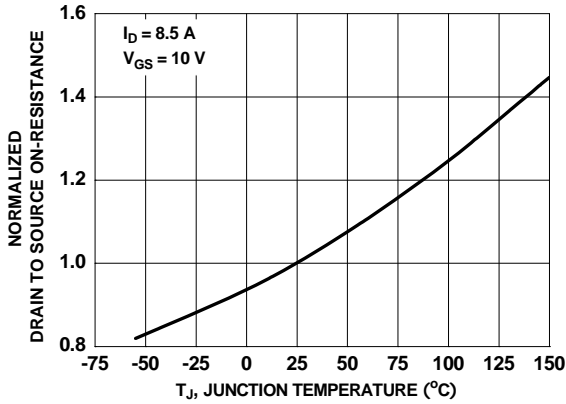


Figure 16. Normalized On-Resistance vs. Junction Temperature

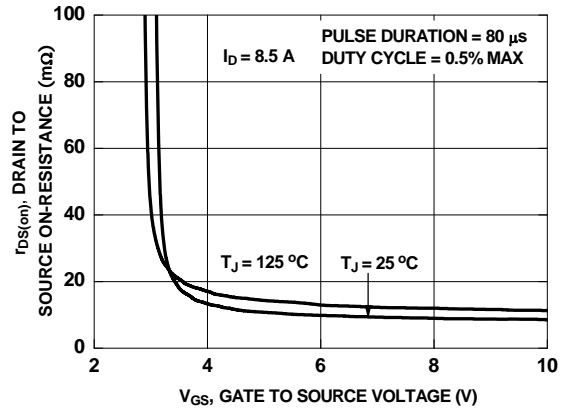


Figure 17. On-Resistance vs. Gate to Source Voltage

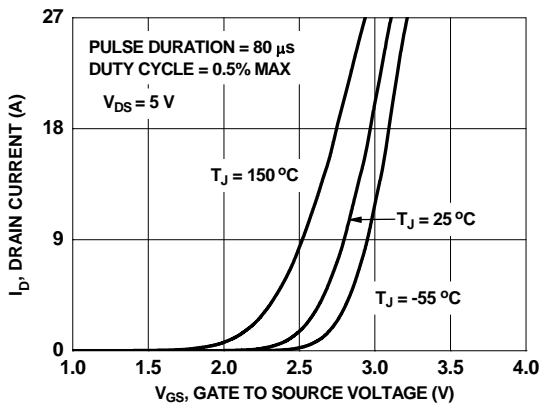


Figure 18. Transfer Characteristics

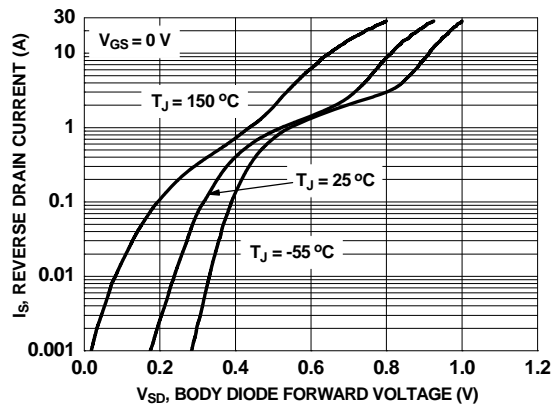
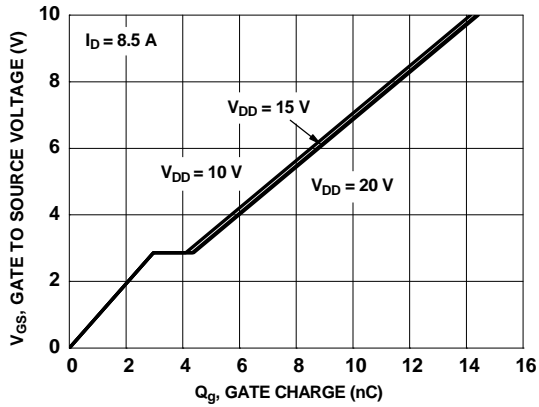
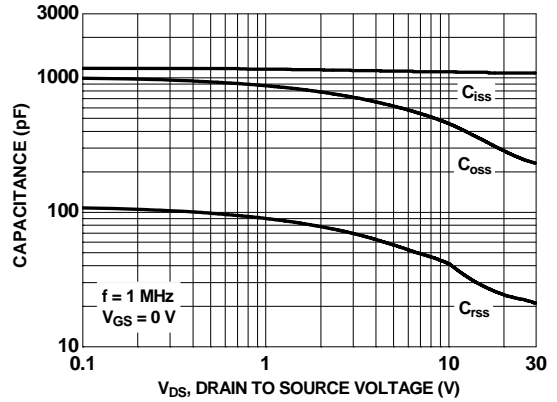


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

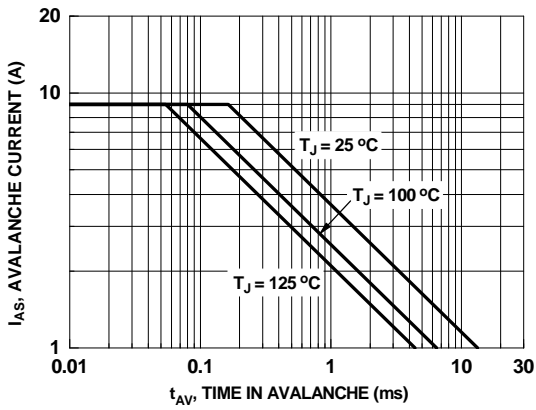
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



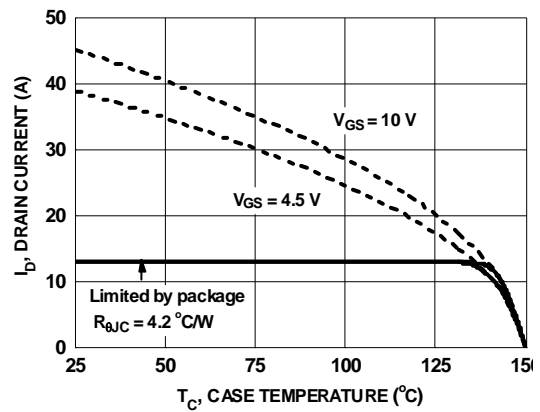
**Figure 20. Gate Charge Characteristics**



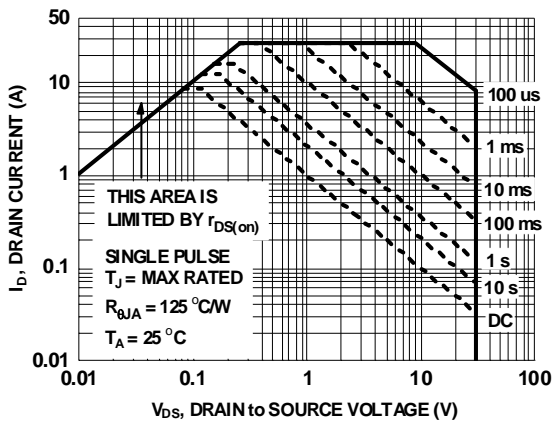
**Figure 21. Capacitance vs. Drain to Source Voltage**



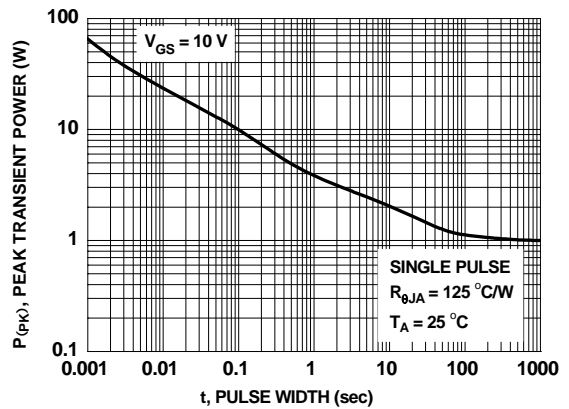
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**



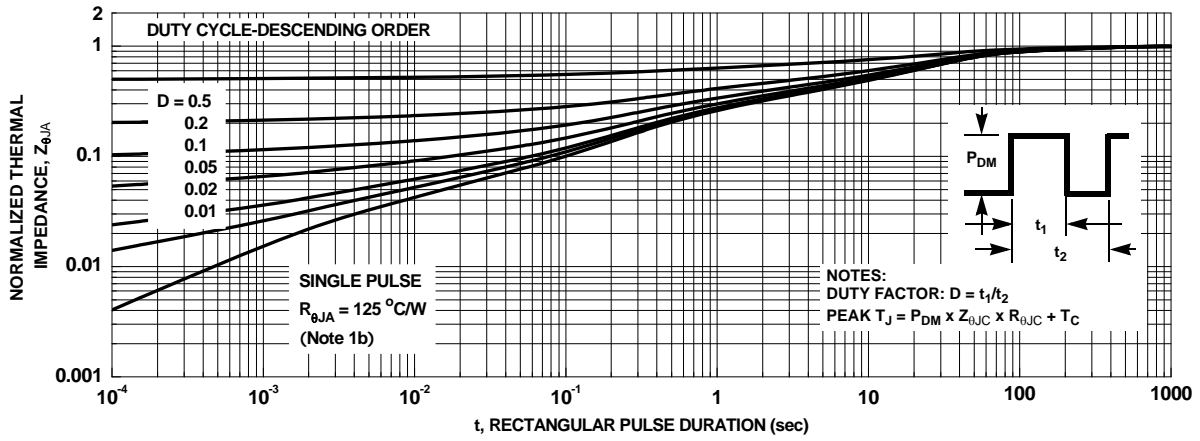
**Figure 24. Forward Bias Safe Operating Area**



**Figure 25. Single Pulse Maximum Power Dissipation**



**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 26. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

### SyncFET<sup>™</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>™</sup> process embeds a Schottky diode in parallel with PowerTrench<sup>®</sup> MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMC7200S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

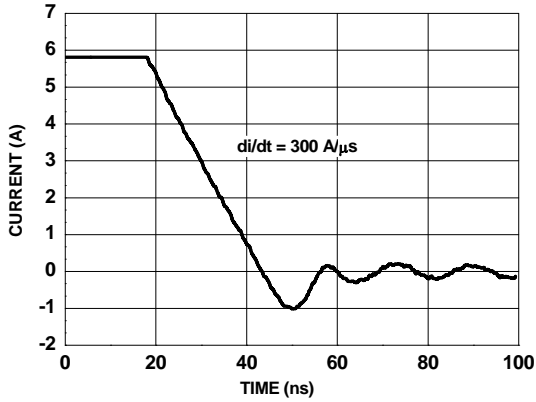


Figure 27. FDMC7200S SyncFET<sup>™</sup> Body Diode Reverse Recovery Characteristic

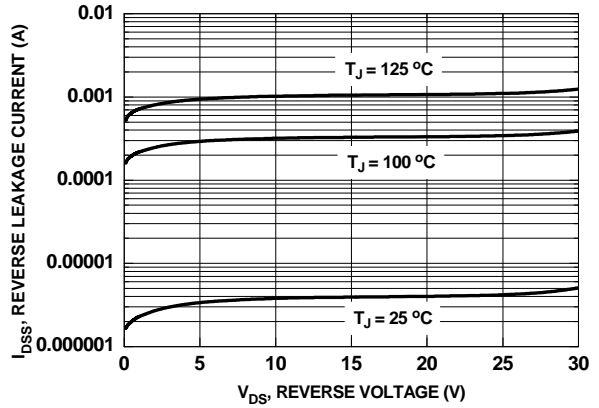
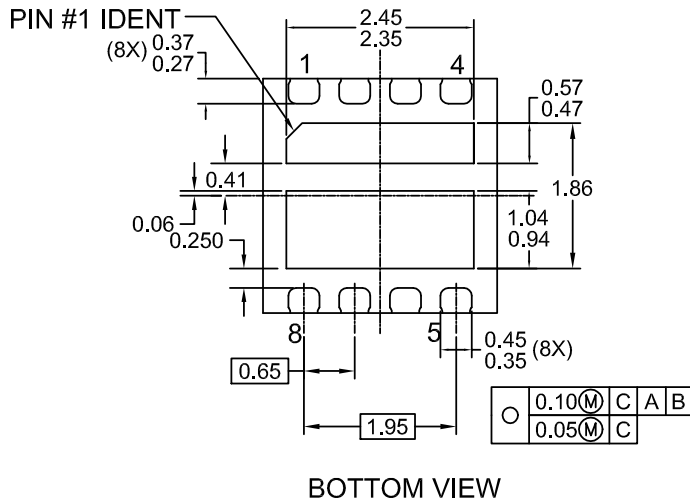
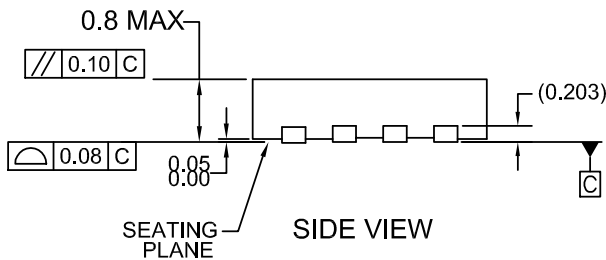
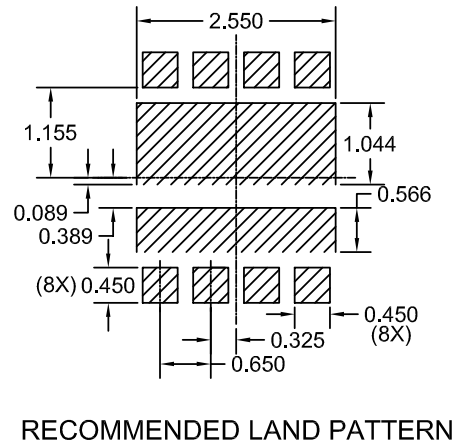
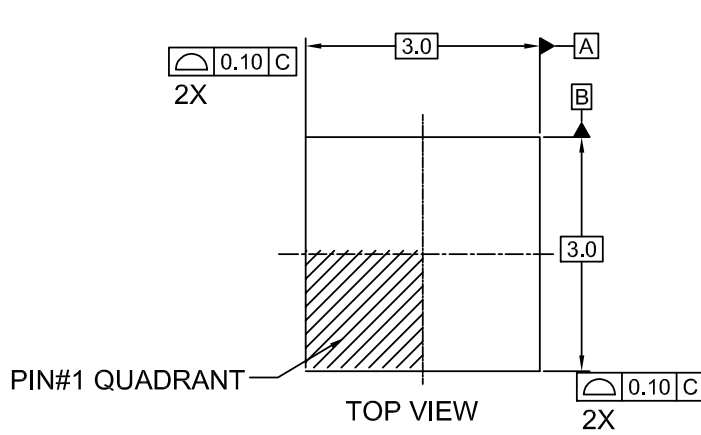


Figure 28. SyncFET<sup>™</sup> Body Diode Reverse Leakage vs. Drain-source Voltage

### Dimensional Outline and Pad Layout



#### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- C. DRAWING FILE NAME : MLP08NREVA






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| FAST®   | OptoHit™  | SuperSOT™-8   | VoltagePlus™  |
| FastvCore™  | OPTOLOGIC®                                      | SupreMOS®   | XST™  |
| FETBench™   | OPTOPLANAR®                                     | SyncFET™  | 仙童™   |
| FPS™  |   | Sync-Lock™  |   |

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