

# FDME1024NZT

## Dual N-Channel PowerTrench® MOSFET

20 V, 3.8 A, 66 mΩ

### Features

- Max  $r_{DS(on)}$  = 66 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 3.4$  A
- Max  $r_{DS(on)}$  = 86 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 2.9$  A
- Max  $r_{DS(on)}$  = 113 mΩ at  $V_{GS} = 1.8$  V,  $I_D = 2.5$  A
- Max  $r_{DS(on)}$  = 160 mΩ at  $V_{GS} = 1.5$  V,  $I_D = 2.1$  A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level > 1600 V (Note 3)
- RoHS Compliant



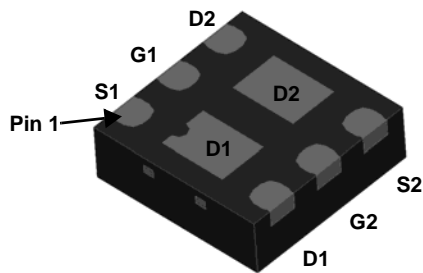
### General Description

This device is designed specifically as a single package solution for dual switching requirement in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses.

The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

### Applications

- Baseband Switch
- Load Switch

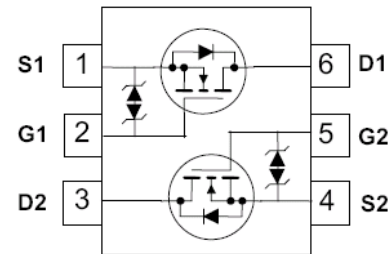


**BOTTOM**



**TOP**

**MicroFET 1.6x1.6 Thin**



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	$\pm 8$	V
$I_D$	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	3.8	A
	-Pulsed	6	
$P_D$	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$ (Note 1a)	1.4	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$ (Note 1b)	0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation)	(Note 1a)	90	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation)	(Note 1b)	195	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
4T	FDME1024NZT	MicroFET 1.6x1.6 <b>Thin</b>	7"	8 mm	5000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		16		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 3.4\text{ A}$		55	66	m $\Omega$
		$V_{GS} = 2.5\text{ V}$ , $I_D = 2.9\text{ A}$		68	86	
		$V_{GS} = 1.8\text{ V}$ , $I_D = 2.5\text{ A}$		85	113	
		$V_{GS} = 1.5\text{ V}$ , $I_D = 2.1\text{ A}$		106	160	
		$V_{GS} = 4.5\text{ V}$ , $I_D = 3.4\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		76	112	
$g_{FS}$	Forward Transconductance	$V_{DD} = 4.5\text{ V}$ , $I_D = 3.4\text{ A}$		9		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		225	300	pF
$C_{oss}$	Output Capacitance			40	55	pF
$C_{rss}$	Reverse Transfer Capacitance			25	40	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		4.5	10	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns
$t_f$	Fall Time			1.7	10	ns
$Q_g$	Total Gate Charge			3	4.2	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 10\text{ V}$ , $I_D = 3.4\text{ A}$ , $V_{GS} = 4.5\text{ V}$		0.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.6		nC

### Drain-Source Diode Characteristics

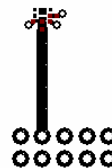
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 0.9\text{ A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 3.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		8.5	17	ns
$Q_{rr}$	Reverse Recovery Charge			1.4	10	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 90  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

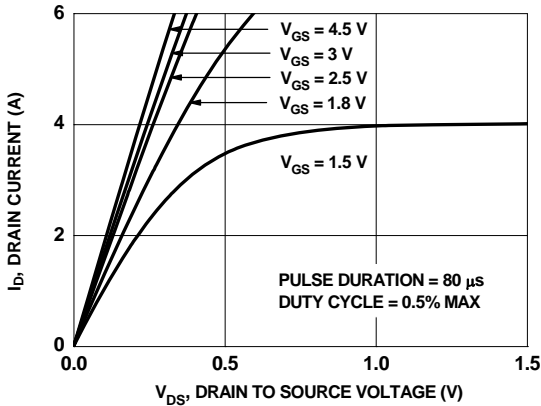


b. 195  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

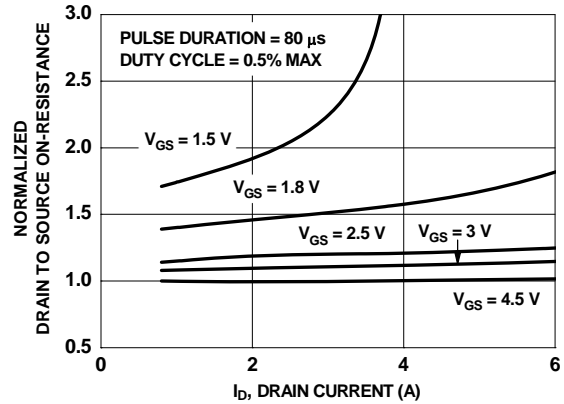
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

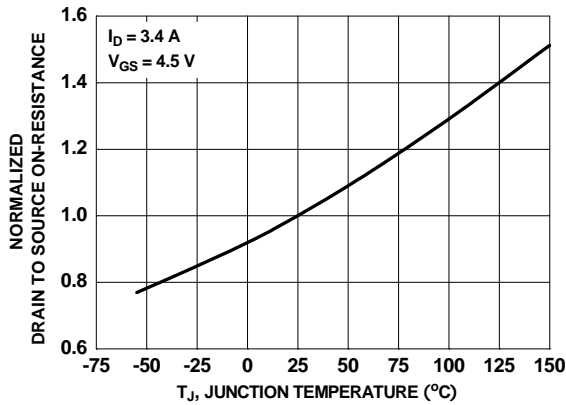
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



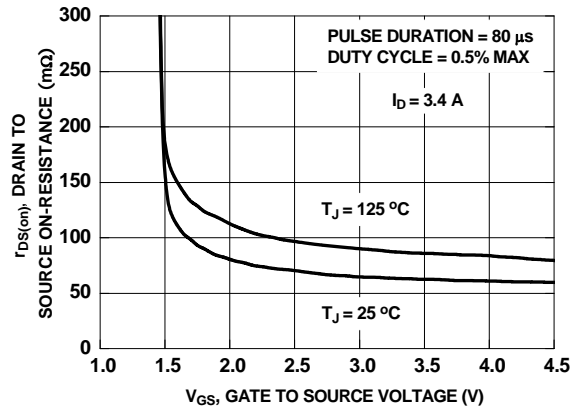
**Figure 1. On-Region Characteristics**



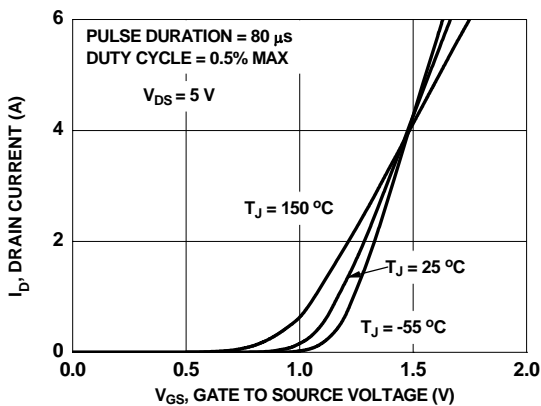
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



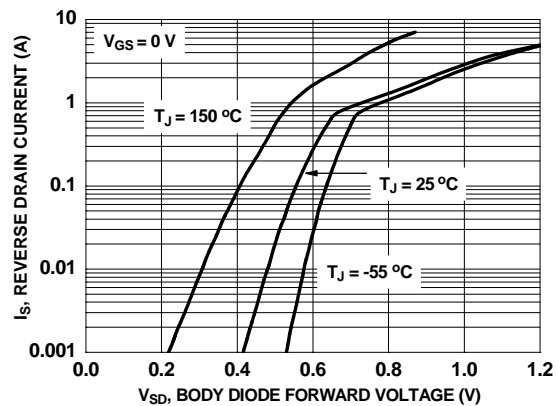
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

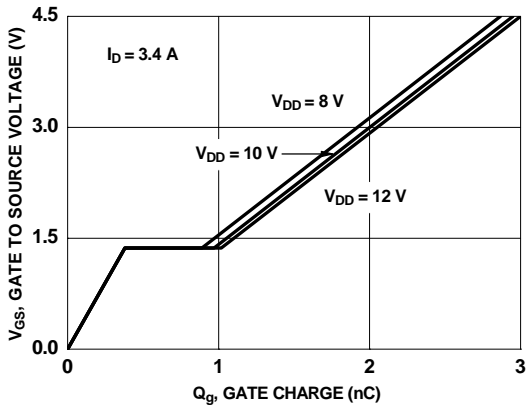


**Figure 5. Transfer Characteristics**

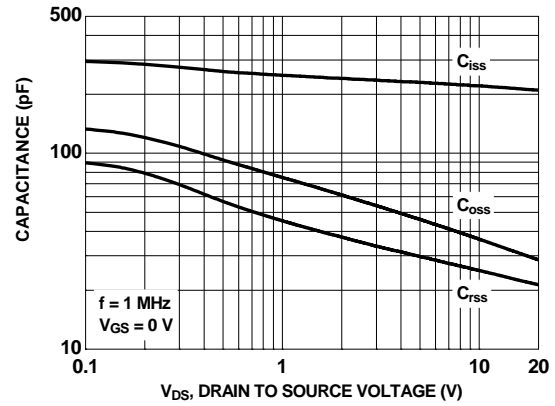


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

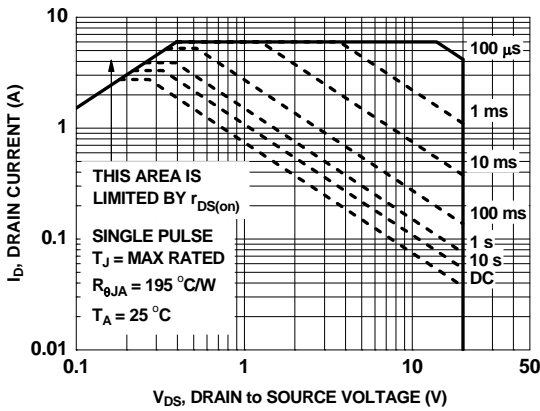
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



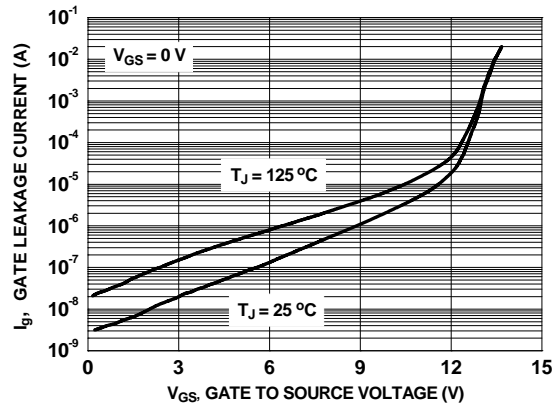
**Figure 7. Gate Charge Characteristics**



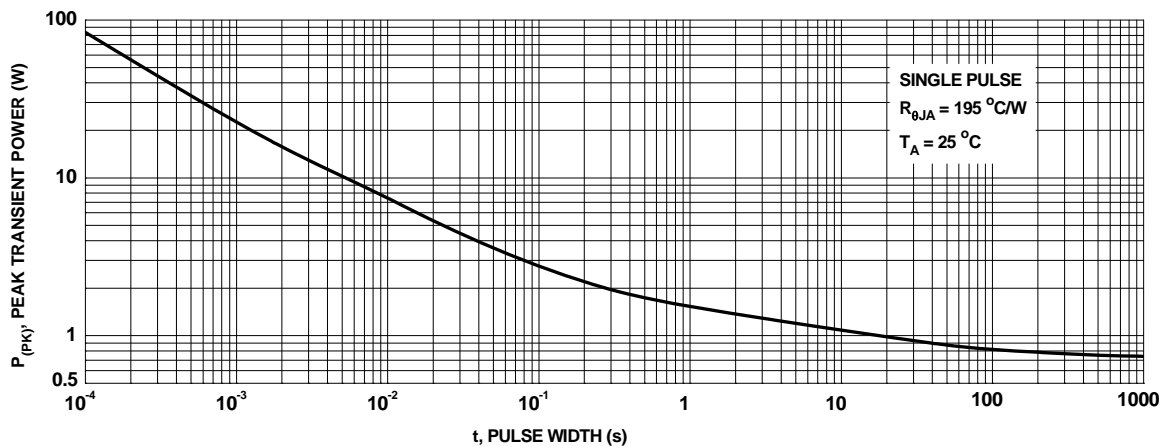
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

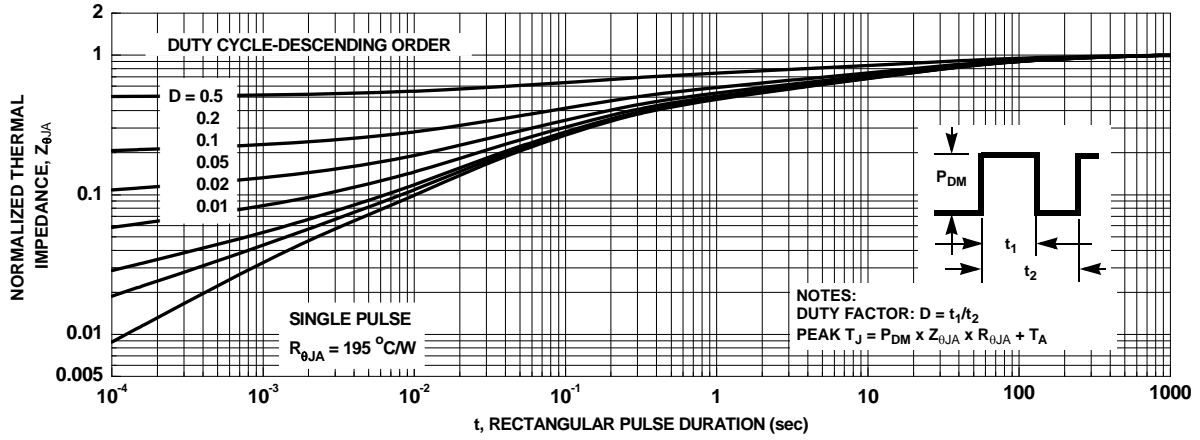


**Figure 10. Gate Leakage Current vs Gate to Source Voltage**



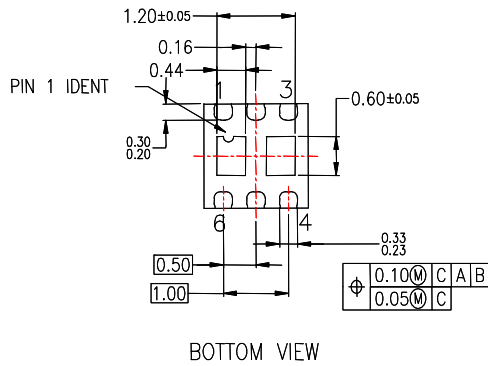
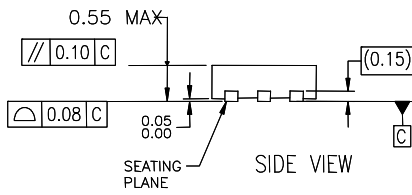
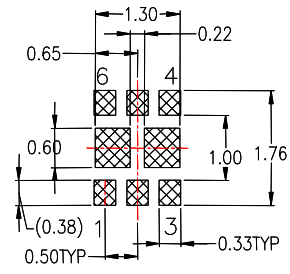
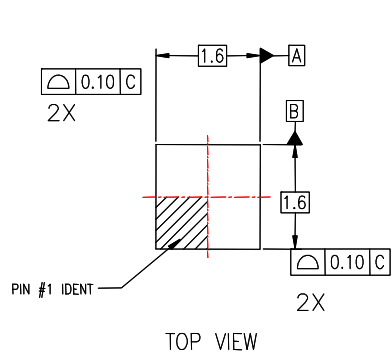
**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout





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