



January 2015

# FDMS0310S

## N-Channel PowerTrench<sup>®</sup> SyncFET<sup>™</sup>

30 V, 42 A, 4 mΩ

### Features

- Max  $r_{DS(on)}$  = 4.0 mΩ at  $V_{GS} = 10$  V,  $I_D = 18$  A
- Max  $r_{DS(on)}$  = 5.2 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 14$  A
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- SyncFET<sup>™</sup> Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

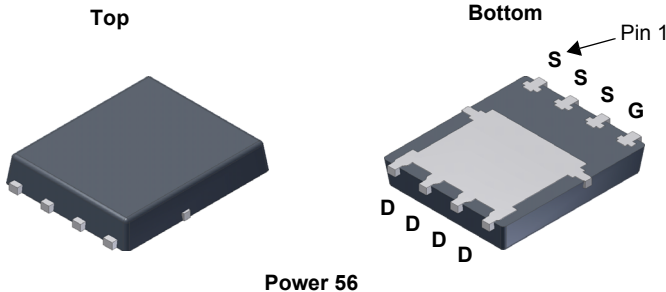


### General Description

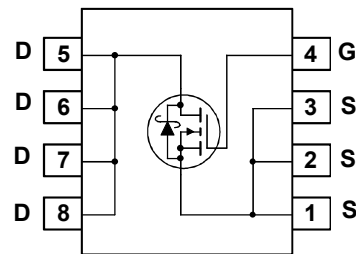
The FDMS0310S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

### Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU low side switch
- Networking Point of Load low side switch
- Desktop



Power 56



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{DSt}$	Drain to Source Transient Voltage ( $t_{\text{Transient}} < 100$ ns)	33	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	42	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	83	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	19	
	-Pulsed	90	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	60	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	46	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS0310S	FDMS0310S	Power 56	13 "	12 mm	3000 units

FDMS0310S N-Channel PowerTrench<sup>®</sup> SyncFET<sup>™</sup>

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25^\circ\text{C}$		18		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.2	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25^\circ\text{C}$		-5		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}$		3.2	4.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$		4.3	5.2	
		$V_{GS} = 10\text{ V}, I_D = 18\text{ A}, T_J = 125^\circ\text{C}$		4.1	5.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 18\text{ A}$		97		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		2120	2820	pF
$C_{oss}$	Output Capacitance			735	975	pF
$C_{rss}$	Reverse Transfer Capacitance			90	135	pF
$R_g$	Gate Resistance			1.1	2.2	$\Omega$

### Switching Characteristics

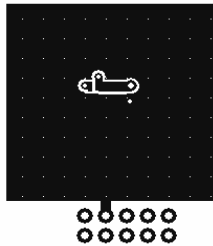
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		12	21	ns	
$t_r$	Rise Time			5	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			28	44	ns	
$t_f$	Fall Time			4	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		33	46	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$		15	22	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 15\text{ V},$ $I_D = 18\text{ A}$		6.5		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			4.0		nC	

### Drain-Source Diode Characteristics

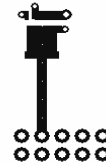
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.48	0.7	V
		$V_{GS} = 0\text{ V}, I_S = 18\text{ A}$ (Note 2)		0.80	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 18\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		26	42	ns
$Q_{rr}$	Reverse Recovery Charge			26	42	nC

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



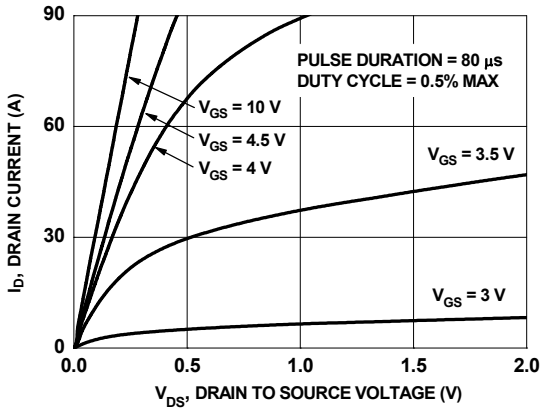
a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



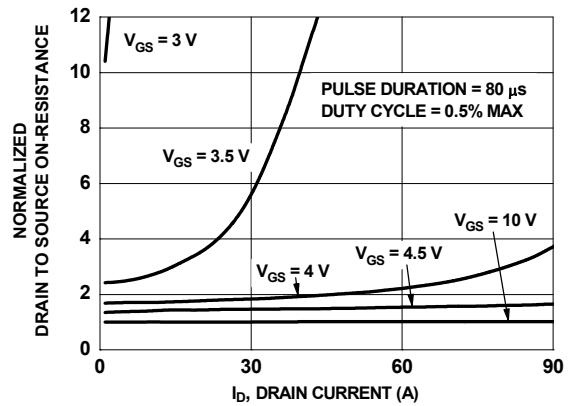
b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width  $< 300\ \mu\text{s}$ , Duty cycle  $< 2.0\%$ .
- $E_{AS}$  of 60 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 11\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ , 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 16\text{ A}$ .
- As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

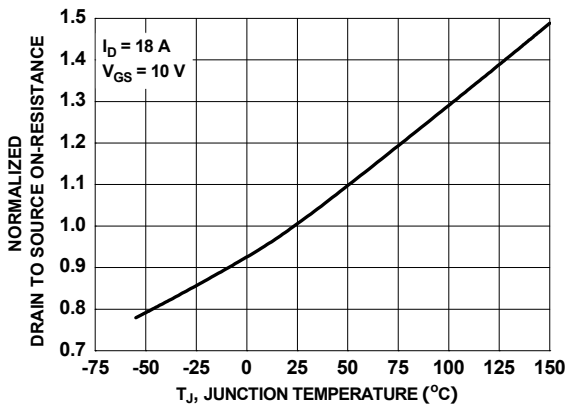
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



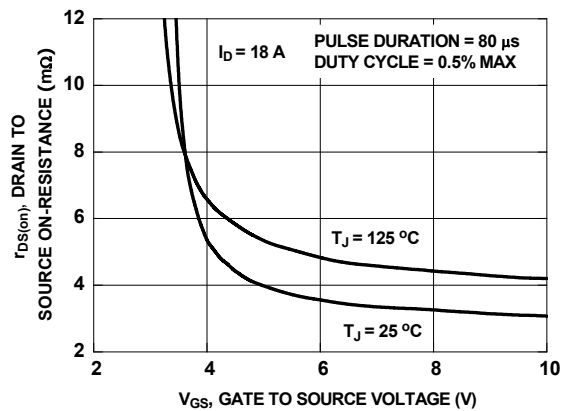
**Figure 1. On-Region Characteristics**



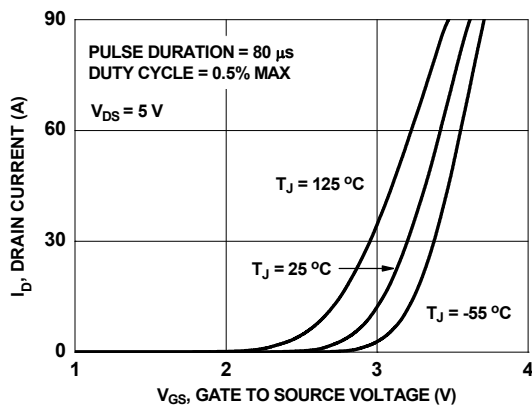
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



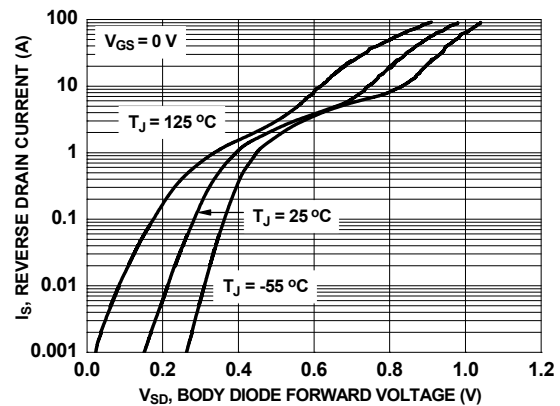
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

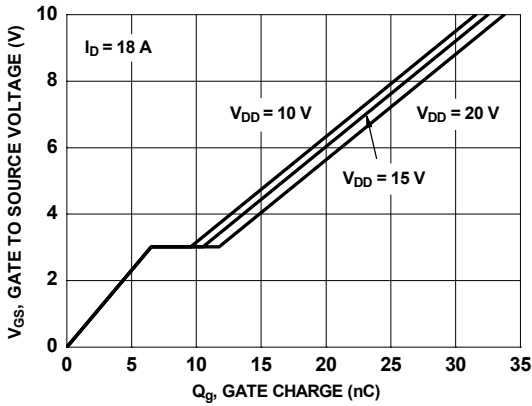


**Figure 5. Transfer Characteristics**

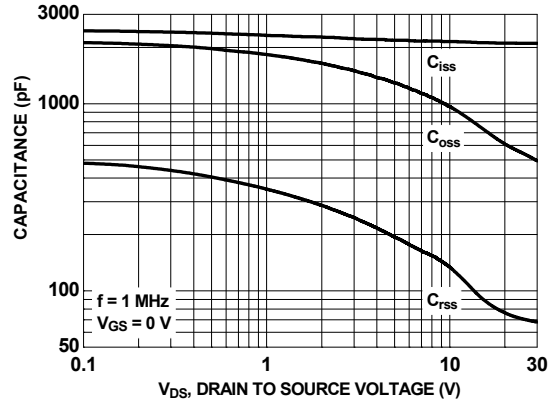


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

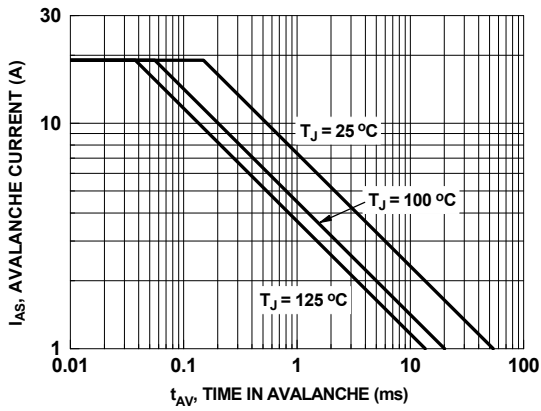
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



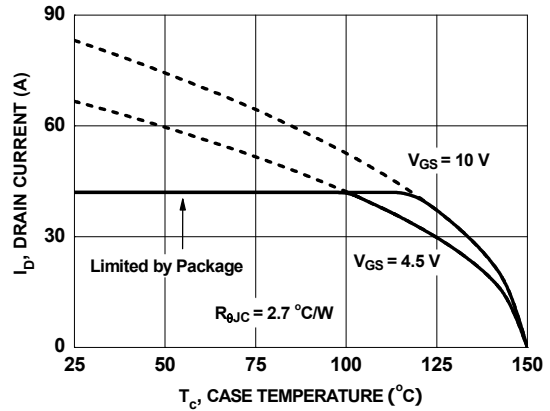
**Figure 7. Gate Charge Characteristics**



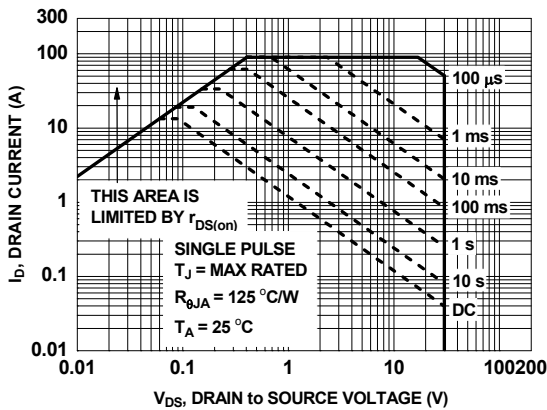
**Figure 8. Capacitance vs Drain to Source Voltage**



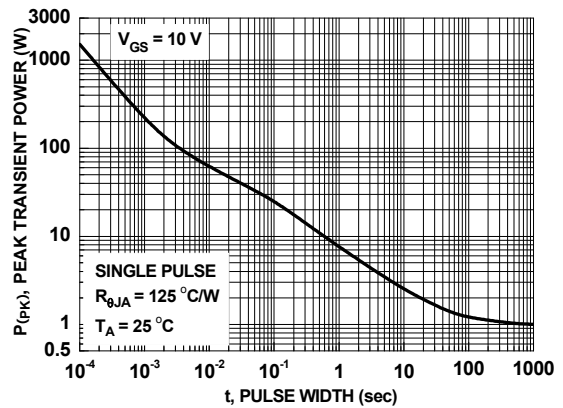
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

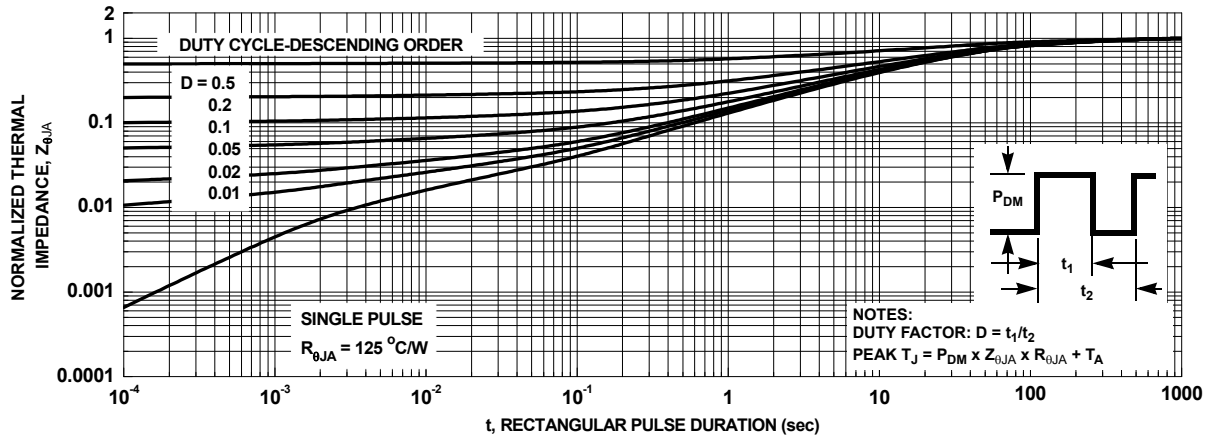


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

### SyncFET<sup>™</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>™</sup> process embeds a Schottky diode in parallel with PowerTrench MoSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS0310S.

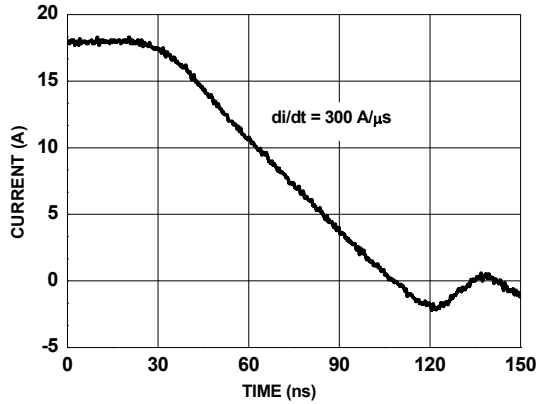


Figure 14. FDMS0310S SyncFET<sup>™</sup> body diode reverse recovery characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

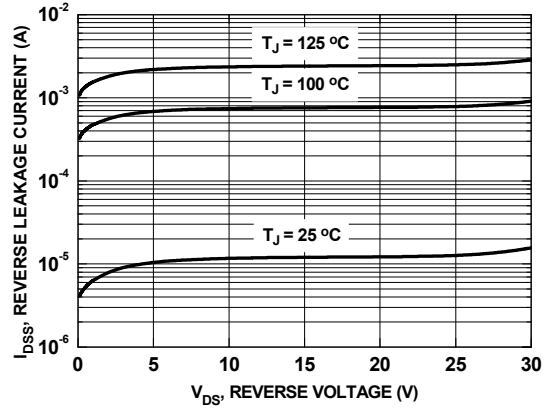
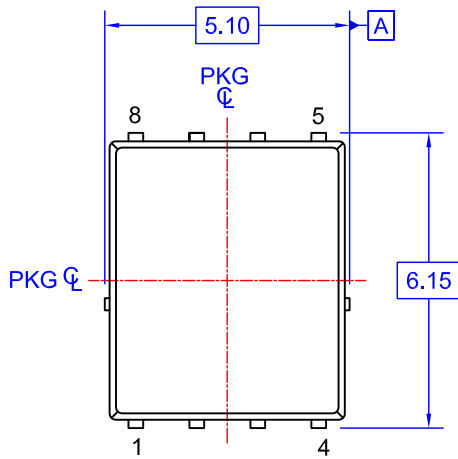
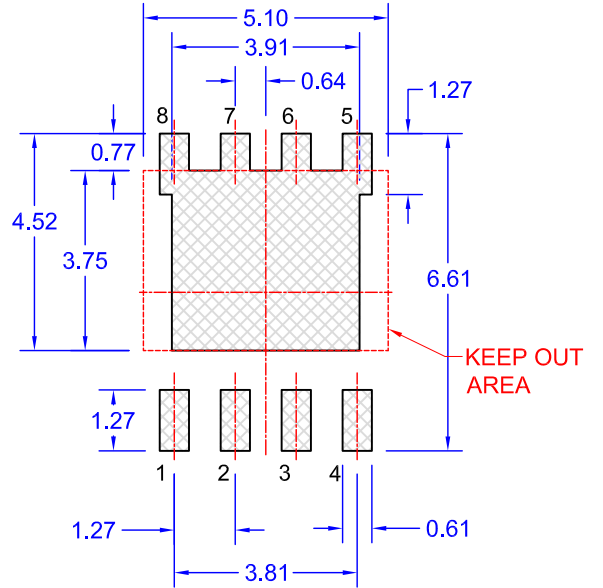
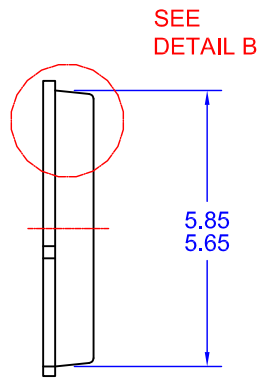


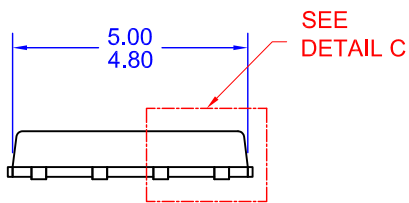
Figure 15. SyncFET<sup>™</sup> body diode reverse leakage versus drain-source voltage



TOP VIEW

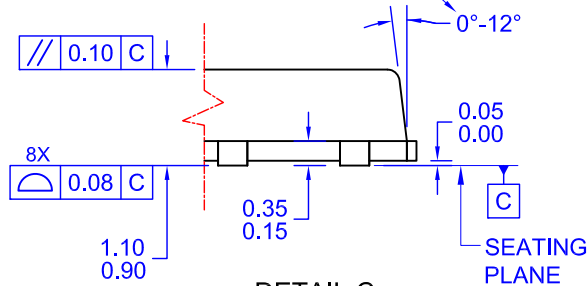


LAND PATTERN RECOMMENDATION

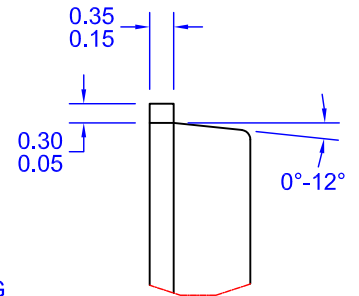


SIDE VIEW

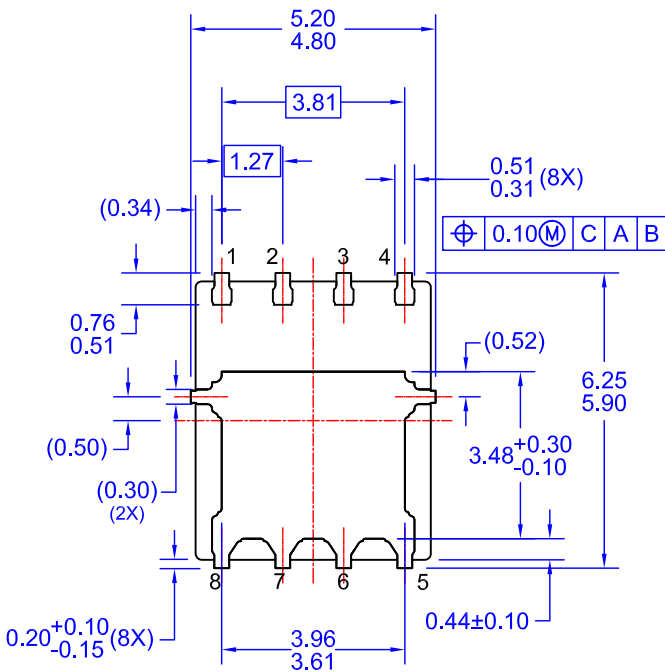
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- DRAWING FILE NAME: PQFN08AREV10





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| EfficientMax™            | MicroPak™                                      | SPM®                                  | Ultra FRFET™     |
| ESBC™                    | MicroPak2™                                     | STEALTH™                              | UniFET™          |
| F <sup>®</sup>           | MillerDrive™                                   | SuperFET®                             | VCX™             |
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| Fairchild Semiconductor® | MotionGrid®                                    | SuperSOT™-6                           | VoltagePlus™     |
| FACT Quiet Series™       | MTi®   | SuperSOT™-8                           | XST™             |
| FACT®                    | MTx®   | SupreMOS®                             | Xsens™           |
| FastvCore™               | MVN®   | SyncFET™                              | 仙童®              |
| FETBench™                | mWSaver®                                       | Sync-Lock™                            |                  |
| FPS™                     | OptoHiT™                                       |                                       |                  |
|                          | OPTOLOGIC®                                     |                                       |                  |

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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