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# FDMS8050ET30

## N-Channel PowerTrench<sup>®</sup> MOSFET

30 V, 423 A, 0.65 mΩ

### Features

- Extended T<sub>J</sub> rating to 175°C
- Max r<sub>DS(on)</sub> = 0.65 mΩ at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 55 A
- Max r<sub>DS(on)</sub> = 0.9 mΩ at V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 47 A
- Advanced Package and Silicon combination for low r<sub>DS(on)</sub> and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

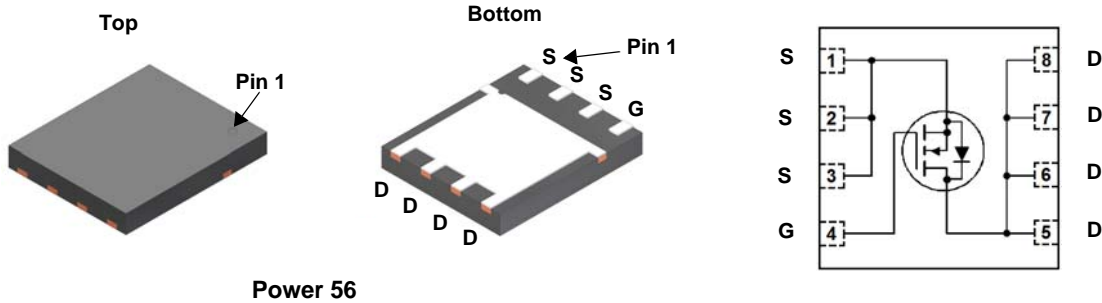


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge and extremely low r<sub>DS(on)</sub>.

### Applications

- OringFET
- Synchronous Rectifier



Power 56

### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Rated	Units
V <sub>DS</sub>	Drain to Source Voltage	30	V
V <sub>GS</sub>	Gate to Source Voltage (Note 4)	±20	V
I <sub>D</sub>	Drain Current -Continuous T <sub>C</sub> = 25 °C (Note 6)	423	A
	-Continuous T <sub>C</sub> = 100 °C (Note 6)	299	
	-Continuous T <sub>A</sub> = 25 °C (Note 1a)	55	
	-Pulsed (Note 5)	1914	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 3)	1536	mJ
P <sub>D</sub>	Power Dissipation T <sub>C</sub> = 25 °C	180	W
	Power Dissipation T <sub>A</sub> = 25 °C (Note 1a)	3.3	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +175	°C

### Thermal Characteristics

R <sub>θJC</sub>	Thermal Resistance, Junction to Case	0.83	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1a)	45	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8050ET	FDMS8050ET30	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 750\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 750\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		20		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 750\text{ }\mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 750\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 55\text{ A}$		0.5	0.65	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 47\text{ A}$		0.7	0.9	
		$V_{GS} = 10\text{ V}, I_D = 55\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.7	0.9	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 55\text{ A}$		333		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		16150	22610	pF
$C_{oss}$	Output Capacitance			4455	6240	pF
$C_{rss}$	Reverse Transfer Capacitance			220	310	pF
$R_g$	Gate Resistance			1.0	3.0	$\Omega$

### Switching Characteristics

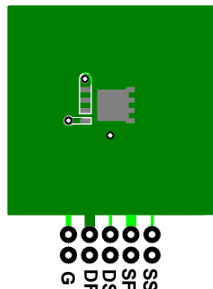
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 55\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		29	47	ns	
$t_r$	Rise Time			22	36	ns	
$t_{d(off)}$	Turn-Off Delay Time			87	139	ns	
$t_f$	Fall Time			16	28	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		204	285	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 15\text{ V},$ $I_D = 55\text{ A}$	93	130	nC
$Q_{gs}$	Gate to Source Charge			41		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			18		nC	

### Drain-Source Diode Characteristics

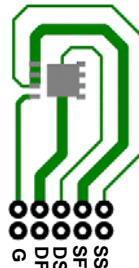
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.2\text{ A}$ (Note 2)		0.64	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 55\text{ A}$ (Note 2)		0.74	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 55\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		77	124	ns
$Q_{rr}$	Reverse Recovery Charge			141	226	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a.  $45\text{ }^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b.  $115\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 1536 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 32\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$ , 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 69\text{ A}$ .

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied

5. Pulse Id please refer to Fig.11 SOA curve for detail.

6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

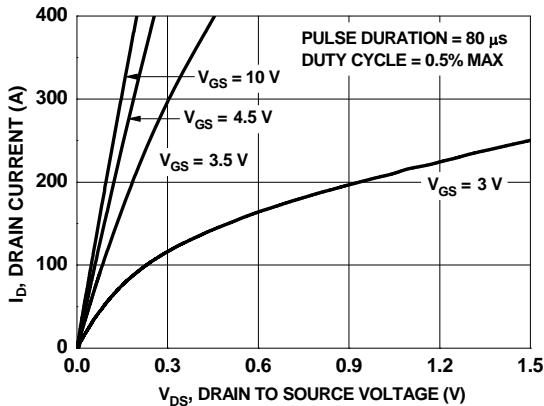


Figure 1. On-Region Characteristics

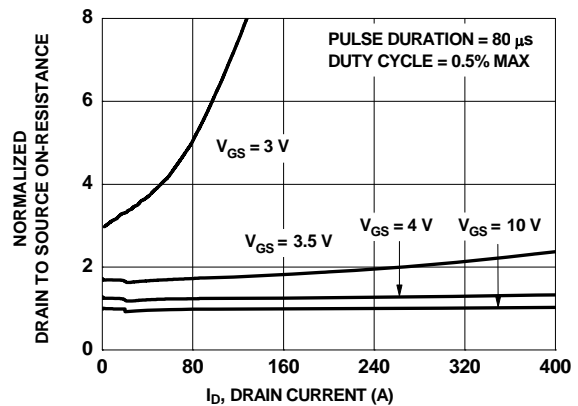


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

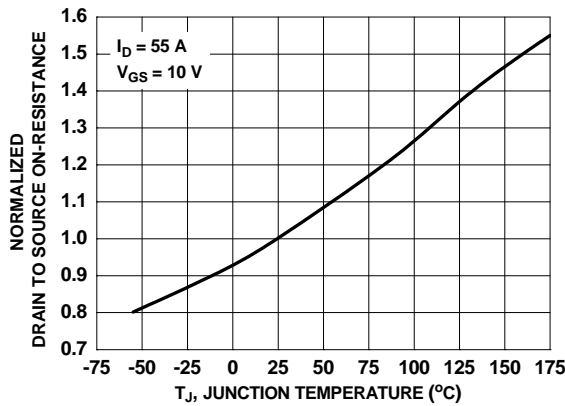


Figure 3. Normalized On-Resistance vs Junction Temperature

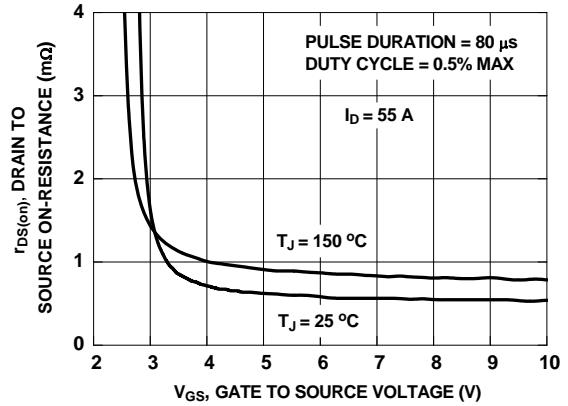


Figure 4. On-Resistance vs Gate to Source Voltage

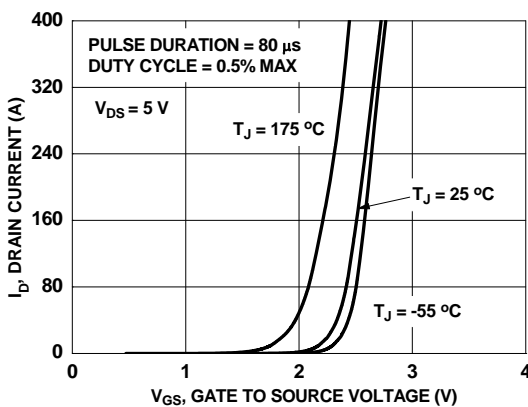


Figure 5. Transfer Characteristics

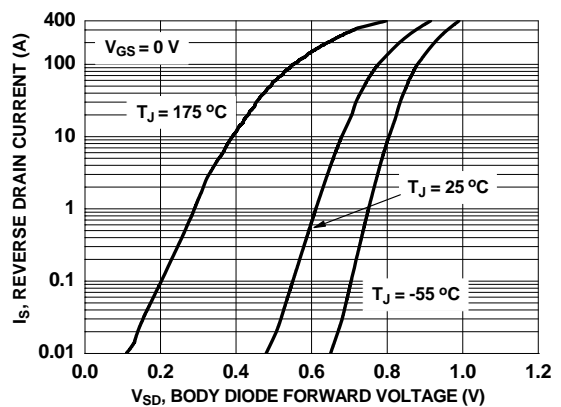
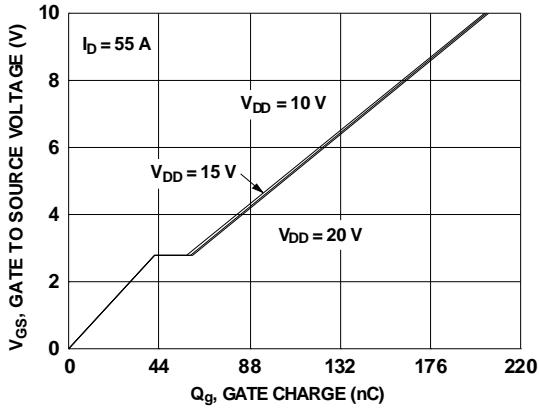
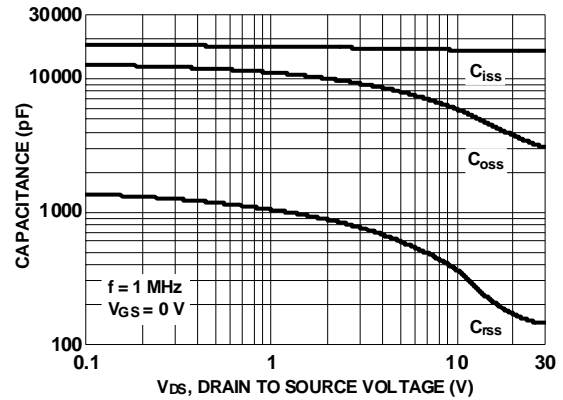


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

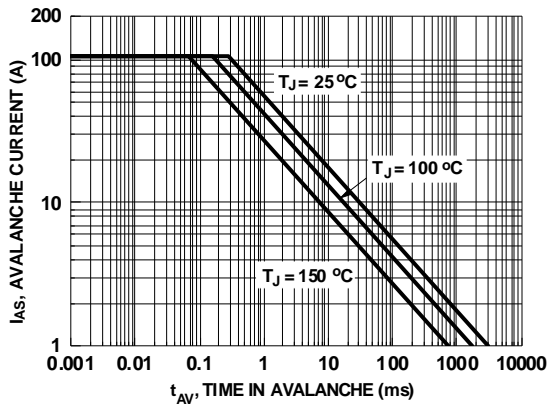
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



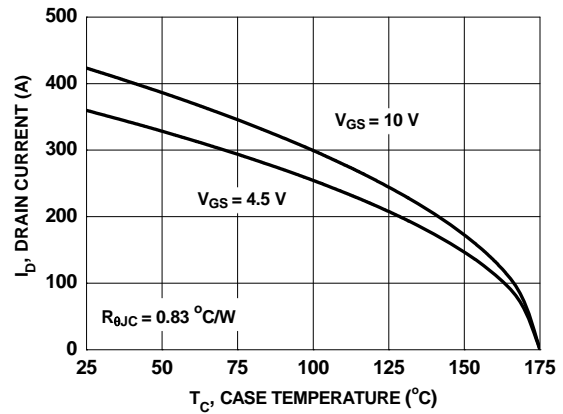
**Figure 7. Gate Charge Characteristics**



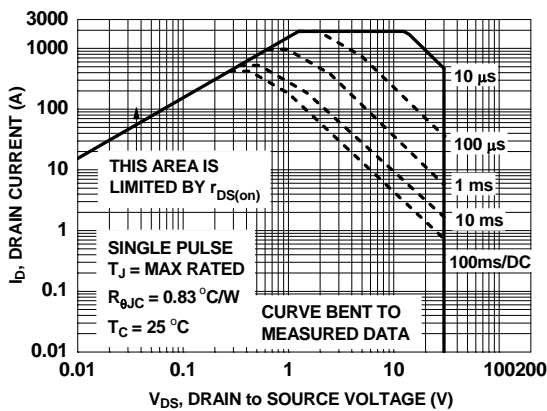
**Figure 8. Capacitance vs Drain to Source Voltage**



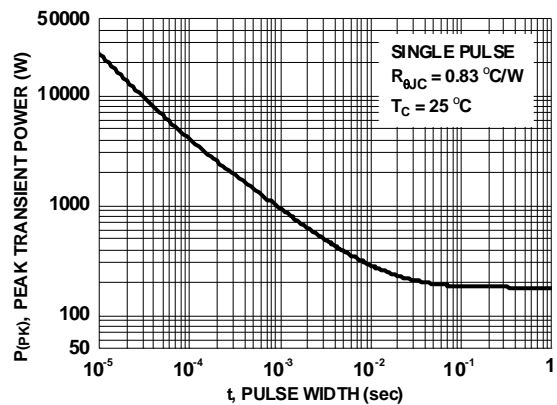
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

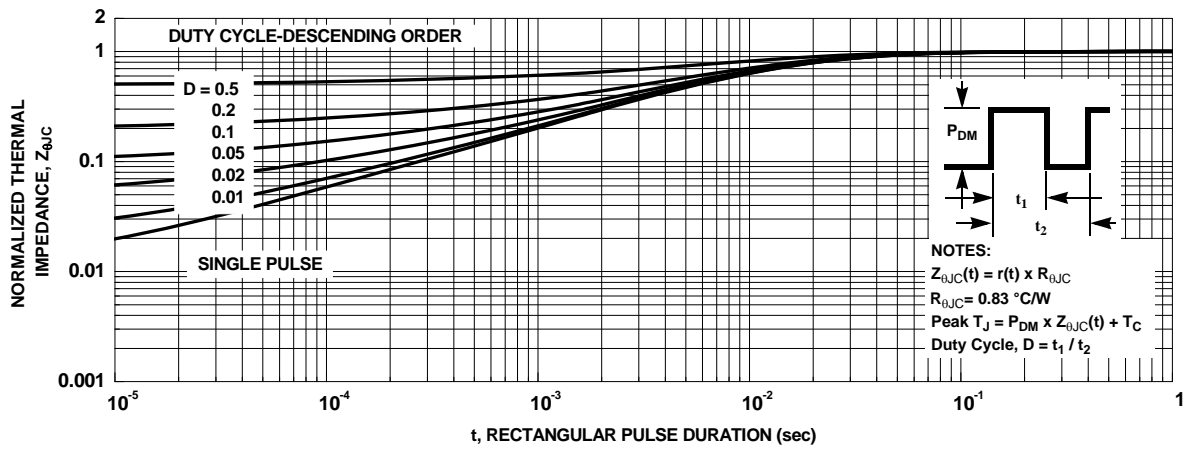


**Figure 11. Forward Bias Safe Operating Area**

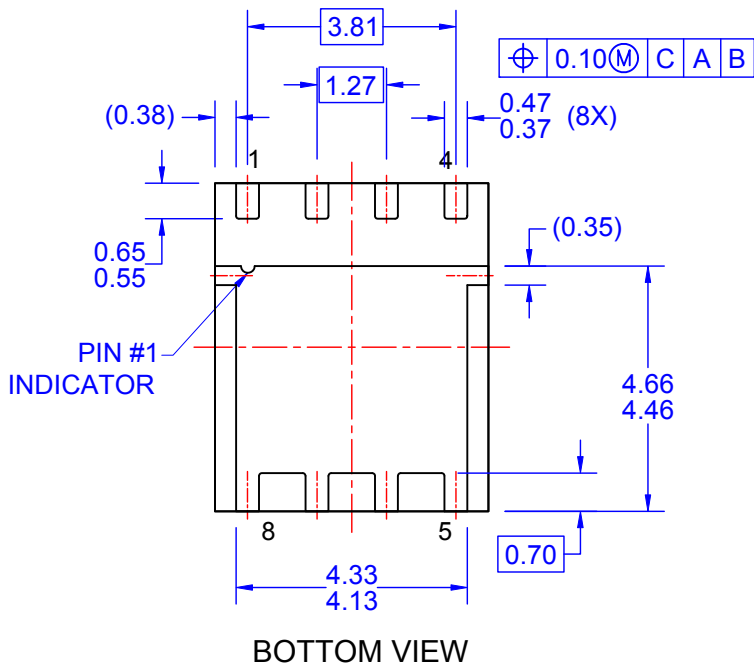
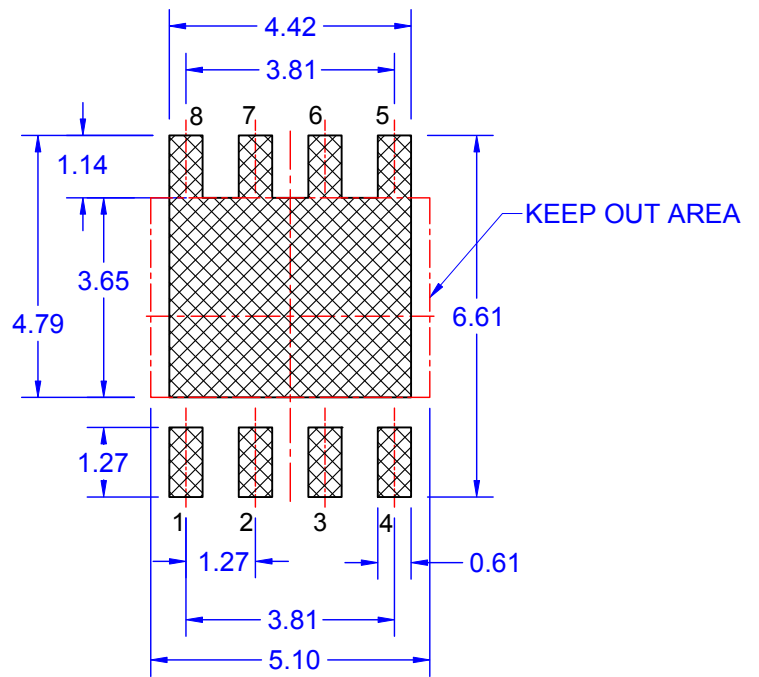
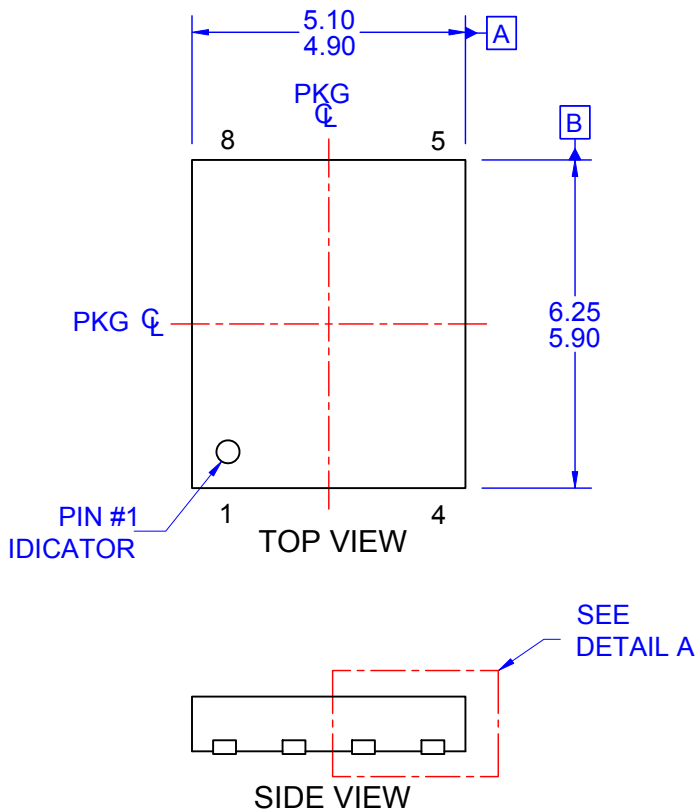


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08JREV3.



**DETAIL A**  
SCALE: 2:1





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