FAIRCHILD SEMICONDUCTOR®

November 2013

# FDP023N08B

## N-Channel PowerTrench® MOSFET

**75 V, 242 A, 2.35 mΩ**

### Features

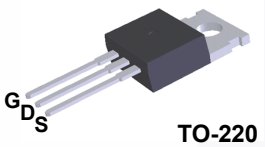
- $R_{DS(on)}$ = 1.96 mΩ ( Typ.) @ $V_{GS}$ = 10 V, $I_D$ = 75 A
- Low FOM $R_{DS(on)}$*$Q_G$
- Low Reverse Recovery Charge, $Q_{rr}$
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

### Description

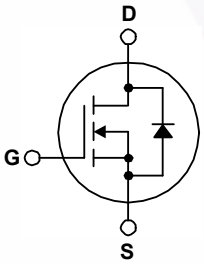
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- DC motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverte




TO-220




### MOSFET Maximum Ratings $T_C$ = 25°C unless otherwise noted.

| Symbol | Parameter | | FDP023N08B_F102 | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | 75 | V |
| $V_{GSS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C, Silicon Limited) | 242* | A |
| | | - Continuous ($T_C$ = 100°C, Silicon Limited) | 171* | |
| | | - Continuous ($T_C$ = 25°C, Package Limited) | 120 | |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | 968 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 961 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 6 | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | 245 | W |
| | | - Derate Above 25°C | 1.64 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +175 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds | | 300 | °C |

* Package limitation current is 120A.

### Thermal Characteristics

| Symbol | Parameter | FDP023N08B_F102 | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | 0.61 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max. | 62.5 | |

## Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|---|
| FDP023N08B_F102 | FDP023N08B | TO-220 | Tube | N/A | N/A | 50 units |

## Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0V, $T_C = 25^oC$ | 75 | - | - | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to $25^oC$ | - | 0.35 | - | V/$^o$C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 60 V, $T_C = 150^oC$ | - | - | 500 | |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.0 | - | 3.8 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 75 A | - | 1.96 | 2.35 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 75 A | - | 185 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 37.5 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 10350 | 13765 | pF |
| $C_{oss}$ | Output Capacitance | | - | 1855 | 2465 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 46.8 | - | pF |
| $C_{oss(er)}$ | Energy Related Output Capacitance | $V_{DS}$ = 37.5 V, $V_{GS}$ = 0 V | - | 3290 | - | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS}$ = 37.5 V, $I_D$ = 100 A, $V_{GS}$ = 10 V (Note 4) | - | 150 | 195 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 50.3 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 31.7 | - | nC |
| $V_{plateau}$ | Gate Plateau Volatge | | - | 4.9 | - | V |
| $Q_{sync}$ | Total Gate Charge Sync. | $V_{DS}$ = 0 V, $I_D$ = 50 A | - | 127.4 | - | nC |
| $Q_{oss}$ | Output Charge | $V_{DS}$ = 37.5 V, $V_{GS}$ = 0 V | - | 146.2 | - | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 37.5 V, $I_D$ = 100 A, $V_{GS}$ = 10 V, $R_G$ = 4.7 Ω (Note 4) | - | 41 | 92 | ns |
| $t_r$ | Turn-On Rise Time | | - | 71 | 151 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 111 | 232 | ns |
| $t_f$ | Turn-Off Fall Time | | - | 56 | 122 | ns |
| ESR | Equivalent Series Resistance (G-S) | f = 1 MHz | - | 2.23 | - | Ω |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 242* | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 968 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 75 A | - | - | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $V_{DD}$=37.5 V, $I_{SD}$ = 100 A, $dI_F/dt$ = 100 A/μs | - | 79.3 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 114 | - | nC |

**Notes:**

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 3 mH, $I_{AS}$ = 25.32 A, starting $T_J = 25°C$.
3. $I_{SD} \le 100$ A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting $T_J = 25°C$.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

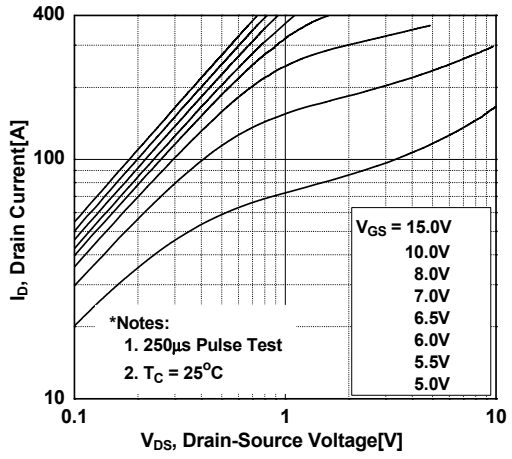



**Figure 2. Transfer Characteristics**

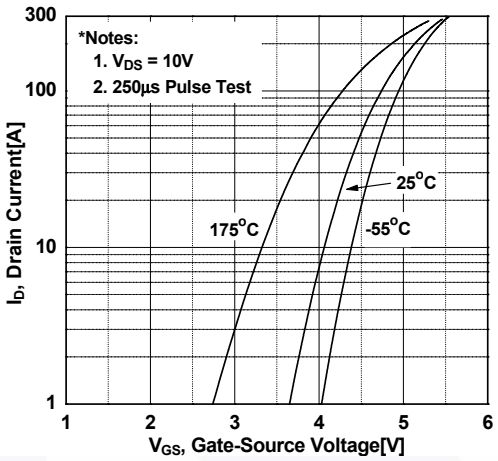



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

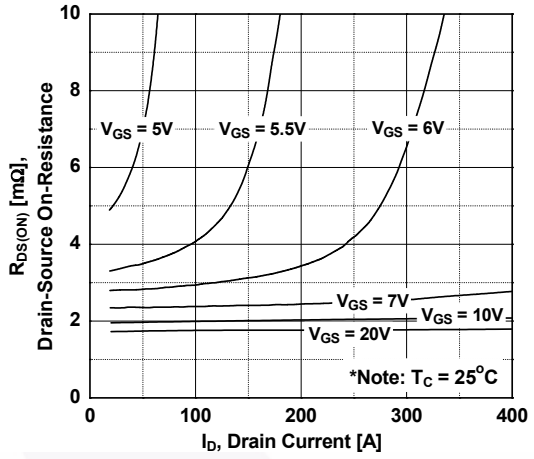



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

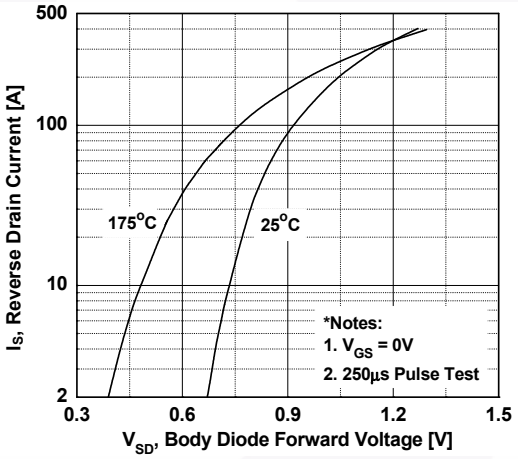



**Figure 5. Capacitance Characteristics**

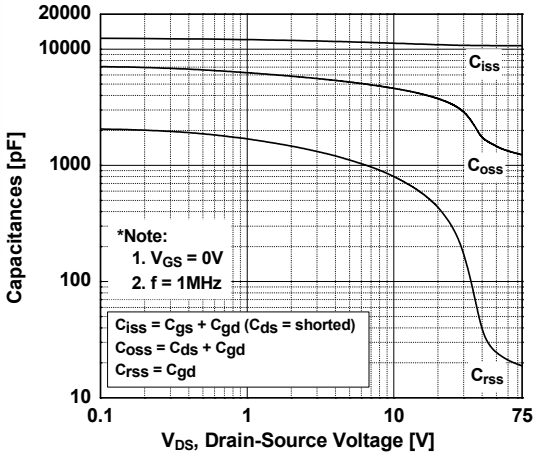
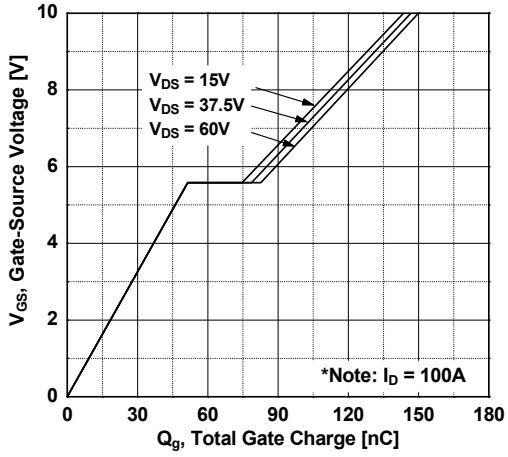



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

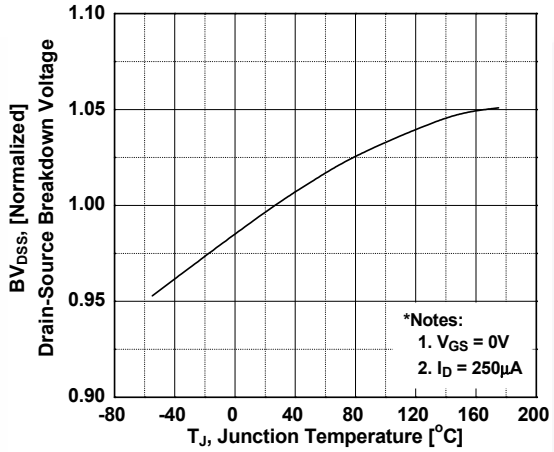



**Figure 8. On-Resistance Variation vs. Temperature**

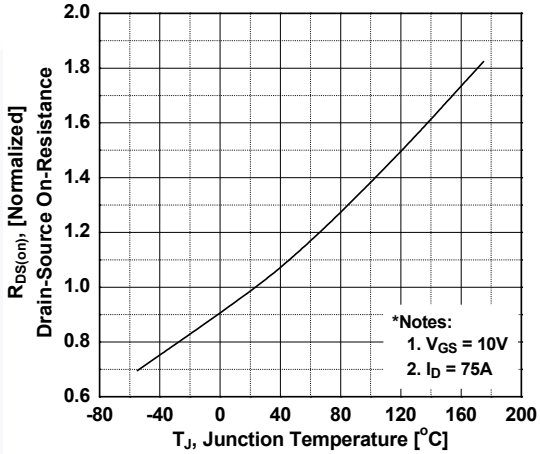



**Figure 9. Maximum Safe Operating Area**

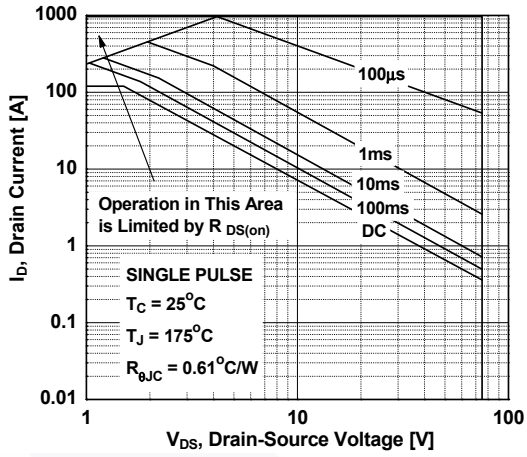



**Figure 10. Maximum Drain Current vs. Case Temperature**

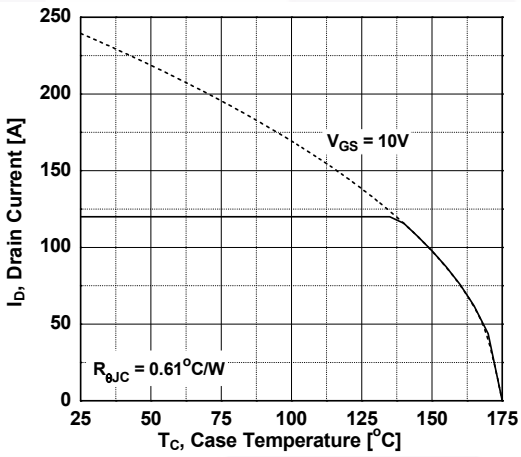



**Figure 11. Eoss vs. Drain to Source Voltage**

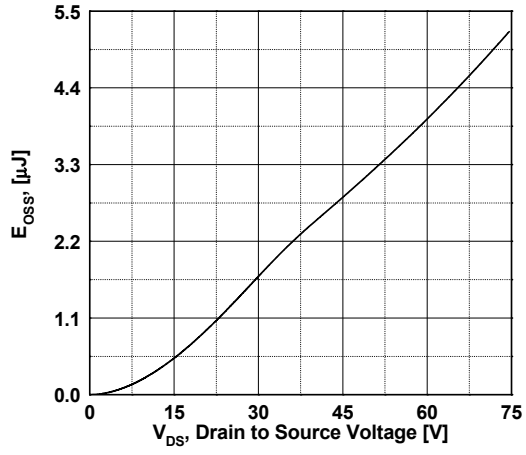
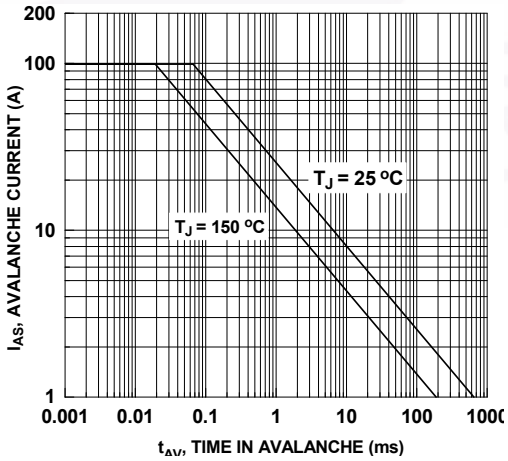
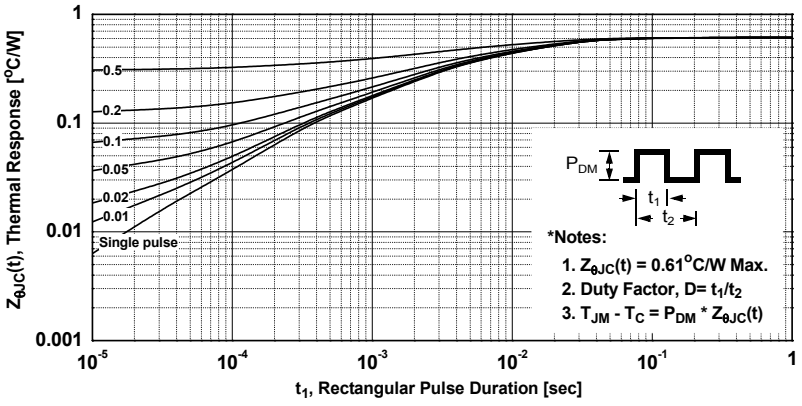



**Figure 12. Unclamped Inductive Switching Capability**



## Typical Performance Characteristics (Continued)

**Figure 13. Transient Thermal Response Curve**



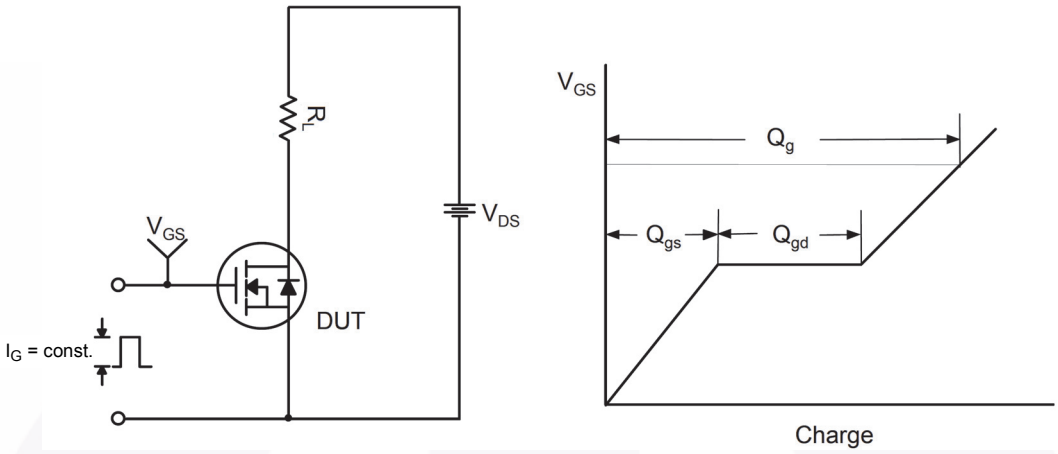



**Figure 14. Gate Charge Test Circuit & Waveform**

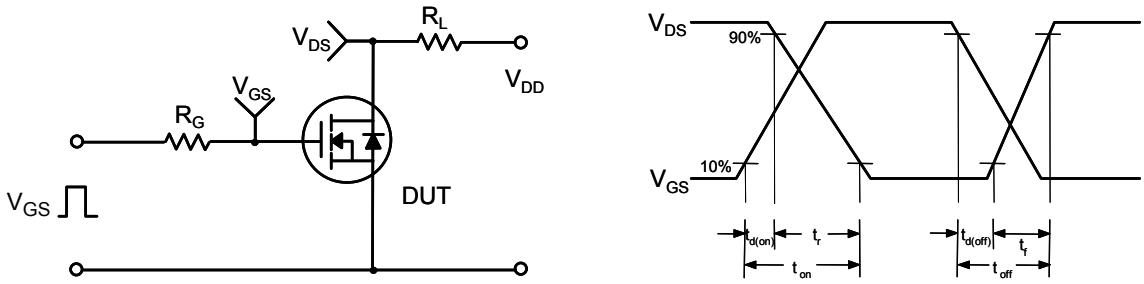



**Figure 15. Resistive Switching Test Circuit & Waveforms**

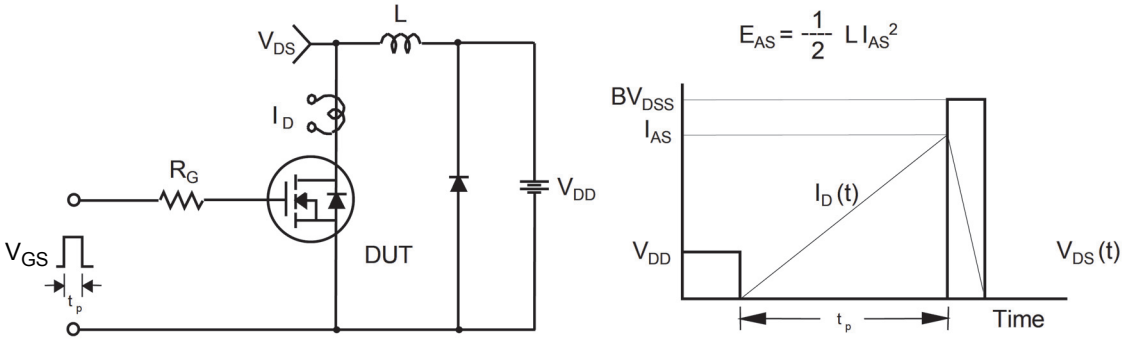



**Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms**

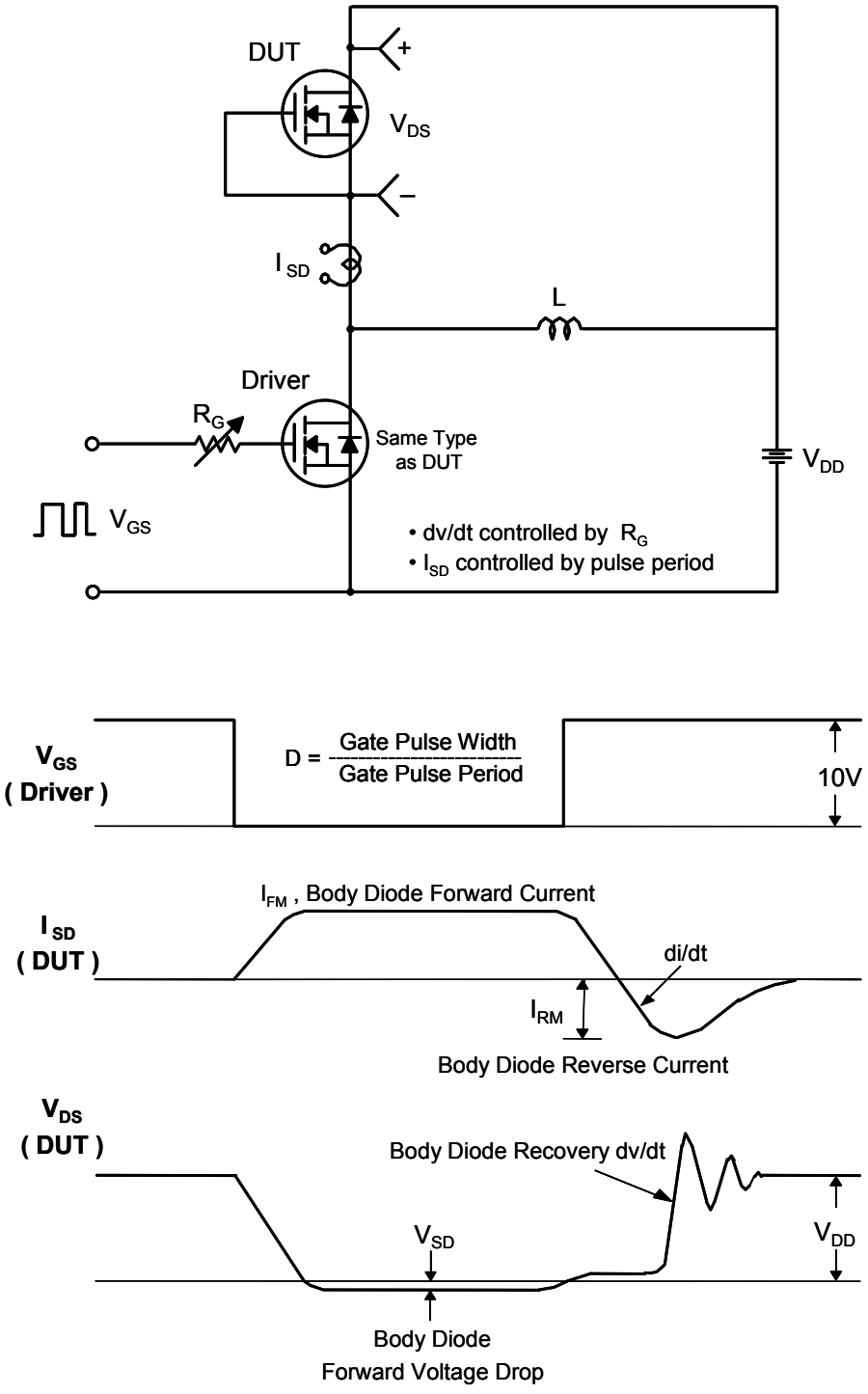
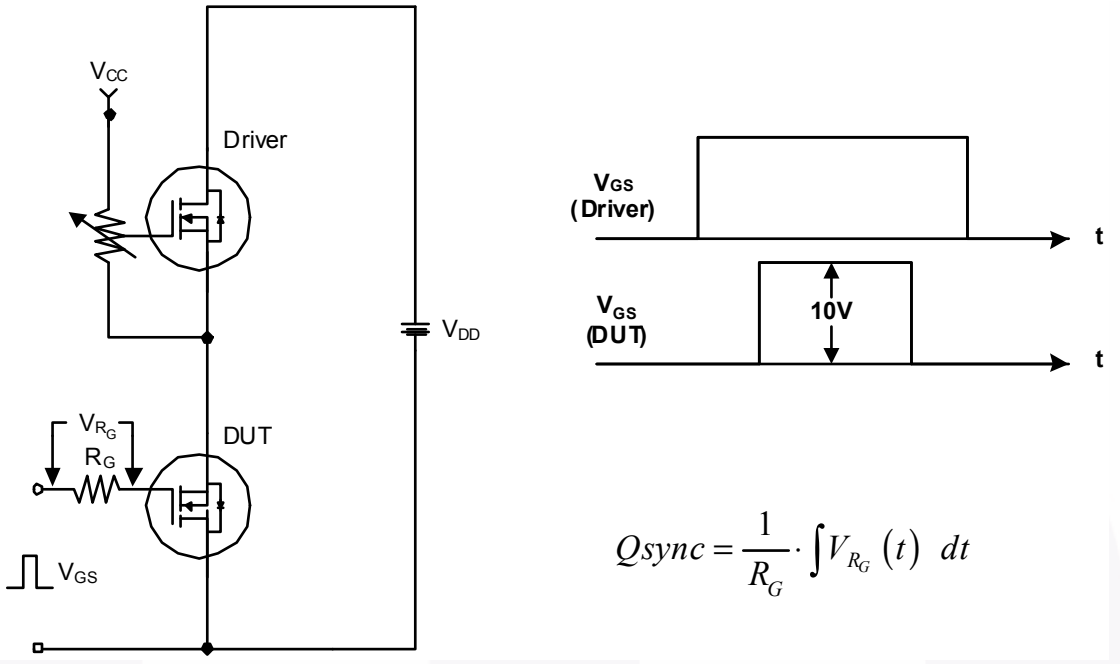



**Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms**




$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}(t)\ dt$$

**Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms**

## Mechanical Dimensions

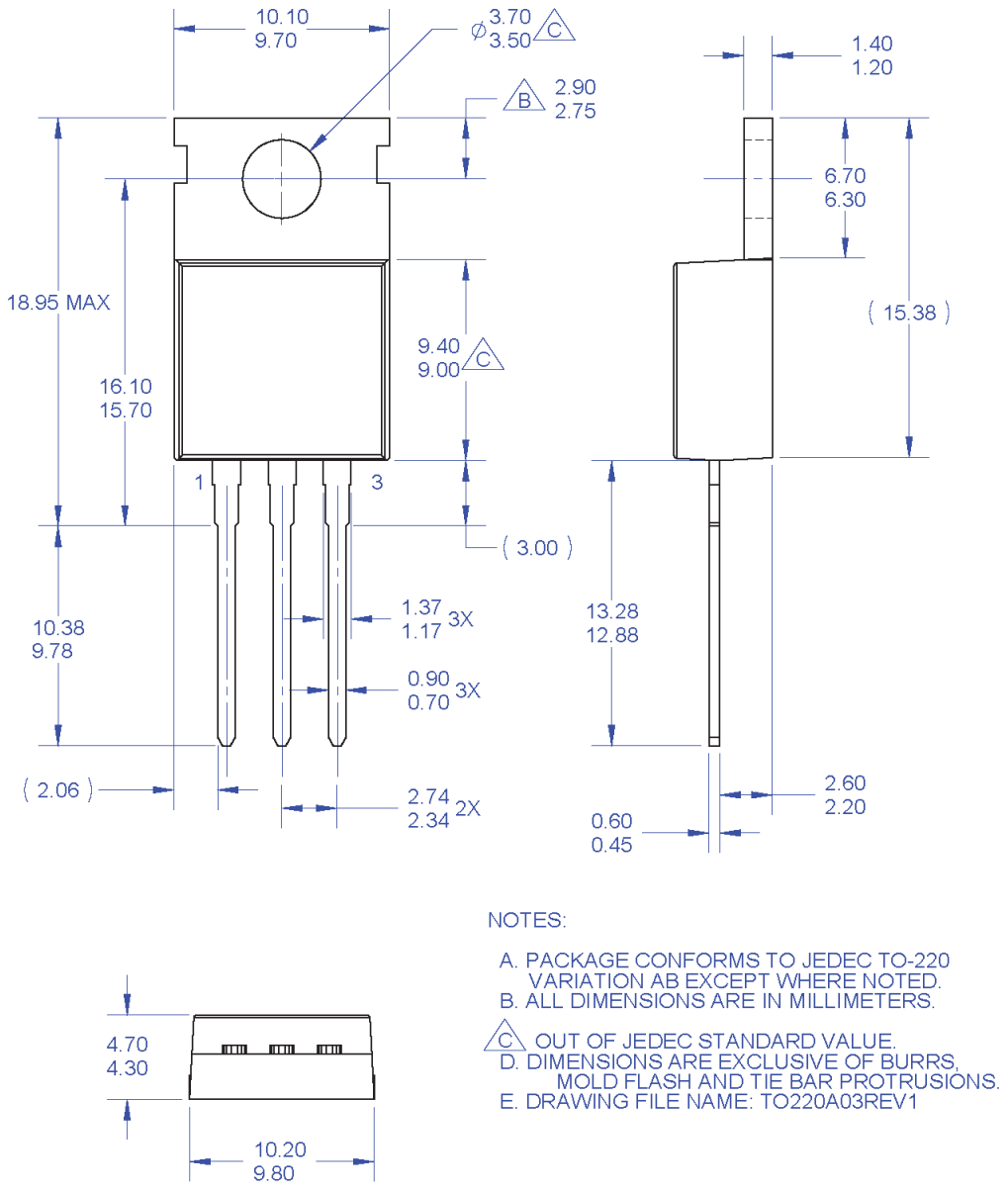



**Figure 19. TO220, Molded, 3-Lead, Jedec Variation AB, Non Jedec F102**

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