

# FDPF035N06B

## N-Channel PowerTrench® MOSFET

60 V, 88 A, 3.5 mΩ

### Features

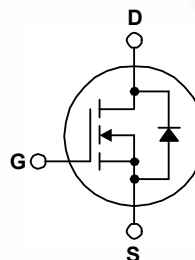
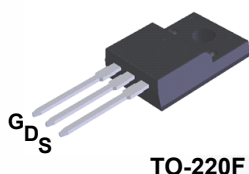
- $R_{DS(on)} = 2.91 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 88 \text{ A}$
- Low FOM  $R_{DS(on)} * Q_G$
- Low Reverse Recovery Charge,  $Q_{rr}$
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDPF035N06B_F152	Unit
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	88
		- Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	62
$I_{DM}$	Drain Current	- Pulsed (Note 1)	352
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	600
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	46.3
		- Derate Above $25^\circ\text{C}$	0.31
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDPF035N06B_F152	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF035N06B_F152	FDPF035N06B	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.03	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2	-	4	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 88 \text{ A}$	-	2.91	3.5	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 88 \text{ A}$	-	176	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	6035	8030	pF
$C_{oss}$	Output Capacitance		-	1685	2240	pF
$C_{rss}$	Reverse Transfer Capacitance		-	55	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	2619	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 30 \text{ V}, I_D = 100 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	76	99	nC
$Q_{gs}$	Gate to Source Gate Charge		-	29	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	12	-	nC
$V_{plateau}$	Gate Plateau Voltage		(Note 4)	-	5.2	-
$Q_{sync}$	Total Gate Charge Sync.	$V_{DS} = 0 \text{ V}, I_D = 50 \text{ A}$	-	67.3	-	nC
$Q_{oss}$	Output Charge	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	92.4	-	nC
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	2.0	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 100 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	32	74	ns
$t_r$	Turn-On Rise Time		-	33	76	ns
$t_{d(off)}$	Turn-Off Delay Time		-	56	122	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	23	56

### Drain-Source Diode Characteristics

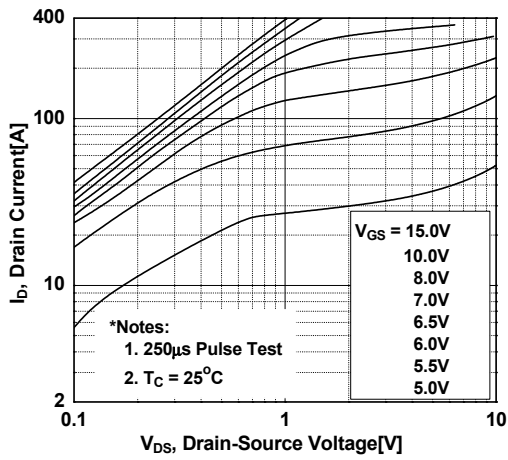
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	88	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	352	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 88 \text{ A}$	-	-	1.25	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 100 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	71	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	78	-	nC

#### Notes:

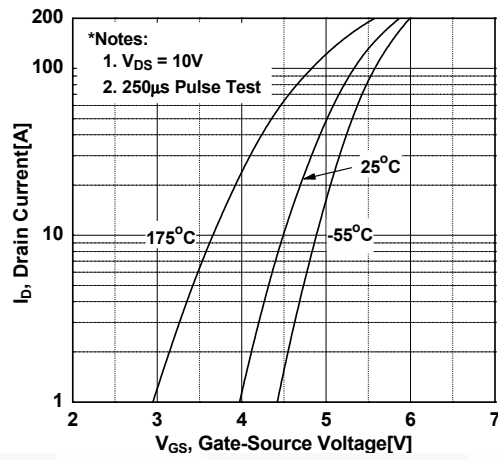
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 3 \text{ mH}, I_{AS} = 20 \text{ A}$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 100 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

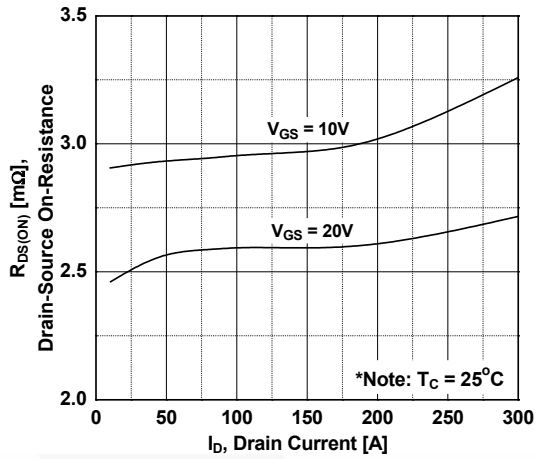
**Figure 1. On-Region Characteristics**



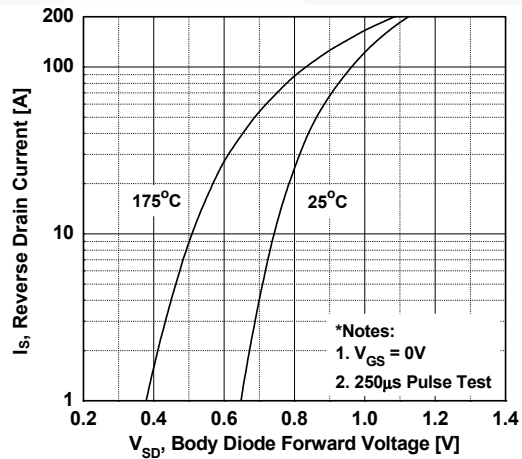
**Figure 2. Transfer Characteristics**



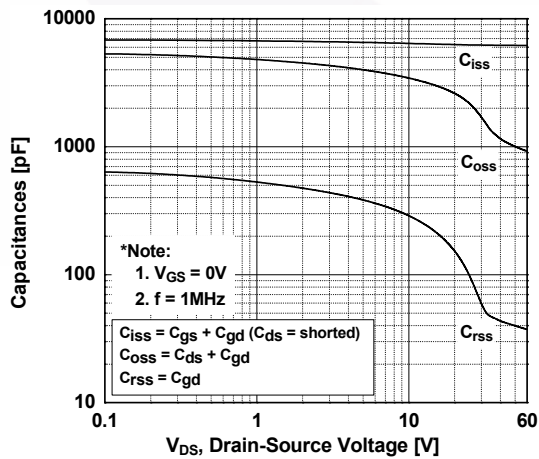
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



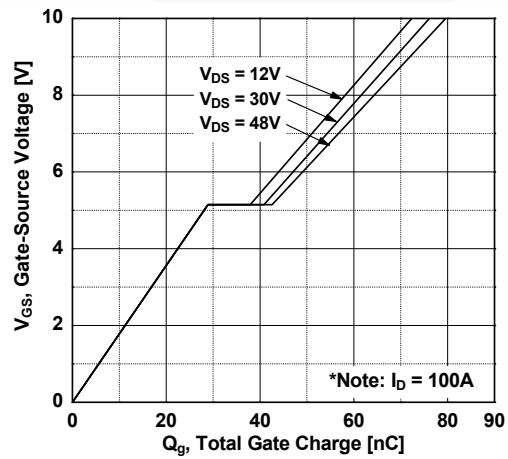
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

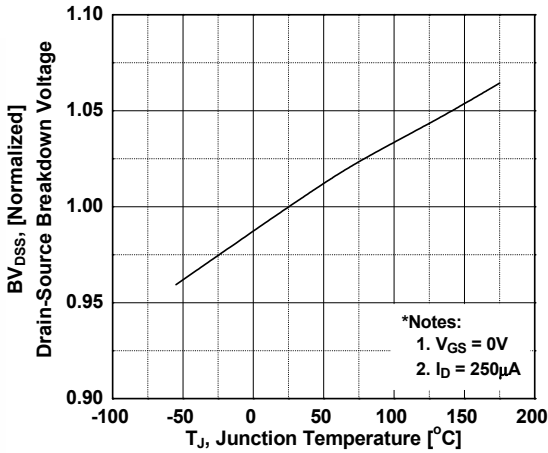


**Figure 6. Gate Charge Characteristics**

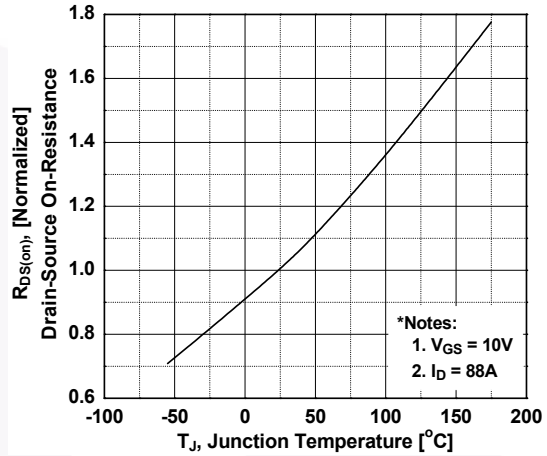


**Typical Performance Characteristics** (Continued)

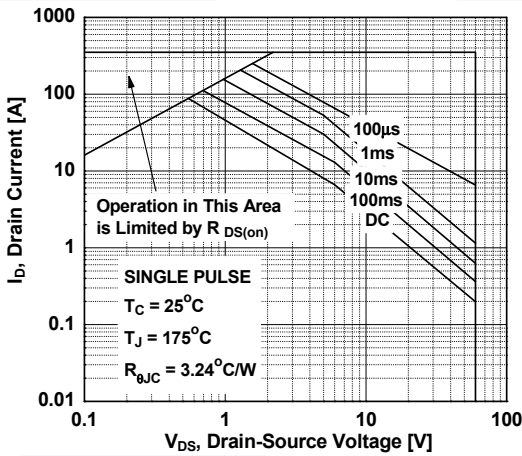
**Figure 7. Breakdown Voltage Variation vs. Temperature**



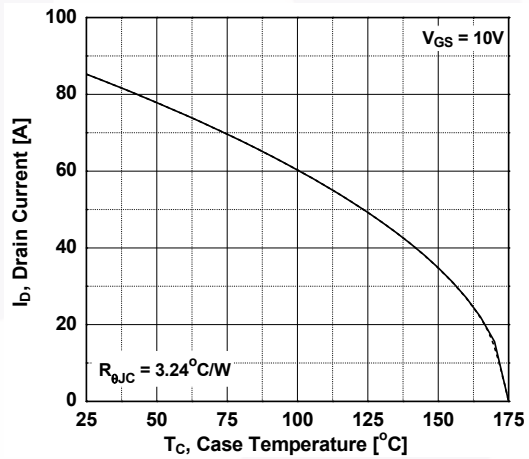
**Figure 8. On-Resistance Variation vs. Temperature**



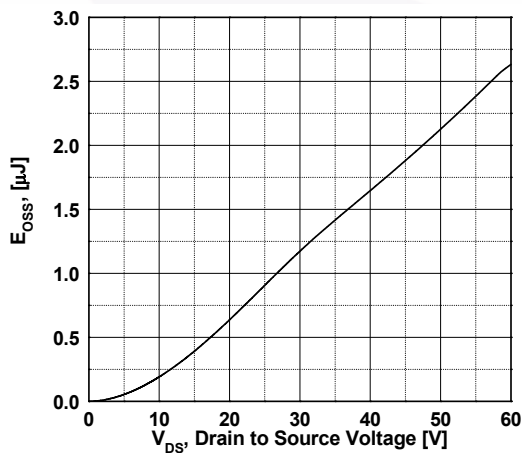
**Figure 9. Maximum Safe Operating Area**



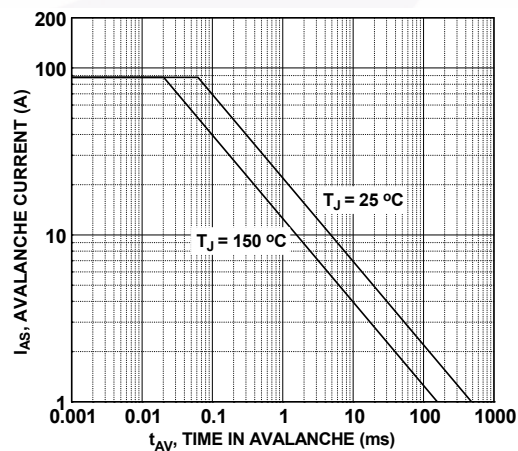
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E\_oss vs. Drain to Source Voltage**

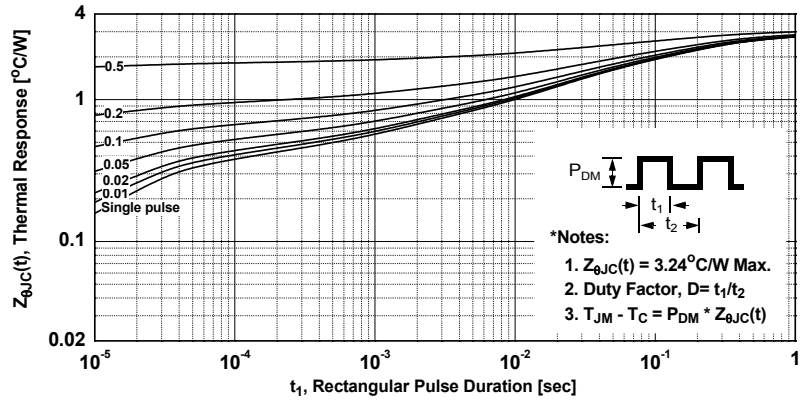


**Figure 12. Unclamped Inductive Switching Capability**



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve





**Figure 14. Gate Charge Test Circuit & Waveform**



**Figure 15. Resistive Switching Test Circuit & Waveforms**



**Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms**



Figure 17. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

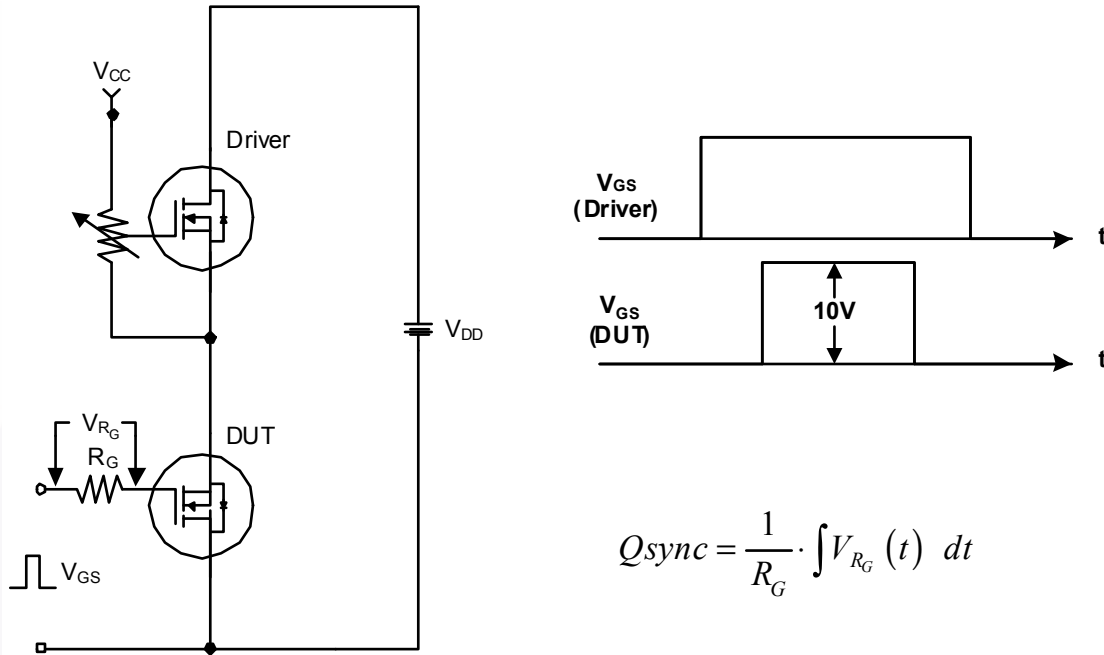
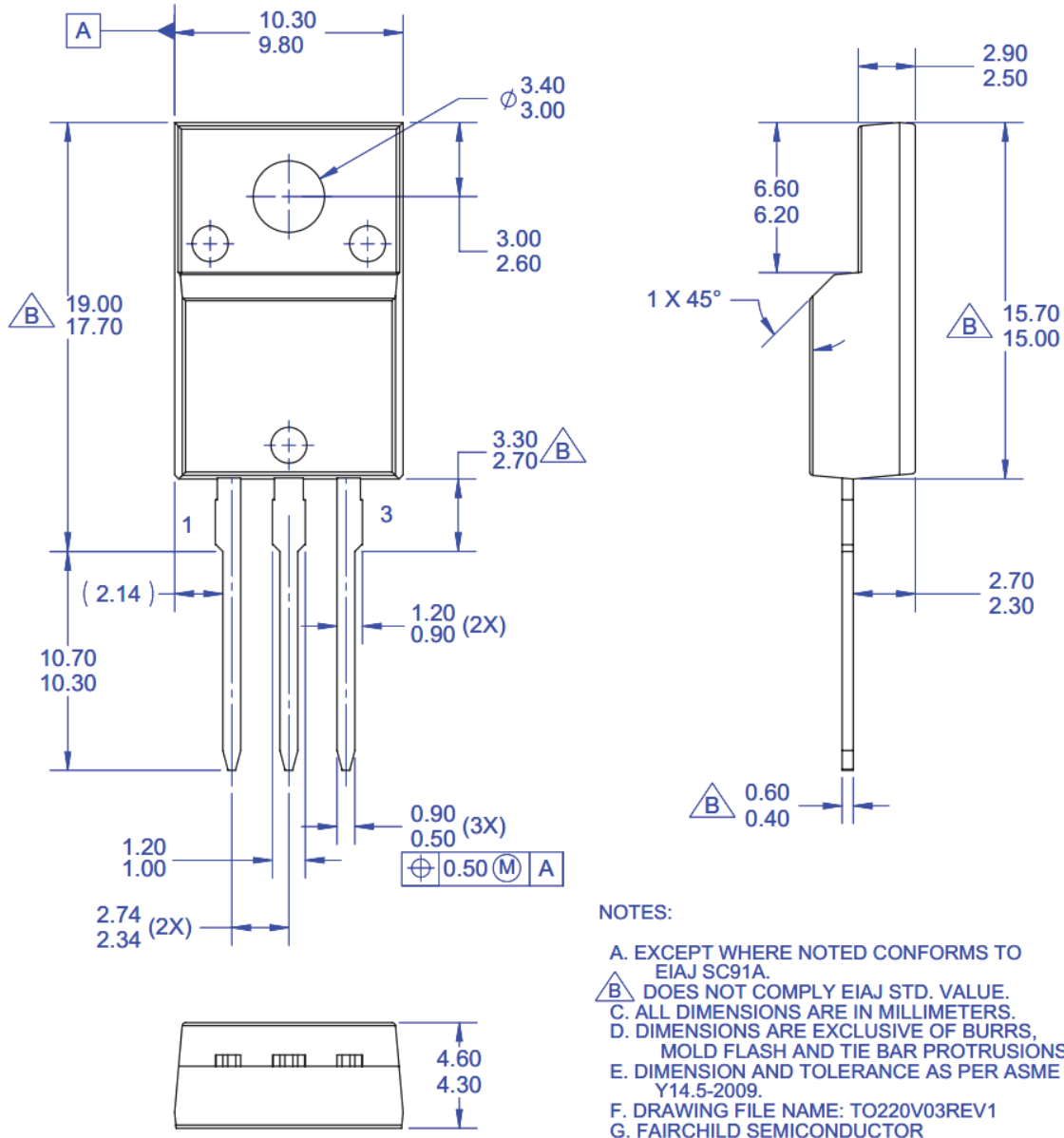


Figure 18. Total Gate Charge  $Q_{sync}$ . Test Circuit & Waveforms



### Mechanical Dimensions



**Figure 19. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Takcheong**

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