

December 2011

### FDZ661PZ

# P-Channel 1.5 V Specified PowerTrench<sup>®</sup> Thin WL-CSP MOSFET -20 V, -2.6 A, 140 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 140 m $\Omega$  at  $V_{GS}$  = -4.5 V,  $I_D$  = -2 A
- Max  $r_{DS(on)} = 182 \text{ m}\Omega$  at  $V_{GS} = -2.5 \text{ V}$ ,  $I_D = -1.5 \text{ A}$
- Max  $r_{DS(on)}$  = 231 m $\Omega$  at  $V_{GS}$  = -1.8 V,  $I_D$  = -1 A
- Max  $r_{DS(on)}$  = 315 m $\Omega$  at  $V_{GS}$  = -1.5 V,  $I_D$  = -1 A
- Occupies only 0.64 mm<sup>2</sup> of PCB area. Less than 16% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.4 mm height when mounted to PCB
- HBM ESD protection level > 2 kV (Note3)
- RoHS Compliant

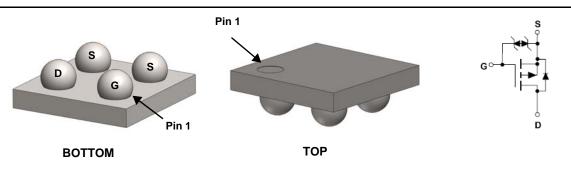


### **General Description**

Designed on Fairchild's advanced 1.5 V PowerTrench<sup>®</sup> process with state of the art "fine pitch" Thin WLCSP packaging process, the FDZ661PZ minimizes both PCB space and  $r_{DS(on)}.$  This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile (0.4 mm) and small (0.8x0.8 mm²) packaging, low gate charge, and low  $r_{DS(on)}.$ 

### **Applications**

- Battery management
- Load switch
- Battery protection



#### WL-CSP 0.8X0.8 Thin

#### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

| Symbol                            | Para                                  | meter                  |           | Ratings     | Units |
|-----------------------------------|---------------------------------------|------------------------|-----------|-------------|-------|
| V <sub>DS</sub>                   | Drain to Source Voltage               |                        |           | -20         | V     |
| V <sub>GS</sub>                   | Gate to Source Voltage                |                        |           | ±8          | V     |
| 1                                 | -Continuous                           | T <sub>A</sub> = 25 °C | (Note 1a) | -2.6        | ^     |
| ID                                | -Pulsed                               |                        |           | -10         | A     |
| D                                 | Power Dissipation                     | T <sub>A</sub> = 25 °C | (Note 1a) | 1.3         | 10/   |
| $P_{D}$                           | Power Dissipation                     | T <sub>A</sub> = 25 °C | (Note 1b) | 0.4         | W     |
| T <sub>J</sub> , T <sub>STG</sub> | Operating and Storage Junction Temper | erature Range          |           | -55 to +150 | °C    |

#### **Thermal Characteristics**

| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 93  | °C/W |
|-----------------|---|-----------|-----|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1b) | 311 | C/VV |

#### **Package Marking and Ordering Information**

| Device Marking | Device   | Package             | Reel Size | Tape Width | Quantity   |
|----------------|----------|---------------------|-----------|------------|------------|
| EH             | FDZ661PZ | WL-CSP 0.8X0.8 Thin | 7 "       | 8 mm       | 5000 units |

### **Electrical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted

| Symbol                                 | Parameter                                    | Test Conditions                                  | Min | Тур | Max | Units |
|--|--|--|-----|-----|-----|-------|
| Off Chara                              | cteristics                                   |  |     |     |     |       |
| BV <sub>DSS</sub>                      | Drain to Source Breakdown Voltage            | $I_D = -250 \mu A, V_{GS} = 0 V$                 | -20 |     |     | V     |
| $\frac{\Delta BV_{DSS}}{\Delta T_{J}}$ | Breakdown Voltage Temperature<br>Coefficient | $I_D$ = -250 μA, referenced to 25 °C             |     | -13 |     | mV/°C |
| I <sub>DSS</sub>                       | Zero Gate Voltage Drain Current              | V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V   |     |     | -1  | μΑ    |
| I <sub>GSS</sub>                       | Gate to Source Leakage Current               | $V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$ |     |     | ±6  | μΑ    |

#### **On Characteristics**

| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                            | $V_{GS} = V_{DS}, I_{D} = -250 \mu A$                                     | -0.3 | -0.7 | -1.2 | V     |
|--|---|---|------|------|------|-------|
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage<br>Temperature Coefficient | $I_D$ = -250 $\mu$ A, referenced to 25 °C                                 |      | 2.5  |      | mV/°C |
|  |   | $V_{GS} = -4.5 \text{ V}, I_D = -2 \text{ A}$                             |      | 108  | 140  |       |
|  |   | $V_{GS} = -2.5 \text{ V}, I_D = -1.5 \text{ A}$                           |      | 129  | 182  |       |
| r <sub>DS(on)</sub>                    | Static Drain to Source On Resistance                        | $V_{GS} = -1.8 \text{ V}, I_D = -1 \text{ A}$                             |      | 159  | 231  | mΩ    |
|  |   | $V_{GS} = -1.5 \text{ V}, I_D = -1 \text{ A}$                             |      | 201  | 315  |       |
|  |   | $V_{GS} = -4.5 \text{ V}, I_D = -2 \text{ A}, T_J = 125 ^{\circ}\text{C}$ |      | 143  | 204  |       |
| 9 <sub>FS</sub>                        | Forward Transconductance                                    | $V_{DD} = -5 \text{ V}, I_D = -2 \text{ A}$                               |      | 7.8  |      | S     |

#### **Dynamic Characteristics**

| C <sub>iss</sub> | Input Capacitance            | V 40 V V 0 V  | 416 | 555 | pF |
|------------------|------------------------------|---|-----|-----|----|
| C <sub>oss</sub> | Output Capacitance           | $V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$ | 61  | 80  | pF |
| C <sub>rss</sub> | Reverse Transfer Capacitance | 1 - 1 101112  | 53  | 70  | pF |

#### **Switching Characteristics**

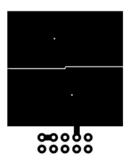
|                     | •                             |   |     |     |    |
|---------------------|-------------------------------|---|-----|-----|----|
| t <sub>d(on)</sub>  | Turn-On Delay Time            |   | 4.9 | 10  | ns |
| t <sub>r</sub>      | Rise Time                     | $V_{DD} = -10 \text{ V}, I_D = -2.5 \text{ A},$                             | 6.3 | 13  | ns |
| t <sub>d(off)</sub> | Turn-Off Delay Time           | $V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$                               | 68  | 108 | ns |
| t <sub>f</sub>      | Fall Time                     |   | 33  | 52  | ns |
| $Q_g$               | Total Gate Charge             | V 45VV 40V  | 6.3 | 8.8 | nC |
| $Q_{gs}$            | Gate to Source Charge         | $V_{GS} = -4.5 \text{ V}, V_{DD} = -10 \text{ V},$ $I_{D} = -2.5 \text{ A}$ | 0.6 |     | nC |
| Q <sub>ad</sub>     | Gate to Drain "Miller" Charge | ID = -2.5 A   | 1.7 |     | nC |

#### **Drain-Source Diode Characteristics**

| $V_{SD}$        | Source to Drain Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_S = -1.4 \text{ A}$ (Note 2) |  | -0.9 | -1.2 | V  |
|-----------------|---------------------------------------|---|--|------|------|----|
| t <sub>rr</sub> | Reverse Recovery Time                 | -I <sub>F</sub> = -2.5 A, di/dt = 100 A/μs            |  | 29   | 46   | ns |
| Q <sub>rr</sub> | Reverse Recovery Charge               | I <sub>F</sub> = -2.5 A, αl/αt = 100 A/μs             |  | 10   | 18   | nC |

#### Notes:

1. R<sub>0JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 93 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 311 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

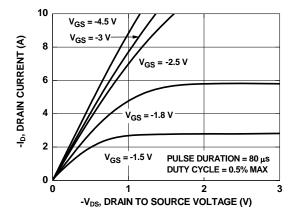


Figure 1. On-Region Characteristics

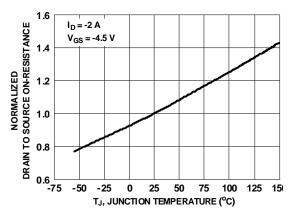


Figure 3. Normalized On-Resistance vs Junction Temperature

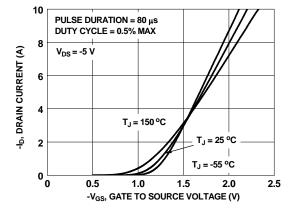


Figure 5. Transfer Characteristics

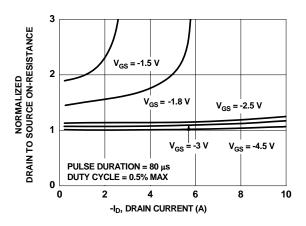


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

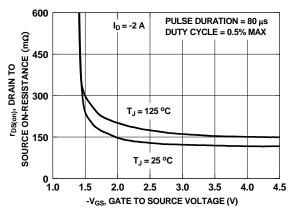


Figure 4. On-Resistance vs Gate to Source Voltage

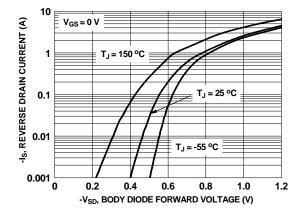


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

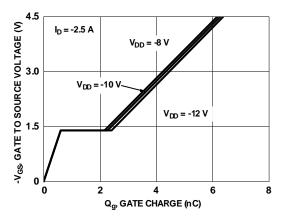


Figure 7. Gate Charge Characteristics

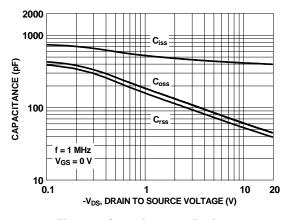


Figure 8. Capacitance vs Drain to Source Voltage

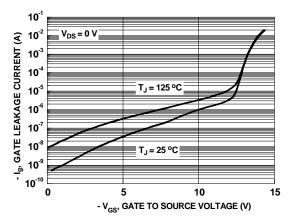


Figure 9. Gate Leakage Current vs Gate to Source Voltage

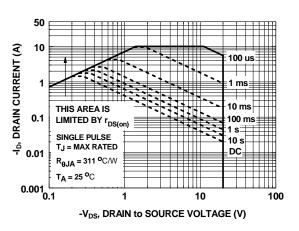


Figure 10. Forward Bias Safe Operating Area

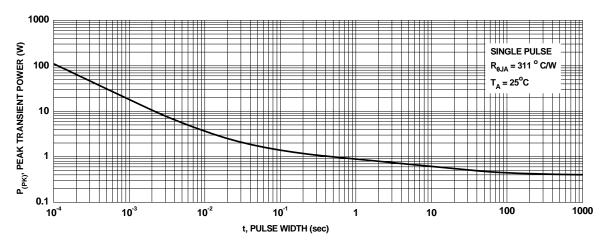


Figure 11. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

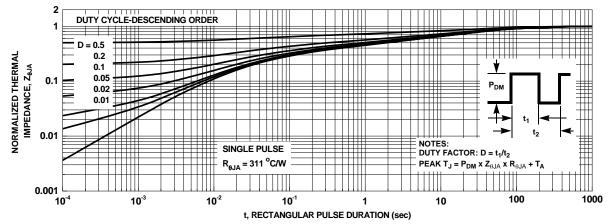
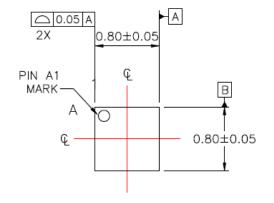
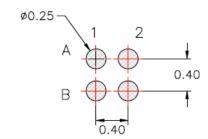


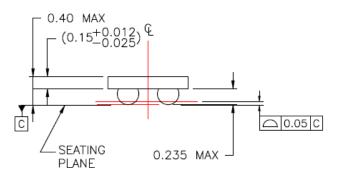
Figure 12. Junction-to-Ambient Transient Thermal Response Curve

### **Dimensional Outline and Pad Layout**

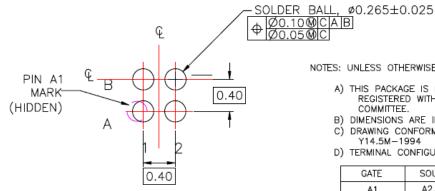




△ 0.05 B



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- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) TERMINAL CONFIGURATION TABLE:

| GATE | SOURCE | DRAIN |
|------|--------|-------|
| A1   | A2, B2 | B1    |





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