

December 2013

# FQP2N60C / FQPF2N60C

# N-Channel QFET® MOSFET

600 V, 2 A, 4.7 Ω

### Description

This N-Channel enhancement mode power MOSFET is • 2 A, 600 V,  $R_{DS(on)}$  = 4.7  $\Omega$  (Max.) @  $V_{GS}$  = 10 V, produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state • Low Gate Charge (Typ. 8.5 nC) resistance, and to provide superior switching performance

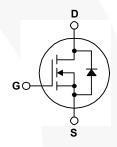
• Low Crss (Typ. 4.3 pF) and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power • 100% Avalanche Tested factor correction (PFC), and electronic lamp ballasts.

#### **Features**

- $I_D = 1 A$







### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP2N60C	FQPF2N60C	Unit
$V_{DSS}$	Drain-Source Voltage		600		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		2.0	2.0 *	Α
	- Continuous (T <sub>C</sub> = 100°C)		1.35	1.35 *	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	8	8 *	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	120		mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	2.0		Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	5.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3		4.5		V/ns
$P_{D}$	Power Dissipation (T <sub>C</sub> = 25°C)		54	23	W
	- Derate above 25°C		0.43	0.18	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		°C	

<sup>\*</sup> Drain current limited by maximum junction temperature.

### **Thermal Characteristics**

Symbol	Parameter	FQP2N60C	FQPF2N60C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.32	5.5	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ, Max.	0.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	°C/W

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP2N60C	FQP2N60C	TO-220	Tube	N/A	N/A	50 units
FQPF2N60C	FQPF2N60C	TO-220F	Tube	N/A	N/A	50 units

### **Flactrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	600			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.6		V/°C
I <sub>DSS</sub> Zer	Zero Onto Valle de Brain Ourrant	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V			1	μА
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C			10	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
r <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A		3.6	4.7	Ω
9 <sub>FS</sub>	Forward Transconductance	uctance $V_{DS} = 40 \text{ V}, I_D = 1 \text{ A}$		5.0		S
Dynam	ic Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		180	235	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		20	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			4.3	5.6	pF
Switch	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V = 200 V I = 2 A		9	28	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 300 \text{ V}, I_{D} = 2 \text{ A},$ $R_{G} = 25 \Omega$		25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	NG - 23 32		24	58	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		28	66	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 2 A,		8.5	12	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	/	1.3		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		4.1		nC
						/-
Drain-S	Source Diode Characteristics ar	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				8	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A		)	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A,		230	//	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		1.0		μС

- Notes: 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. L = 56 mH,  $I_{AS}$  = 2 A,  $V_{DD}$  = 50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C. 3.  $I_{SD}$   $\leq$  2 A, di/dt  $\leq$  200 A/ $\mu$ s,  $V_{DD}$   $\leq$  BV<sub>DSS</sub>, starting  $T_{J}$  = 25°C. 4. Essentially independent of operating temperature.

### **Typical Characteristics**

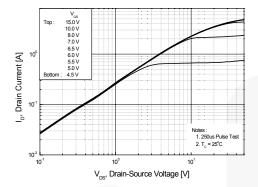
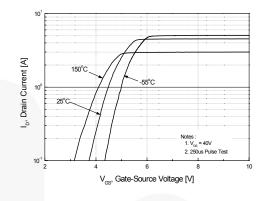


Figure 1. On-Region Characteristics



**Figure 2. Transfer Characteristics** 

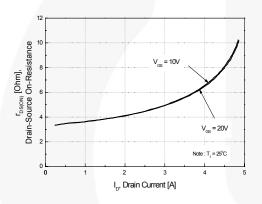


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

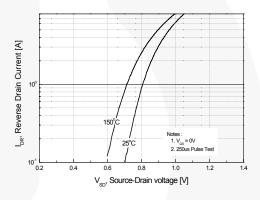


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

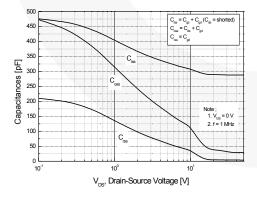


Figure 5. Capacitance Characteristics

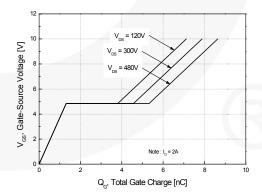


Figure 6. Gate Charge Characteristics

### Typical Characteristics (Continued)

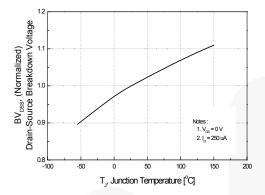


Figure 7. Breakdown Voltage Variation vs Temperature

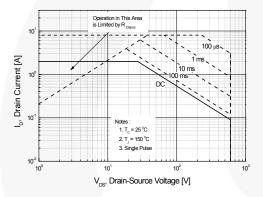


Figure 9-1. Maximum Safe Operating Area for FQP2N60C

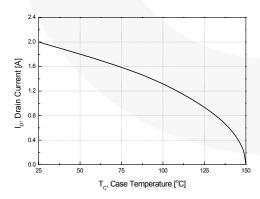


Figure 10. Maximum Drain Current vs Case Temperature

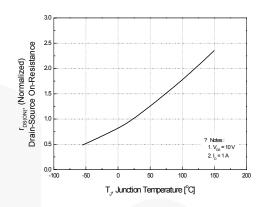


Figure 8. On-Resistance Variation vs Temperature

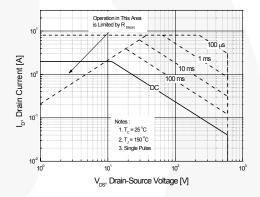


Figure 9-2. Maximum Safe Operating Area for FQPF2N60C

## Typical Characteristics (Continued)

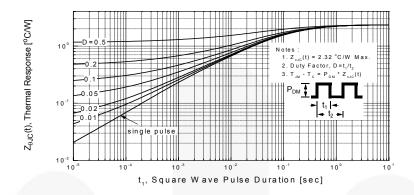


Figure 11-1. Transient Thermal Response Curve for FQP2N60C

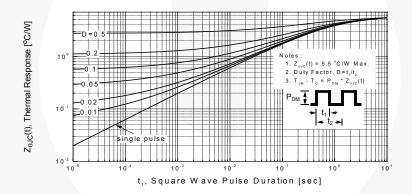


Figure 11-2. Transient Thermal Response Curve for FQPF2N60C

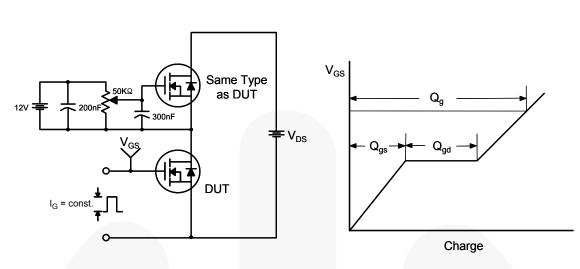


Figure 12. Gate Charge Test Circuit & Waveform

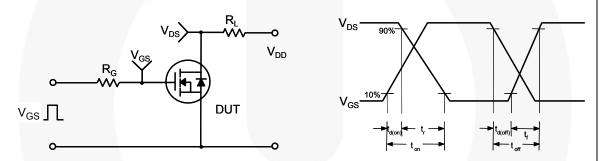


Figure 13. Resistive Switching Test Circuit & Waveforms

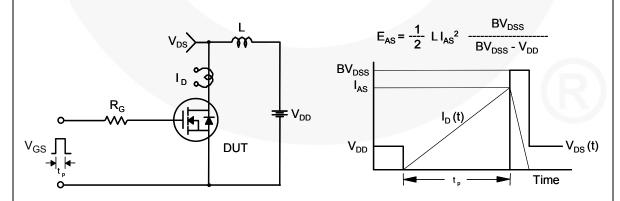
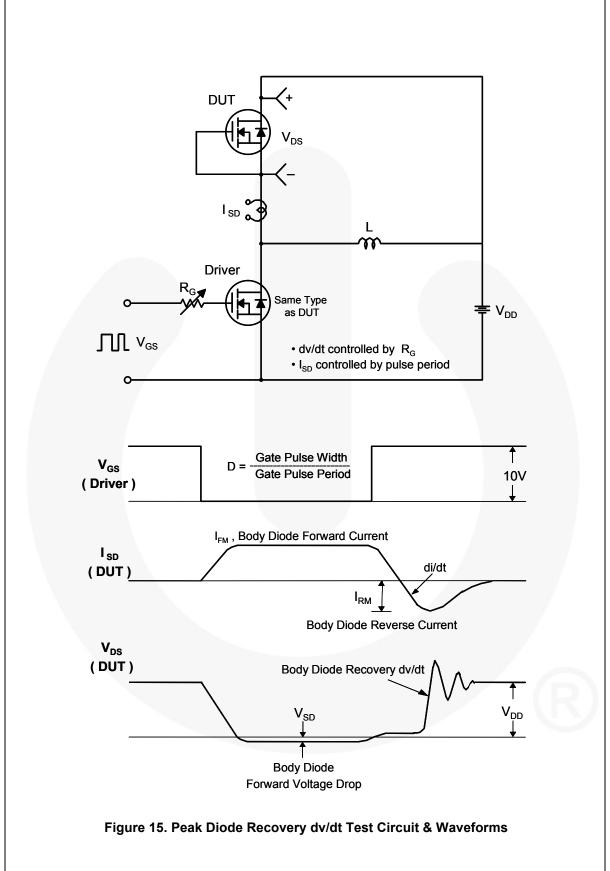


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



### **Mechanical Dimensions**

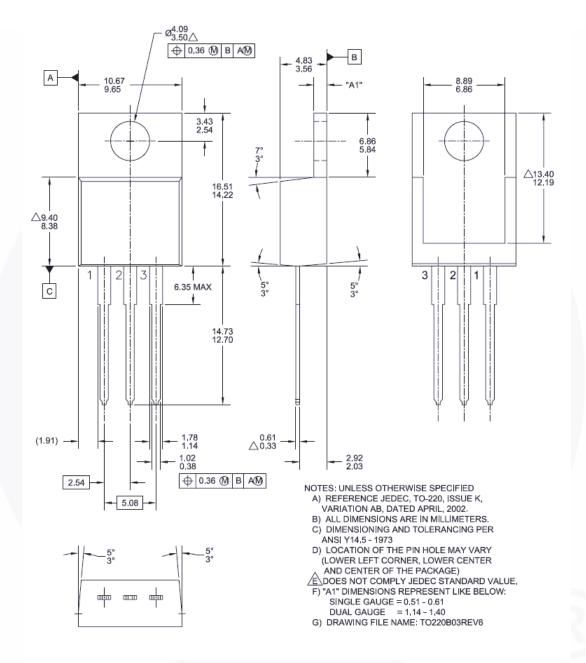


Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB

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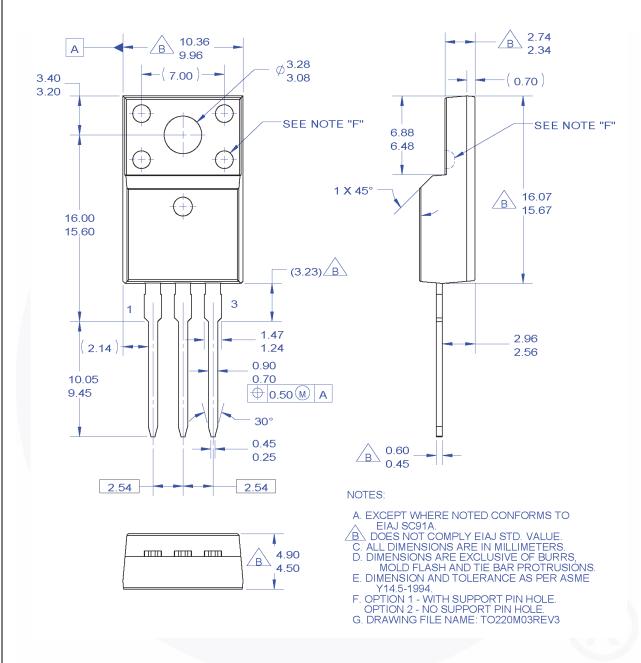


Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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