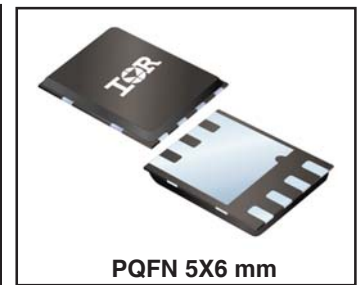
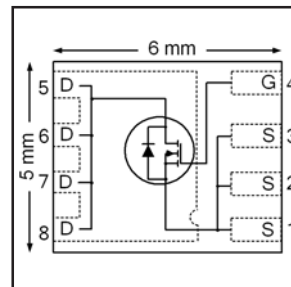


<b>V<sub>DS</sub></b>	<b>30</b>	<b>V</b>
<b>R<sub>DS(on)</sub> max</b> (@ V <sub>GS</sub> = 10V)	<b>8.1</b>	<b>mΩ</b>
<b>Q<sub>g</sub> (typical)</b>	<b>7.8</b>	<b>nC</b>
<b>R<sub>G</sub> (typical)</b>	<b>1.4</b>	<b>Ω</b>
<b>I<sub>D</sub></b> (@ T <sub>C(Bottom)</sub> = 25°C)	<b>44</b>	<b>A</b>



### Applications

- Control MOSFET for buck converters

### Features and Benefits

#### Features

Low charge (typical 7.8nC)
Low thermal resistance to PCB (< 4.9°C/W)
100% R <sub>g</sub> tested
Low profile (< 0.9 mm)
Industry-standard pinout
Compatible with existing Surface Mount Techniques
RoHS compliant containing no lead, no bromide and no halogen
MSL1, Industrial qualification

results in

⇒

#### Benefits

Lower switching losses
Increased power density
Increased reliability
Increased power density
Multi-vendor compatibility
Easier manufacturing
Environmentally friendly
Increased reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH5306TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRFH5306TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	EOL notice #259

### Absolute Maximum Ratings

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	±20	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	15	A
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	13	
I <sub>D</sub> @ T <sub>C(Bottom)</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	44	
I <sub>D</sub> @ T <sub>C(Bottom)</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	28	
I <sub>DM</sub>	Pulsed Drain Current ①	60	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Power Dissipation ②	3.6	W
P <sub>D</sub> @ T <sub>C(Bottom)</sub> = 25°C	Power Dissipation ②	26	
	Linear Derating Factor ③	0.029	W/°C
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		

Notes ① through ⑤ are on page 9

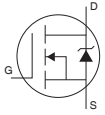
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	6.9	8.1	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 15A ③
		—	11	13.3		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.8	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-6.4	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	5.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	35	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 15A
Q <sub>g</sub>	Total Gate Charge	—	7.8	12	nC	V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 15A See Fig.17 & 18
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	1.8	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	1.1	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	3.0	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	1.9	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	4.1	—		
Q <sub>oss</sub>	Output Charge	—	4.9	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	1.4	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.0	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 15A R <sub>G</sub> = 1.8Ω See Fig.15
t <sub>r</sub>	Rise Time	—	26	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	9.1	—		
t <sub>f</sub>	Fall Time	—	6.1	—		
C <sub>iss</sub>	Input Capacitance	—	1125	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	230	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	102	—		

**Avalanche Characteristics**

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	46	mJ
I <sub>AR</sub>	Avalanche Current ①	—	15	A

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	44	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	60		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 15A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	17	26	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 15A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	18	27	nC	di/dt = 200A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic Inductance				

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	4.9	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	24	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	35	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	22	

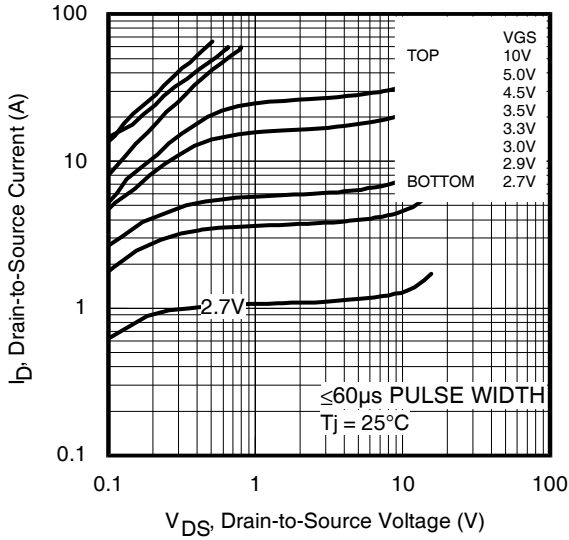


Fig 1. Typical Output Characteristics

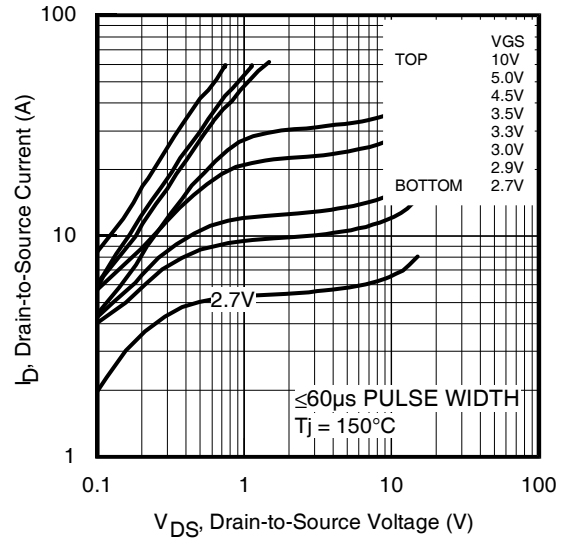


Fig 2. Typical Output Characteristics

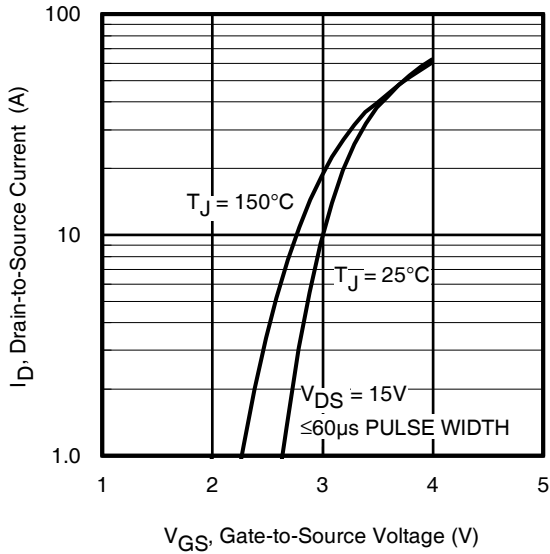


Fig 3. Typical Transfer Characteristics

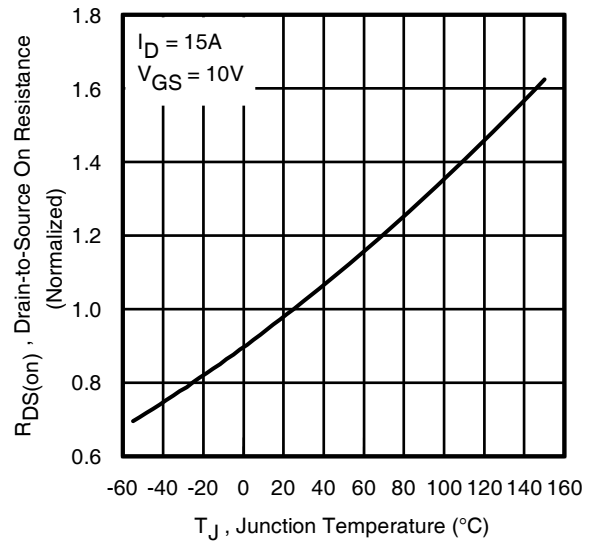


Fig 4. Normalized On-Resistance vs. Temperature

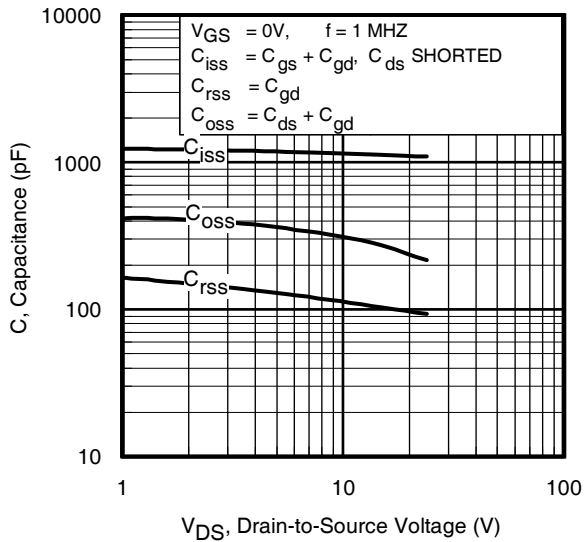


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

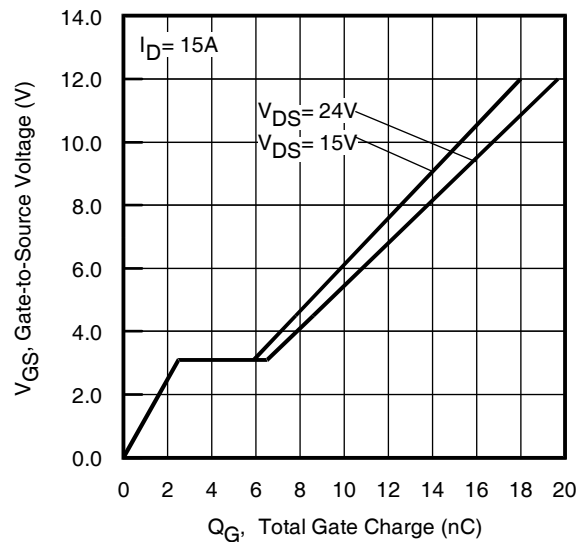
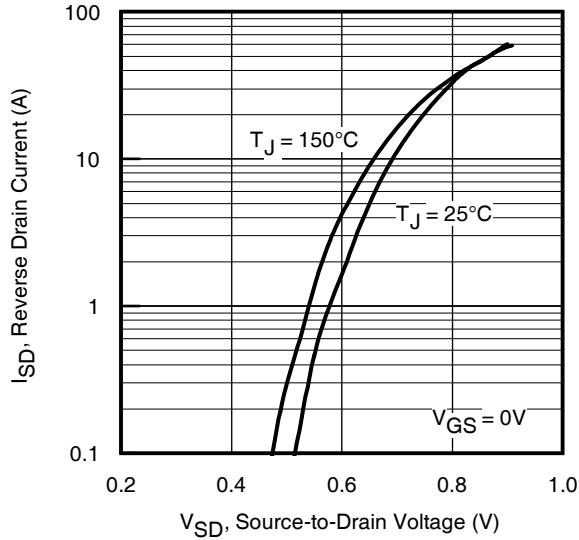
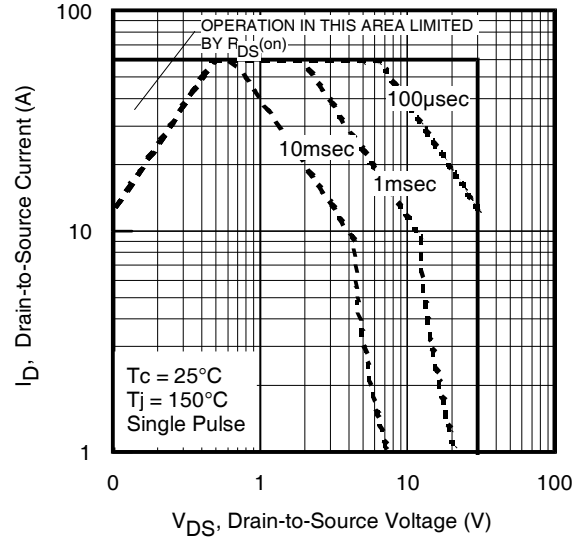
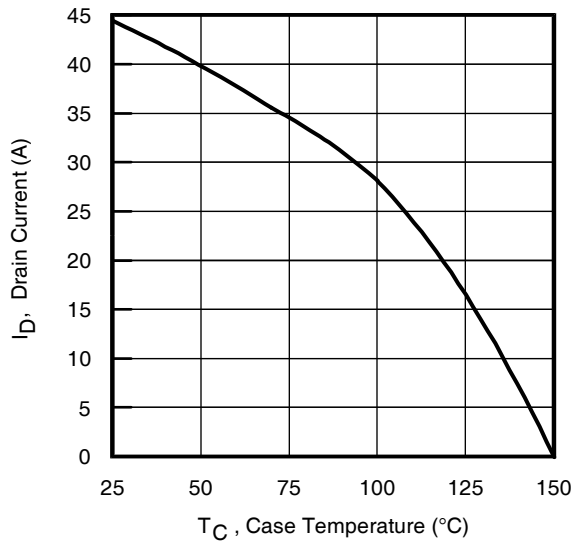
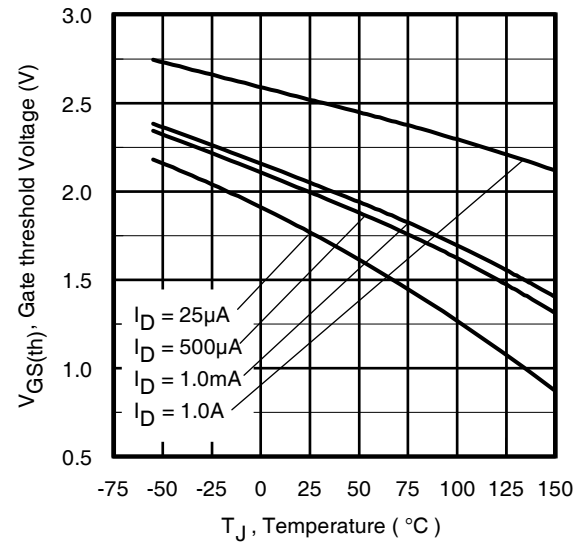
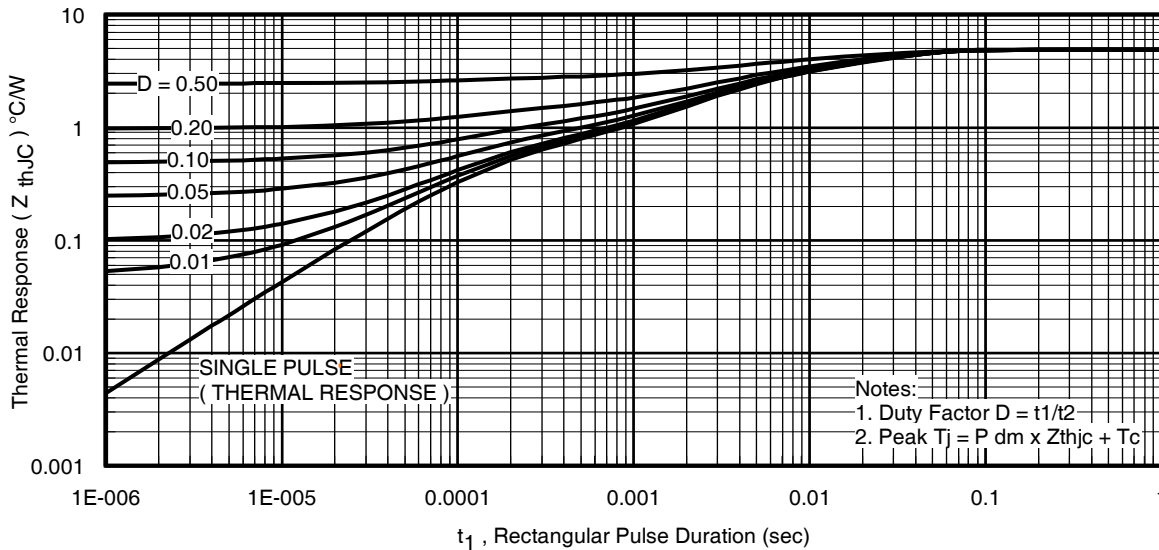
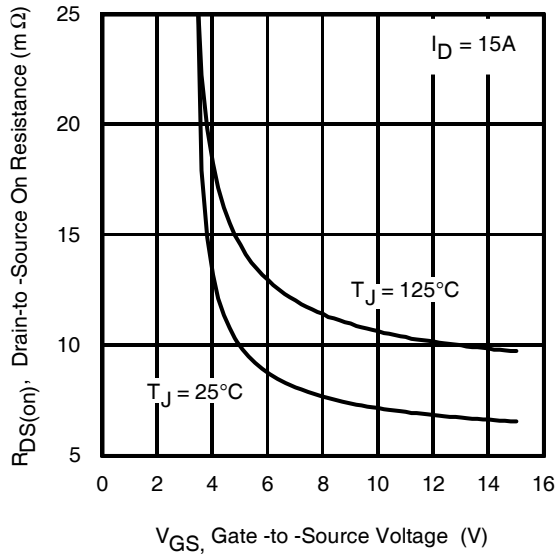
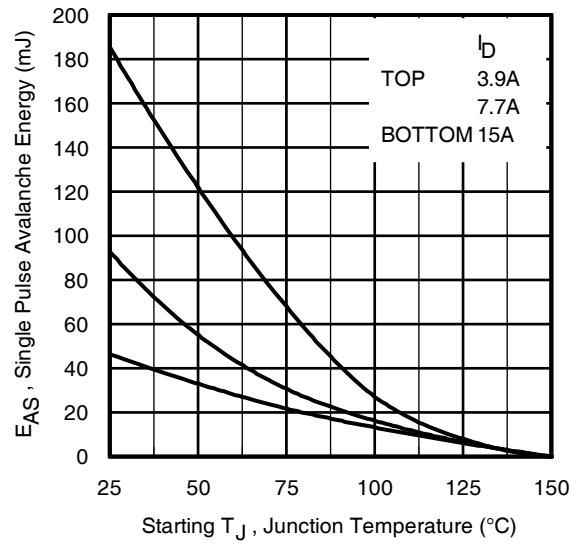


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case (Bottom) Temperature

**Fig 10.** Threshold Voltage vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)



**Fig 12.** On-Resistance vs. Gate Voltage



**Fig 13.** Maximum Avalanche Energy vs. Drain Current



**Fig 14a.** Unclamped Inductive Test Circuit



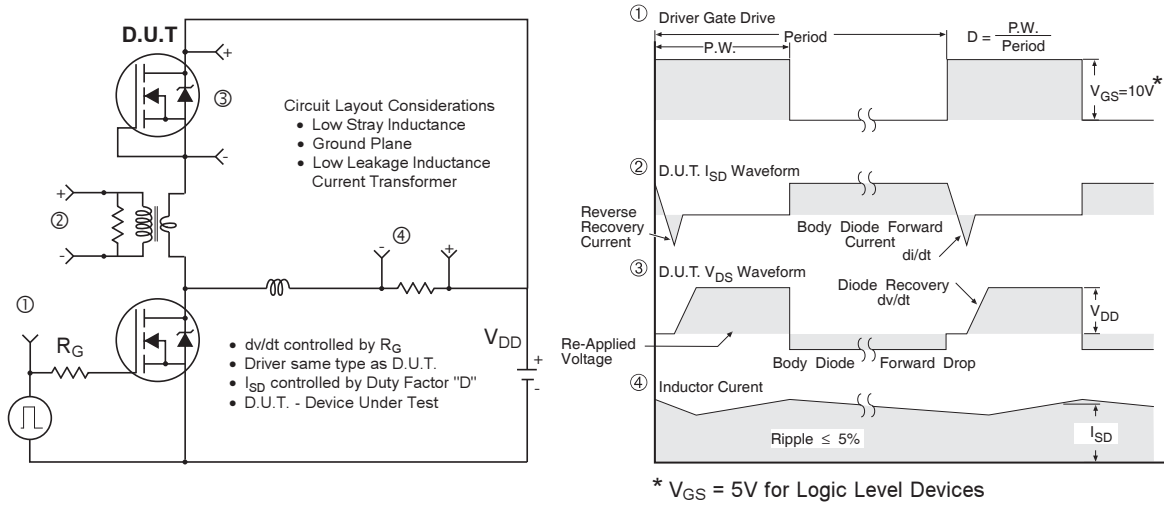
**Fig 14b.** Unclamped Inductive Waveforms



**Fig 15a.** Switching Time Test Circuit



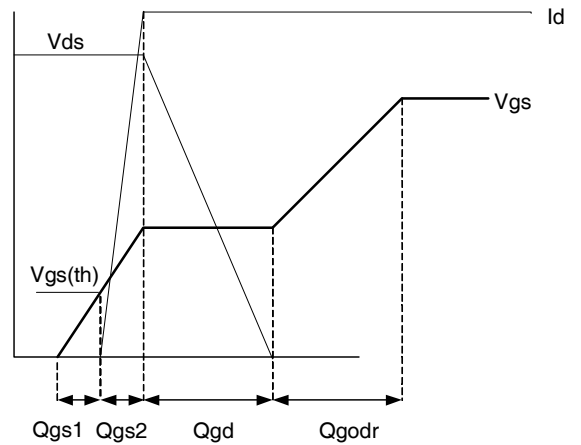
**Fig 15b.** Switching Time Waveforms



**Fig 16. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**

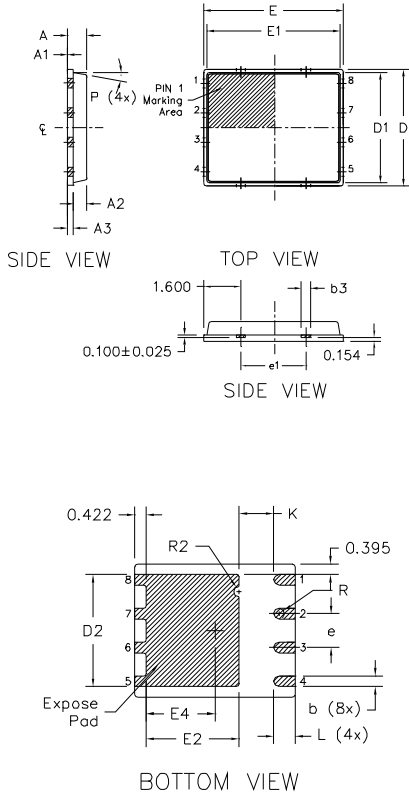


**Fig 17. Gate Charge Test Circuit**



**Fig 18. Gate Charge Waveform**

# PQFN 5x6 Outline "B" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

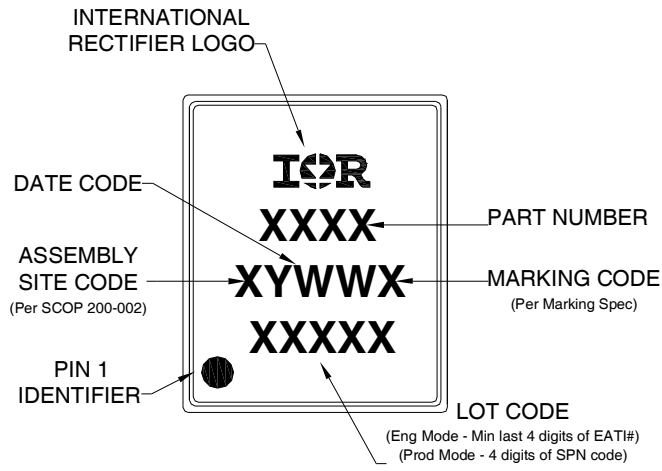
**Note:**

- Dimensions and tolerancing confirm to ASME Y14.5M-1994
- Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
- Caplanarity applies to the expose Heat Slug as well as the terminal
- Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

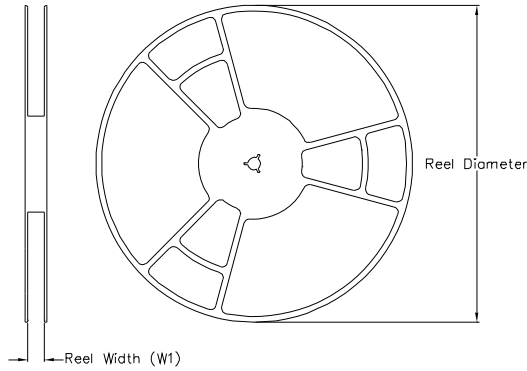
# PQFN 5x6 Outline "B" Part Marking



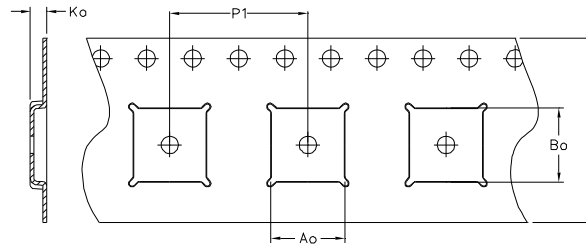
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

# PQFN 5x6 Outline "B" Tape and Reel

## REEL DIMENSIONS

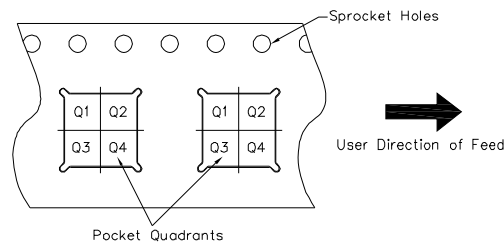


## TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component length
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**Qualification information<sup>†</sup>**

Qualification level	Industri <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.41\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 15\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.

**Revision History**

Date	Comment
1/20/2014	<ul style="list-style-type: none"> <li>• Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259).</li> <li>• Updated data sheet with the new IR corporate template.</li> </ul>
3/17/2015	<ul style="list-style-type: none"> <li>• Updated package outline and tape and reel on pages 7 and 8.</li> </ul>

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