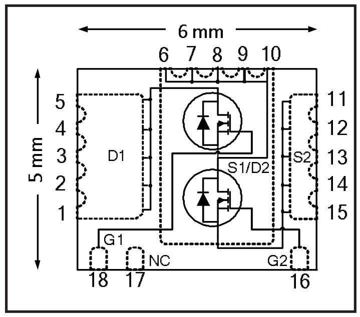
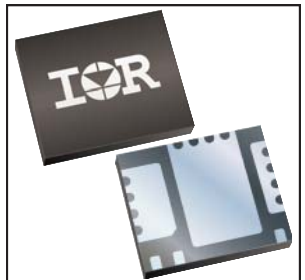
HEXFET® Power MOSFET

	Q1	Q2	
V_{DS}	30	30	V
$R_{DS(on)\ max}$ ($@V_{GS} = 10V$)	8.6	3.0	mΩ
$Q_{g\ (typical)}$	8.3	34	nC
I_D ($@T_A = 25°C$)	13	28	A




Dual PQFN 5X6 mm

Applications

- Control and synchronous MOSFET for buck converters

Features and Benefits

Features		Benefits
Control and synchronous FET in one package		Increased power density (50% vs two PQFN 5x6)
Low charge control MOSFET (8.3 nC typical)		Lower switching losses
Low R_{DSon} synchronous MOSFET (< 3.0 mΩ)	results in ⇒	Lower conduction losses
100% Rg tested		Increased reliability
Low Profile (≤ 0.9 mm)		Increased power density
Compatible with Existing Surface Mount Techniques		Easier manufacturing
RoHS Compliant Containing no Lead, no Bromide and no Halogen		Environmentally Friendlier
MSL2, Consumer Qualification		Increased reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH7911TRPbF	PQFN 5mm x 6mm	Tape and Reel	4000	
~~IRFH7911TR2PbF~~	~~PQFN 5mm x 6mm~~	~~Tape and Reel~~	~~400~~	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{DS}	Drain-to-Source Voltage	30		V
V_{GS}	Gate-to-Source Voltage	± 20		
I_D @ $T_A = 25°C$	Continuous Drain Current, V_{GS} @ 10V	13	28	A
I_D @ $T_A = 70°C$	Continuous Drain Current, V_{GS} @ 10V	10	23	
I_{DM}	Pulsed Drain Current ①	100	230	
P_D @$T_A = 25°C$	Power Dissipation	2.4	3.4	W
P_D @$T_A = 70°C$	Power Dissipation	1.5	2.2	
	Linear Derating Factor ⑤	0.019	0.027	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	7.7	2.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	53	37	

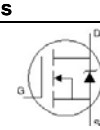
Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	Q1&Q2	30	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Q1	—	0.021	—	V/°C	Reference to 25°C, I_D = 1mA
		Q2	—	0.022	—		
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	Q1	—	7.2	8.6	mΩ	V_{GS} = 10V, I_D = 12A ③
			—	11.1	14.5		V_{GS} = 4.5V, I_D = 10A ③
		Q2	—	2.4	3.0		V_{GS} = 10V, I_D = 26A ③
			—	3.4	4.0		V_{GS} = 4.5V, I_D = 21A ③
$V_{GS(th)}$	Gate Threshold Voltage	Q1&Q2	1.35	—	2.35	V	Q1: V_{DS} = V_{GS}, I_D = 25μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	Q1	—	-6.8	—	mV/°C	Q2: V_{DS} = V_{GS}, I_D = 100μA
		Q2	—	-6.4	—		
I_{DSS}	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V_{DS} = 24V, V_{GS} = 0V
		Q1&Q2	—	—	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	Q1	17	—	—	S	V_{DS} = 15V, I_D = 10A
		Q2	106	—	—		V_{DS} = 15V, I_D = 21A
Q_g	Total Gate Charge	Q1	—	8.3	12	nC	
		Q2	—	34	51		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	Q1	—	2.0	—		Q1
		Q2	—	7.9	—		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	Q1	—	1.0	—		V_{GS} = 4.5V, I_D = 10A
		Q2	—	3.6	—		
Q_{gd}	Gate-to-Drain Charge	Q1	—	3.2	—		Q2
		Q2	—	11	—		V_{DS} = 15V
Q_{godr}	Gate Charge Overdrive	Q1	—	2.1	—		V_{GS} = 4.5V, I_D = 21A
		Q2	—	12	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	Q1	—	4.2	—		
		Q2	—	15	—		
Q_{oss}	Output Charge	Q1	—	5.0	—	nC	V_{DS} = 16V, V_{GS} = 0V
		Q2	—	19	—		
R_G	Gate Resistance	Q1	—	1.8	—	Ω	
		Q2	—	0.7	—		
$t_{d(on)}$	Turn-On Delay Time	Q1	—	12	—	ns	Q1
		Q2	—	22	—		V_{DD} = 15V, V_{GS} = 4.5V
t_r	Rise Time	Q1	—	15	—		I_D = 10A
		Q2	—	35	—		R_G=1.8Ω
$t_{d(off)}$	Turn-Off Delay Time	Q1	—	12	—		Q2
		Q2	—	28	—		V_{DD} = 15V, V_{GS} = 4.5V
t_f	Fall Time	Q1	—	5.9	—		I_D = 21A
		Q2	—	14	—		R_G=1.8Ω
C_{iss}	Input Capacitance	Q1	—	1060	—	pF	
		Q2	—	4450	—		V_{GS} = 0V
C_{oss}	Output Capacitance	Q1	—	230	—		V_{DS} = 15V
		Q2	—	850	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	Q1	—	110	—		
		Q2	—	440	—		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	12	32	mJ
I_{AR}	Avalanche Current ①	—	10	21	A

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	Q1	—	—	3.0	A	MOSFET symbol
	(Body Diode)	Q2	—	—	3.0		showing the
I_{SM}	Pulsed Source Current	Q1	—	—	100	A	integral reverse
	(Body Diode) ①	Q2	—	—	230		p-n junction diode. 
V_{SD}	Diode Forward Voltage	Q1	—	—	1.0	V	T_J = 25°C, I_S = 10A, V_{GS} = 0V ③
		Q2	—	—	1.0		T_J = 25°C, I_S = 21A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	Q1	—	13	20	ns	Q1 T_J = 25°C, I_F = 10A,
		Q2	—	20	29		V_{DD} = 15V, di/dt = 300A/μs ③
Q_{rr}	Reverse Recovery Charge	Q1	—	13	20	nC	Q2 T_J = 25°C, I_F = 21A,
		Q2	—	24	36		V_{DD} = 15V, di/dt = 280A/μs ③

Typical Characteristics

Q1 - Control FET

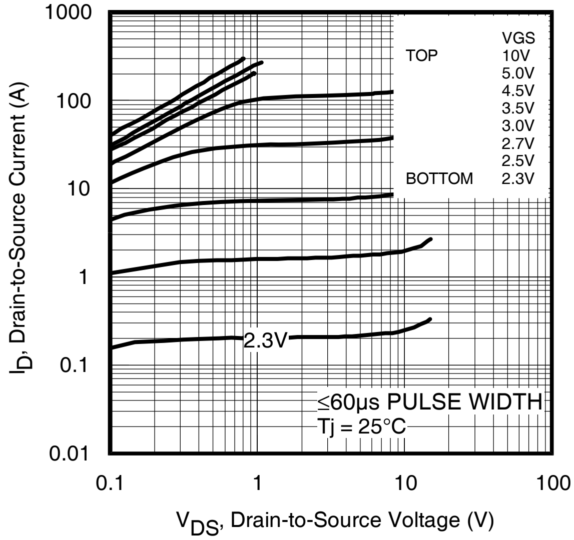


Fig 1. Typical Output Characteristics

Q2 - Synchronous FET

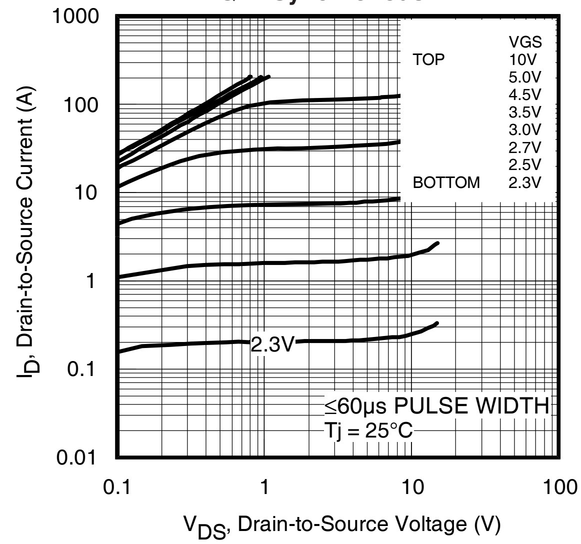


Fig 2. Typical Output Characteristics

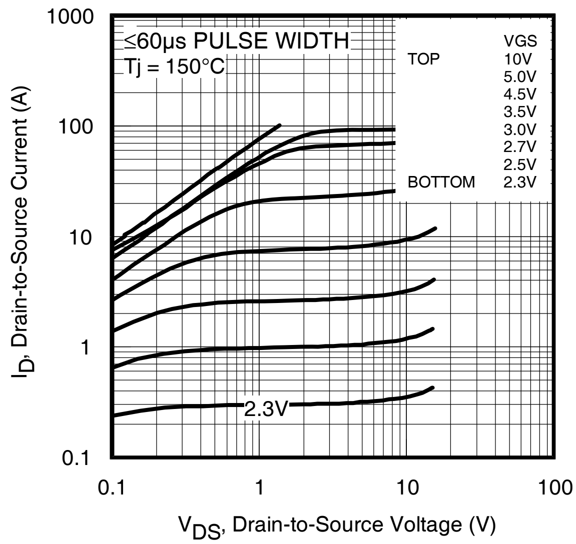


Fig 3. Typical Output Characteristics

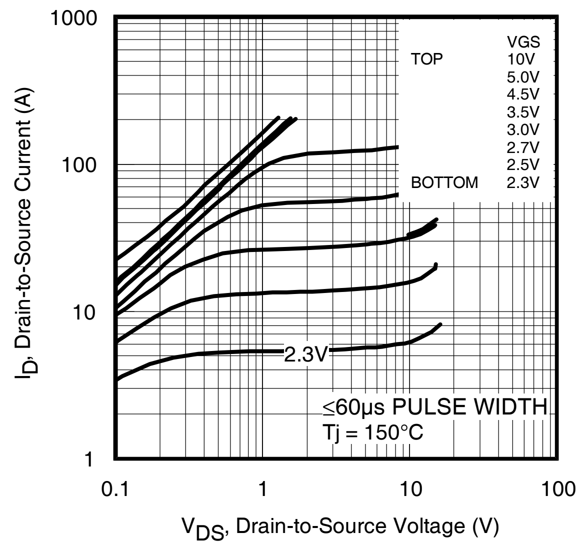


Fig 4. Typical Output Characteristics

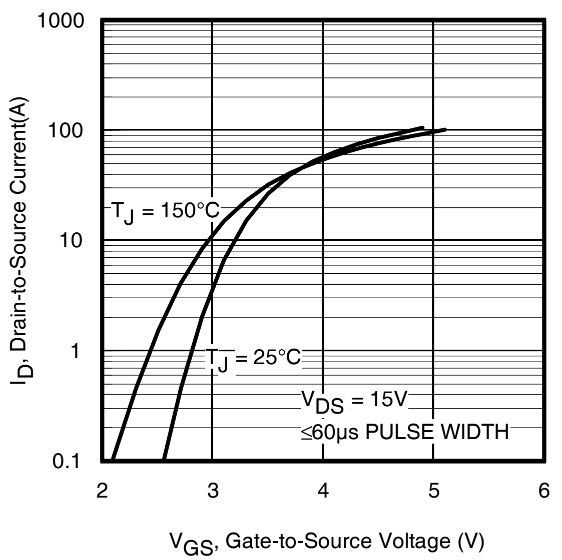


Fig 5. Typical Transfer Characteristics

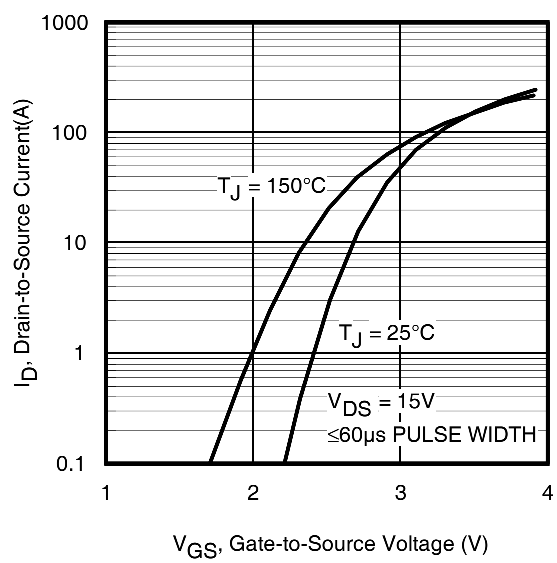


Fig 6. Typical Transfer Characteristics

Typical Characteristics

Q1 - Control FET

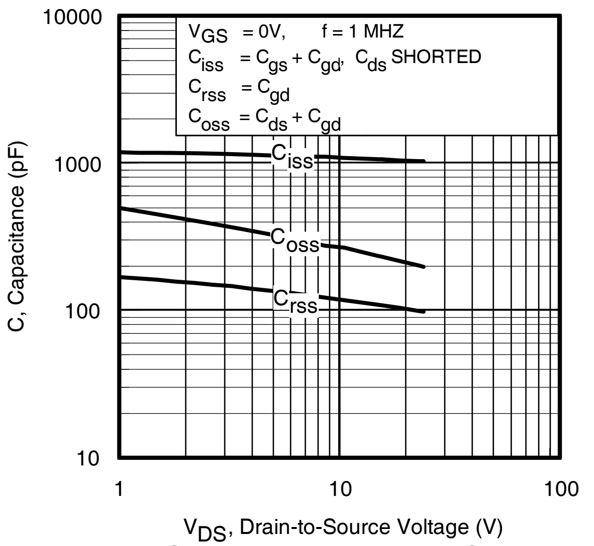


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Q2 - Synchronous FET

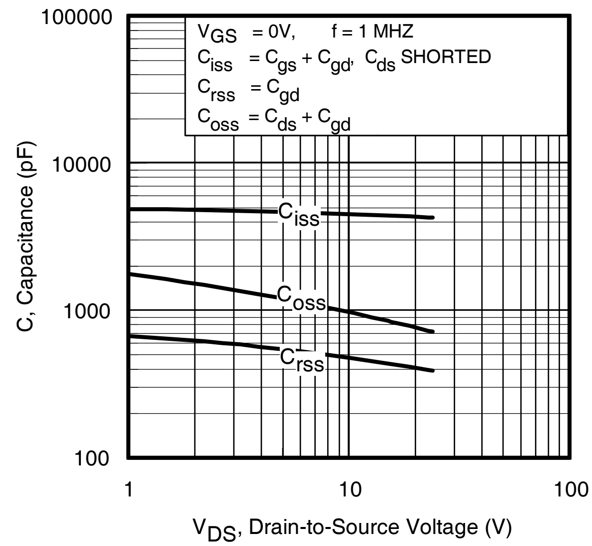


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

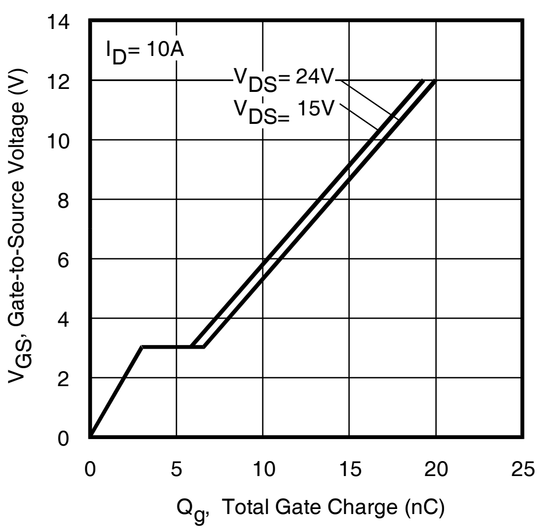


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

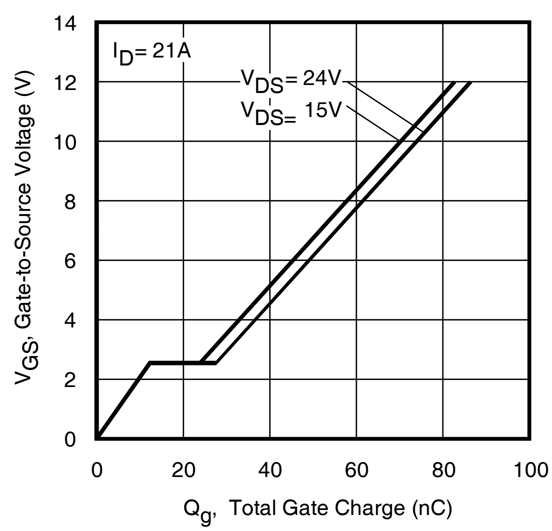


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

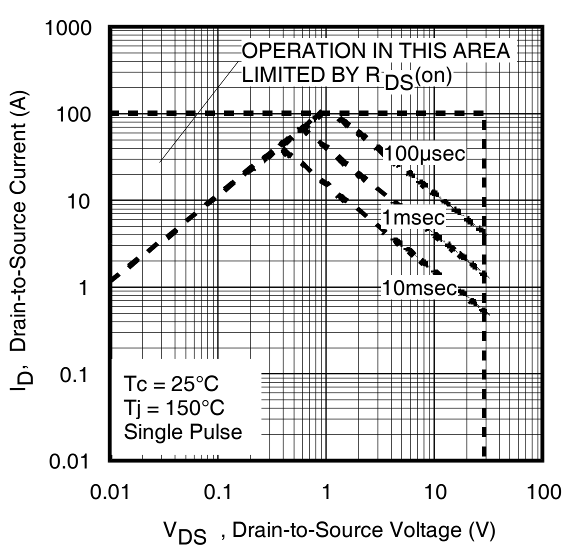


Fig 11. Maximum Safe Operating Area

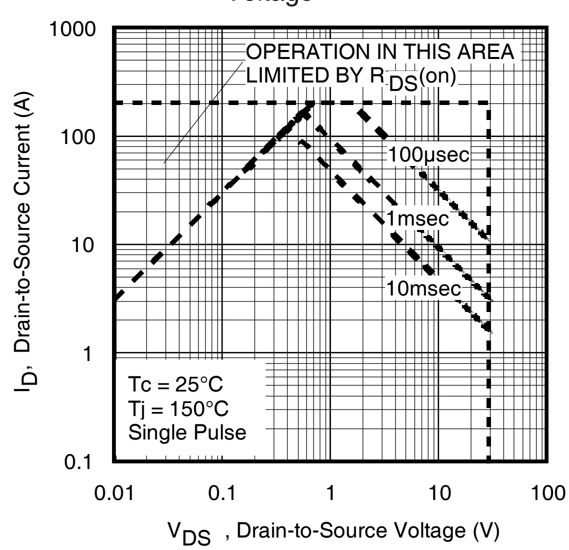


Fig 12. Maximum Safe Operating Area

Typical Characteristics

Q1 - Control FET

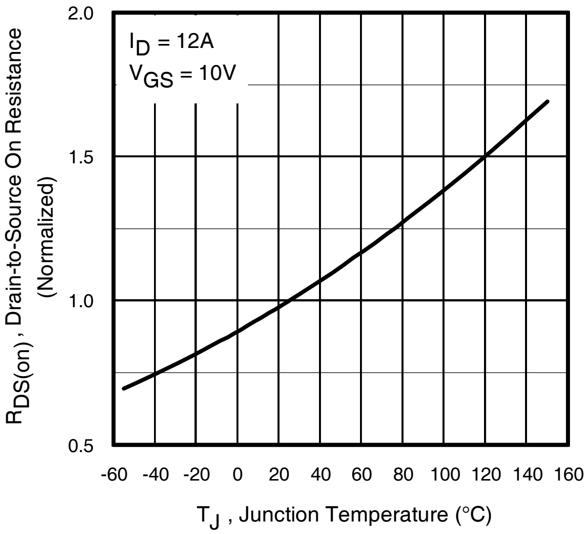


Fig 13. Normalized On-Resistance vs. Temperature

Q2 - Synchronous FET

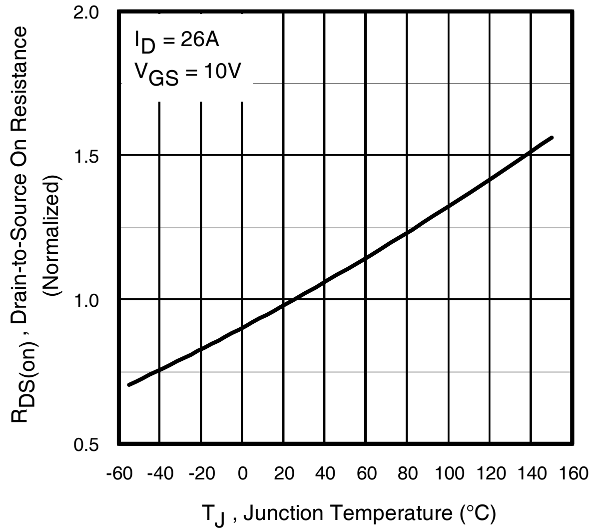


Fig 14. Normalized On-Resistance vs. Temperature

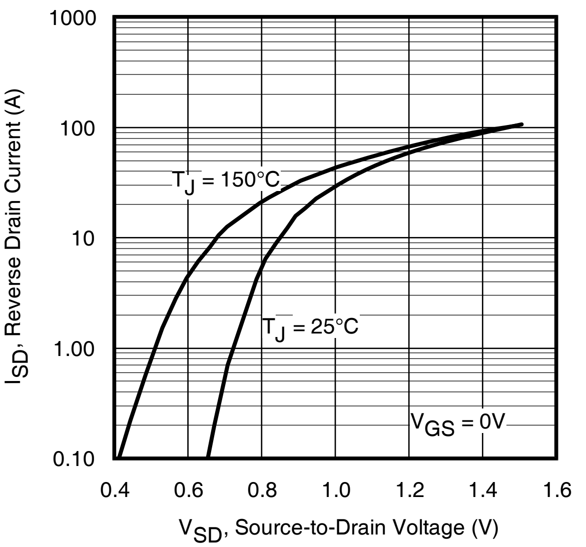


Fig 15. Typical Source-Drain Diode Forward Voltage

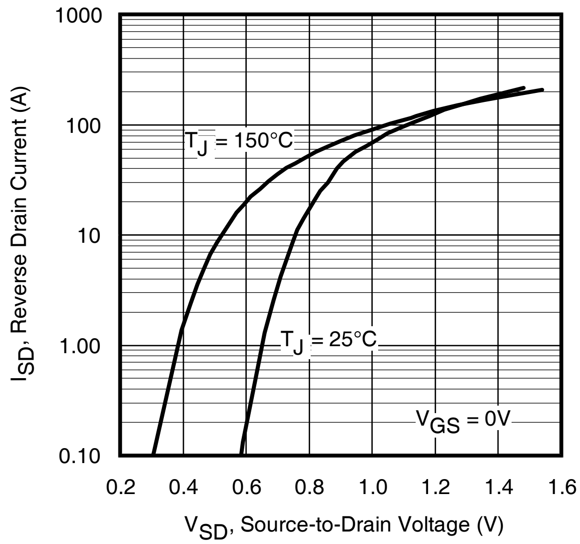


Fig 16. Typical Source-Drain Diode Forward Voltage

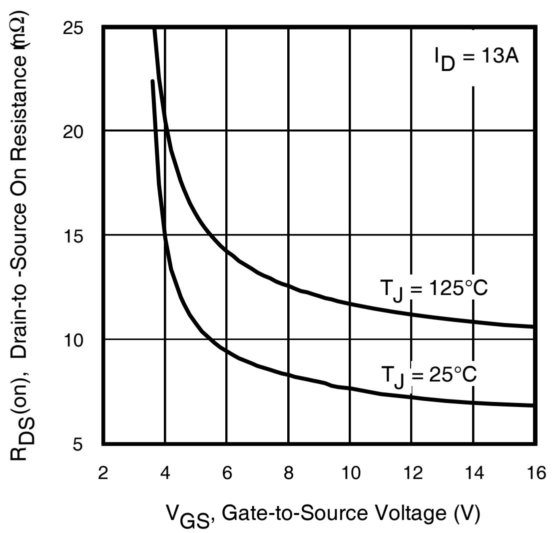


Fig 17. Typical On-Resistance vs.Gate Voltage

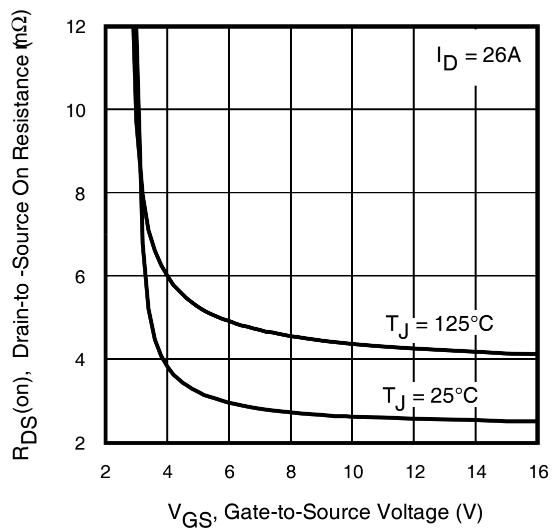


Fig 18. Typical On-Resistance vs.Gate Voltage

Typical Characteristics

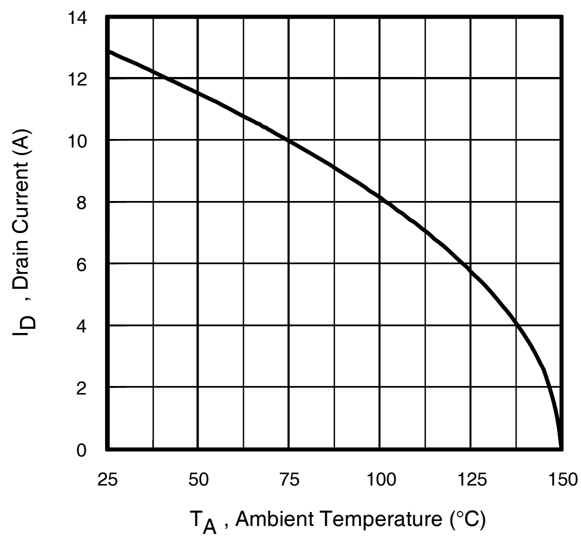


Fig 19. Maximum Drain Current vs. Ambient Temp.

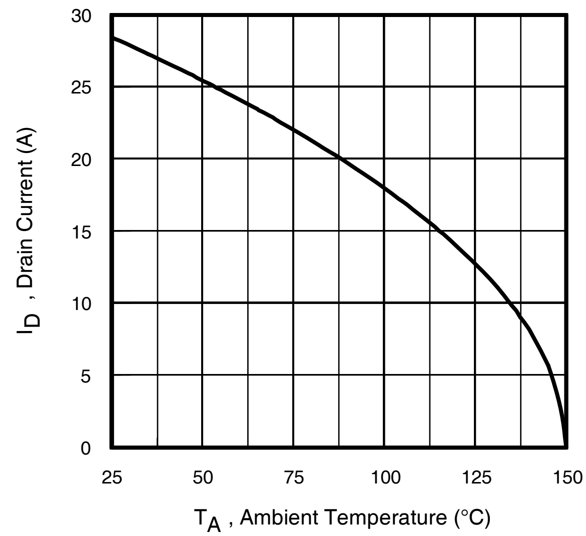


Fig 20. Maximum Drain Current vs. Ambient Temp.

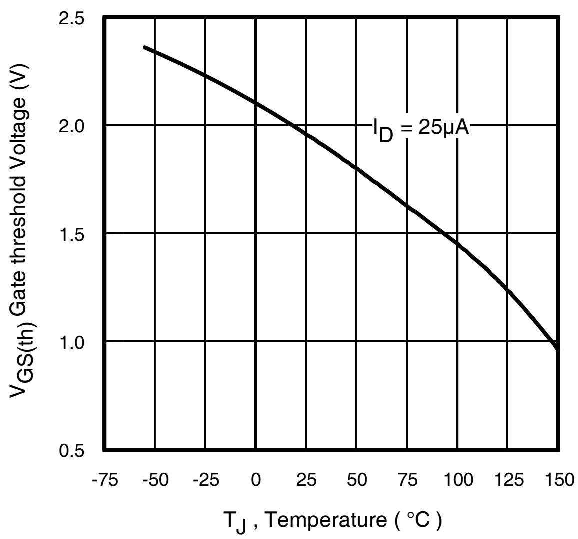


Fig 21. Threshold Voltage vs. Temperature

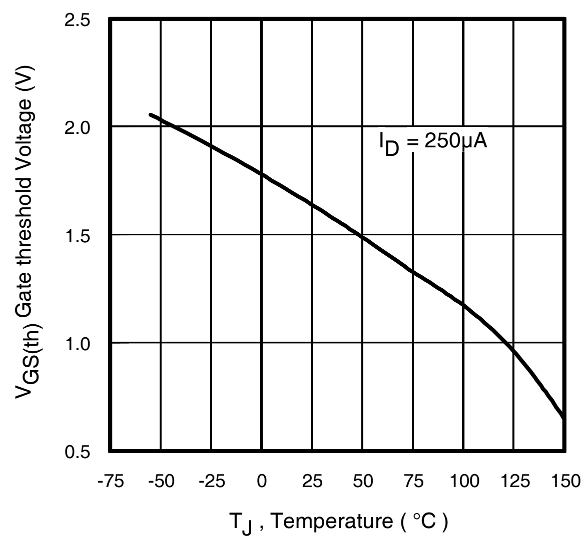


Fig 22. Threshold Voltage vs. Temperature

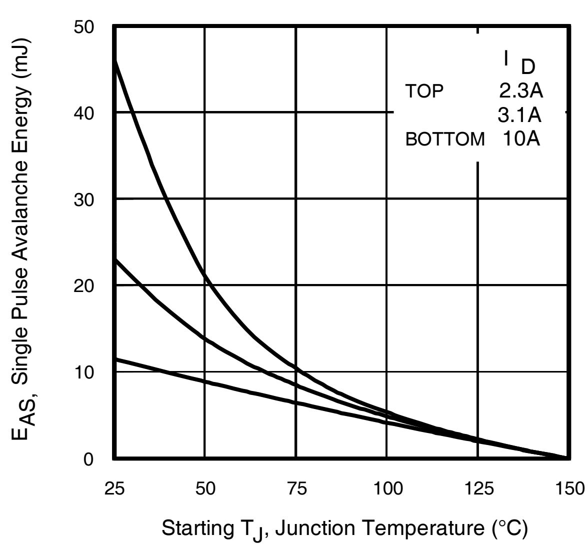


Fig 23. Maximum Avalanche Energy vs. Drain Current

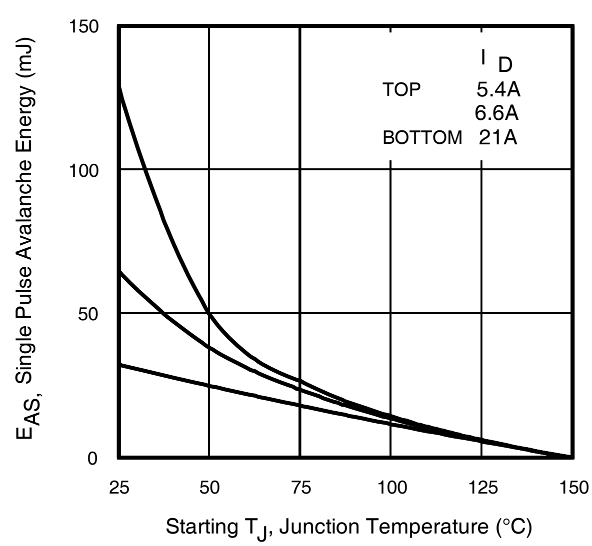


Fig 24. Maximum Avalanche Energy vs. Drain Current

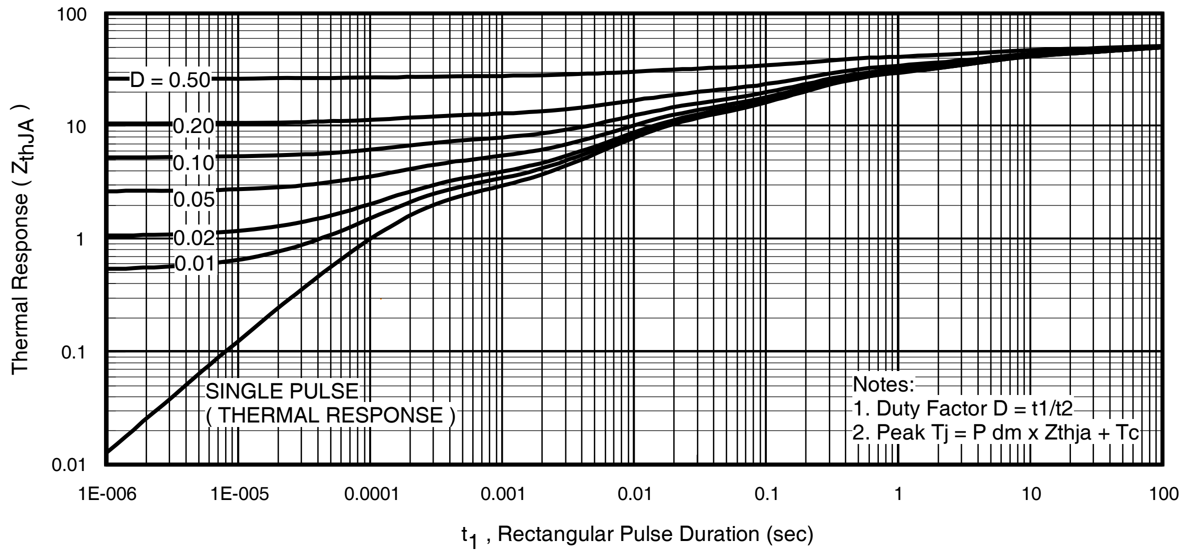


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

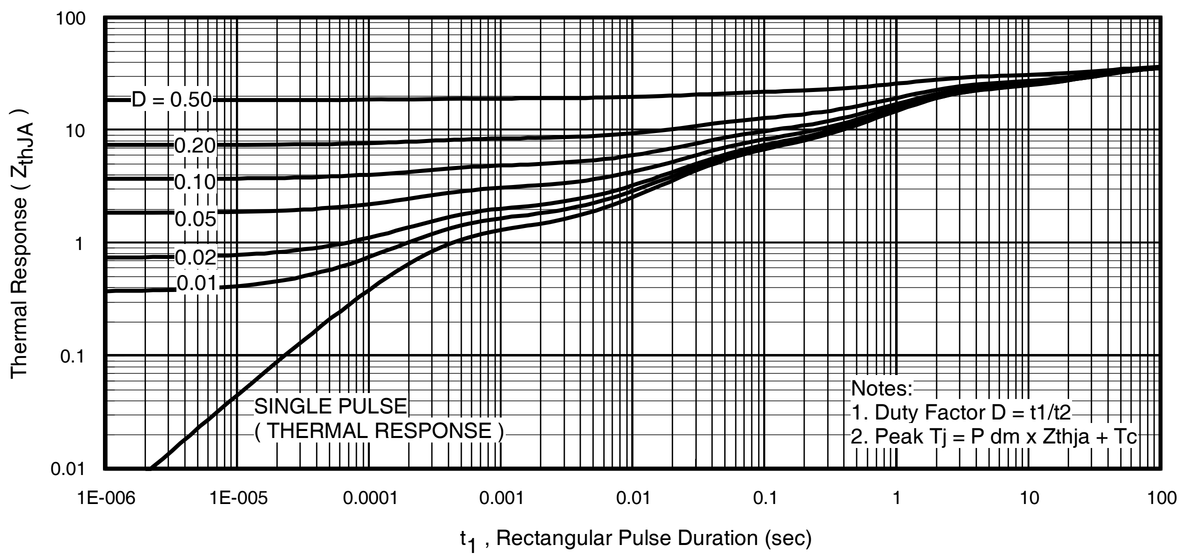


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)

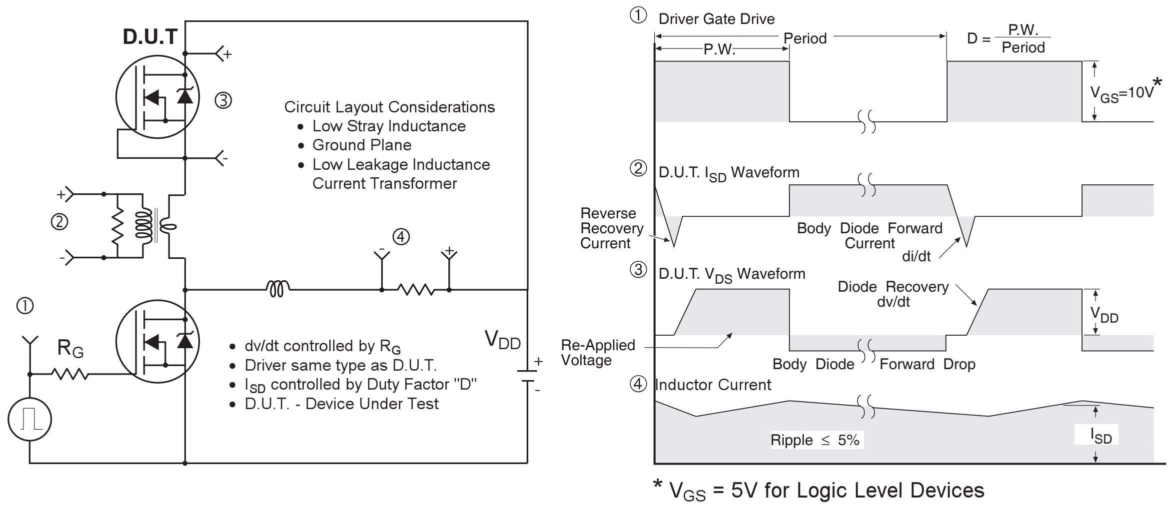


Fig 28. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

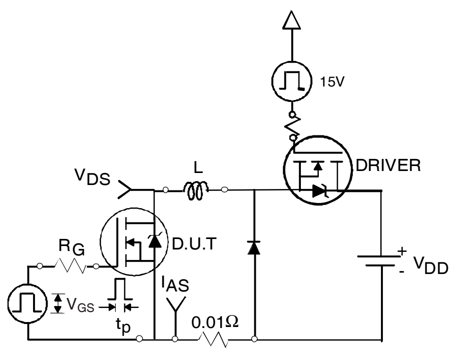


Fig 29a. Unclamped Inductive Test Circuit

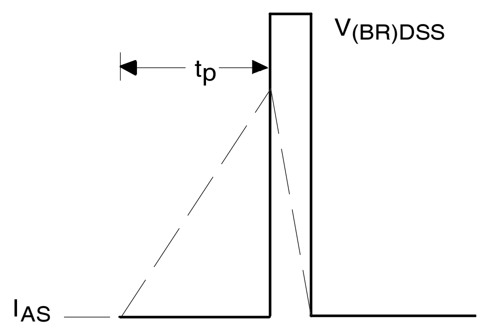


Fig 29b. Unclamped Inductive Waveforms

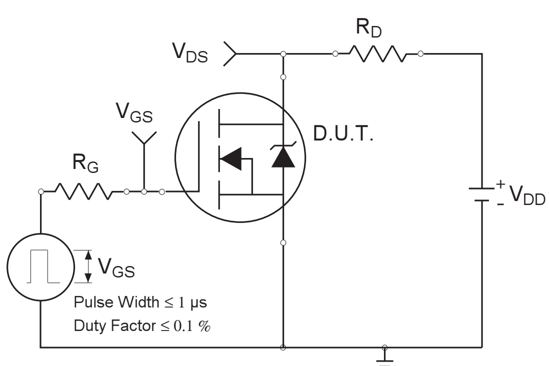


Fig 30a. Switching Time Test Circuit

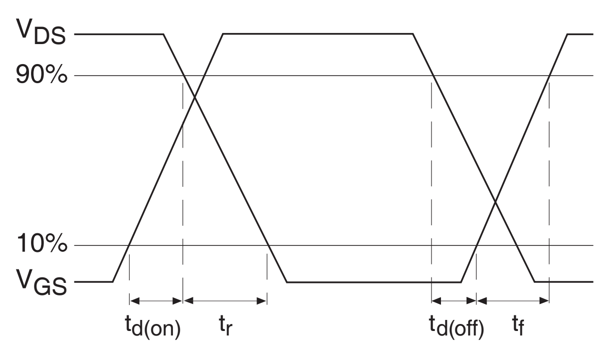


Fig 30b. Switching Time Waveforms

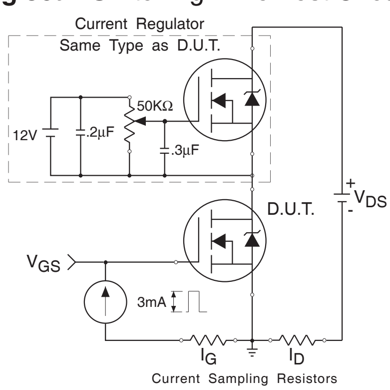


Fig 31a. Gate Charge Test Circuit

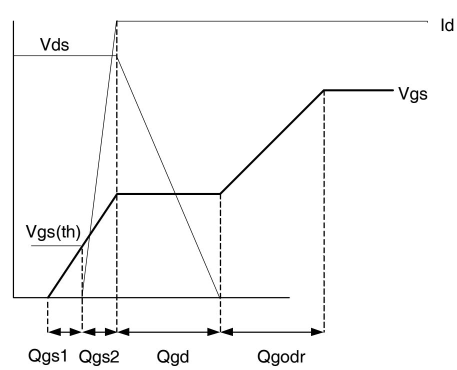
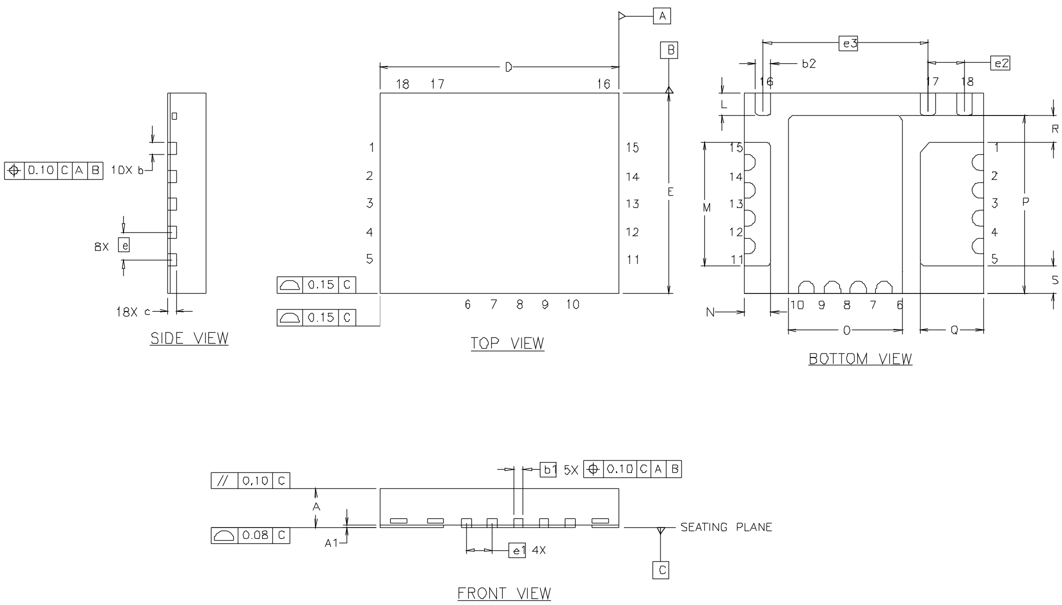


Fig 31b. Gate Charge Waveform

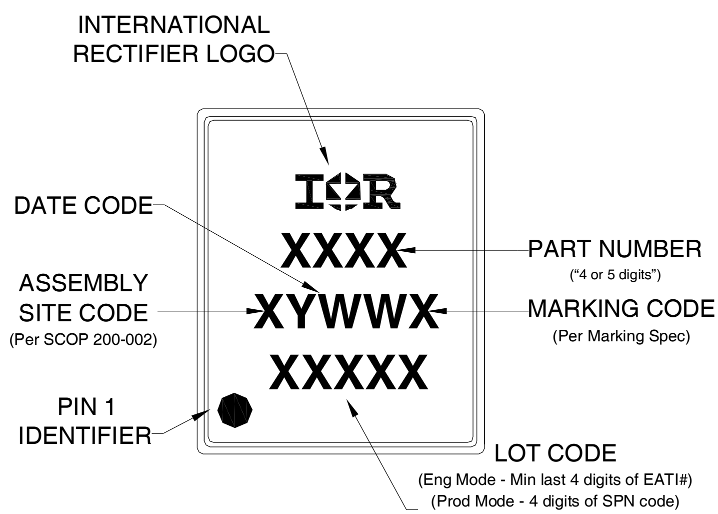
PQFN 5x6 Outline "C" Package Details



Outline PQFN 5X6 C				
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0315	.0394	0.800	1.000
A1	0000	0020	0.000	0.050
b	.0098	.0138	0.250	0.350
b1	.0079	0118	0.200	0.300
b2	.0138	.0177	0.350	0.450
c	.0080 REF.		0.203 REF	
D	.2362 BASIC		6.000 BASIC	
E	.1969 BASIC		5.000 BASIC	
e	.0276 BASIC		0.700 BASIC	
e1	.0256 BASIC		0.650 BASIC	
e2	.0365 BASIC		0.926 BASIC	
e3	.1630 BASIC		4.140 BASIC	
L	.0197	0236	0 500	0.600
M	.1201	1240	3.050	3.150
N	.0243	.0282	.617	.717
O	.1102	1142	2.800	2.900
P	.1732	.1772	4.400	4.500
Q	.0607	.0647	1.543	1.643
R	.0266 REF.		0.675 REF.	
S	.0266 REF.		0.675 REF.	

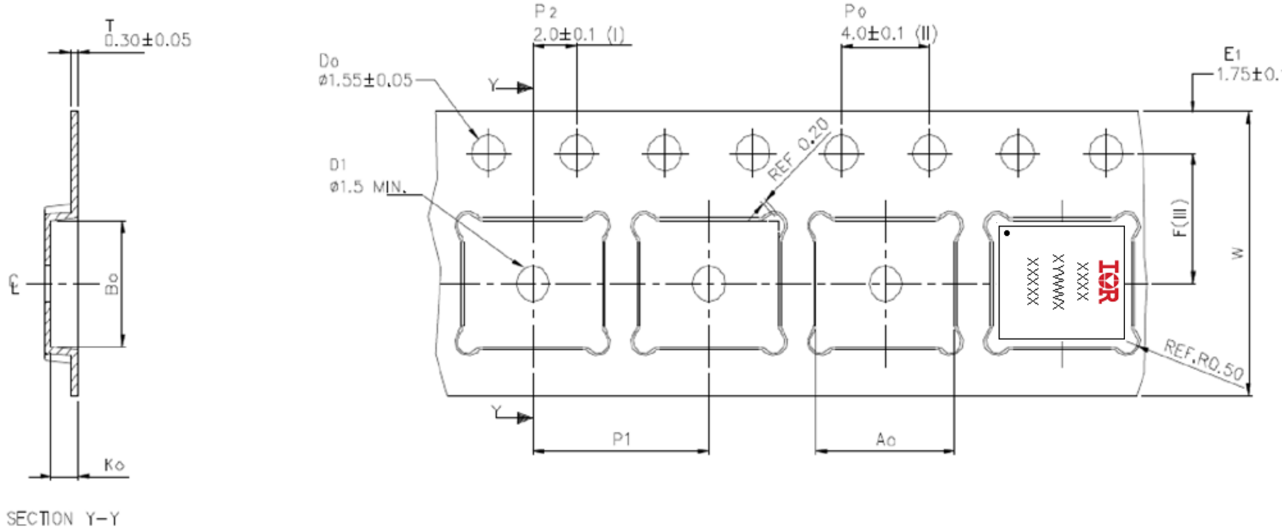
For footprint and stencil design recommendations, please refer to application note AN-1136 at **http://www.irf.com/technical-info/appnotes/an-1136.pdf**

PQFN 5x6 Outline "C" Part Marking



Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

PQFN 5x6 Outline "C" Tape and Reel



Ao	6.30 +/− 0.1
Bo	5.30 +/− 0.1
Ko	1.20 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^9 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Qualification information†

Qualification level	Consumer†† (per JEDEC JESD47F ††† guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL2 †††† (per JEDEC J-STD-020D†††)
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

†††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$,
Q1: $L = 0.23mH$, $R_G = 25\Omega$, $I_{AS} = 10A$;
Q2: $L = 0.15mH$, $R_G = 25\Omega$, $I_{AS} = 21A$.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J approximately 90°C.

Revision History

Date	Comment
1/8/2010	• Pin number on front page drawing has been corrected
7/15/2010	• MSL2 Consumer Qualification on page1 has been corrected
10/25/2011	• Link from AN-1152 to AN-1136 on page 9 has been corrected
5/9/2014	• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259) • Updated data sheet based on corporate template.

International Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/