

IRS2003(S)PbF

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side output in phase with HIN input
- Low-side output out of phase with LIN input
- RoHS compliant

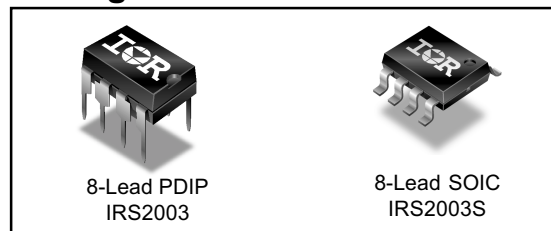
Description

The IRS2003 is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 200 V.

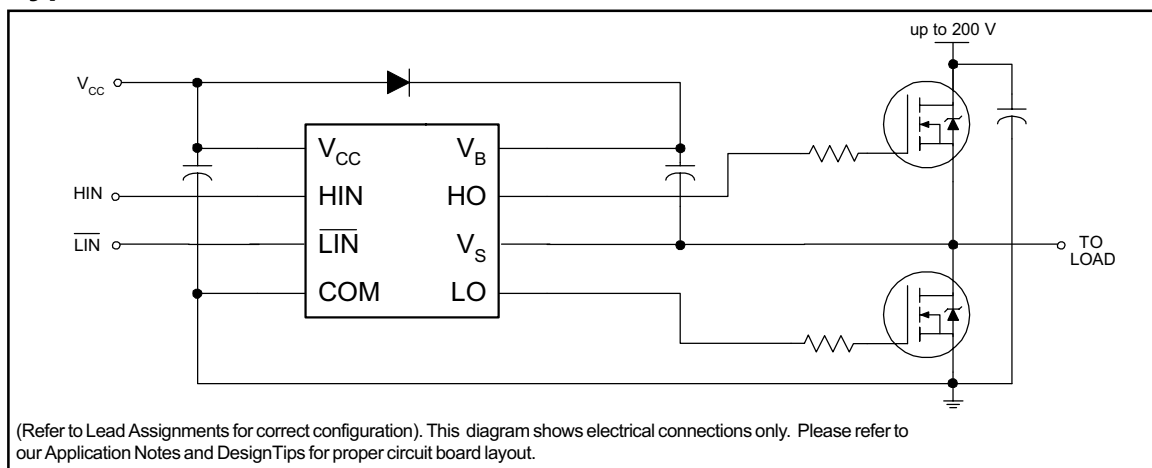
Product Summary

V_{OFFSET}	200 V max.
$I_{\text{O}+/-}$	130 mA/270 mA
V_{OUT}	10 V - 20 V
$t_{\text{on/off}}$ (typ.)	680 ns/150 ns
Deadtime (typ.)	520 ns

Packages



Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V_B	High-side floating absolute voltage	-0.3	225	V	
V_S	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$		
V_{HO}	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25		
V_{LO}	Low-side output voltage	-0.3	$V_{CC} + 0.3$		
V_{IN}	Logic input voltage (HIN & \overline{LIN})	-0.3	$V_{CC} + 0.3$		
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns	
P_D	Package power dissipation @ $T_A \leq +25$ °C	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
R_{thJA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction temperature	—	150	°C	
T_S	Storage temperature	-55	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High-side floating supply offset voltage	Note 1	200	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & \overline{LIN})	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 V to +200 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $C_L = 1000\text{ pF}$ and $T_A = 25\text{ °C}$ unless otherwise specified.

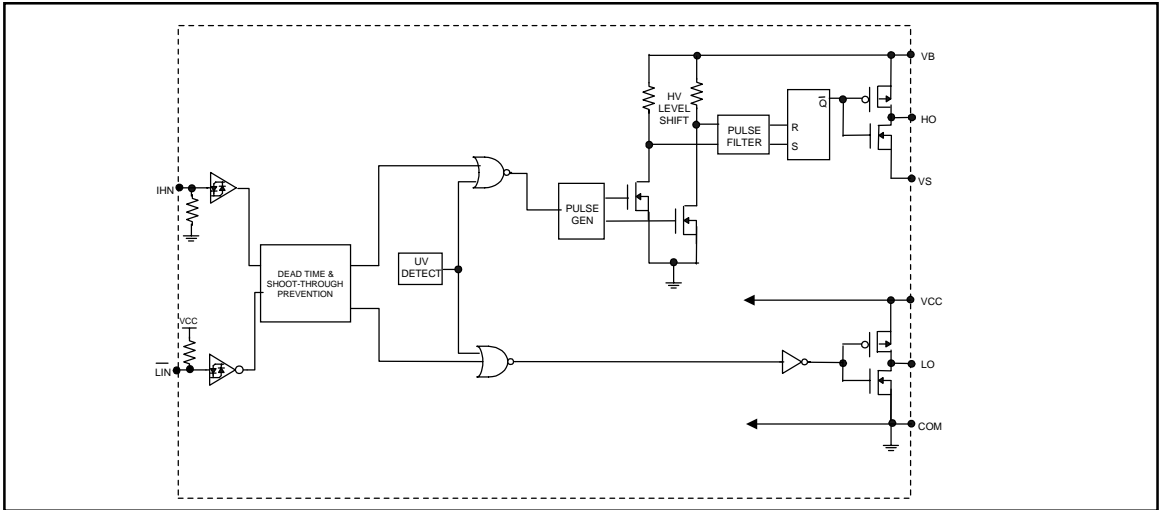
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	$V_S = 0\text{ V}$
t_{off}	Turn-off propagation delay	—	150	220		$V_S = 200\text{ V}$
t_r	Turn-on rise time	—	70	170		
t_f	Turn-off fall time	—	35	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ and $T_A = 25\text{ °C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" (HIN) & Logic "0" (\overline{LIN}) input voltage	2.5	—	—	V	$V_{CC} = 10\text{ V to }20\text{ V}$
V_{IL}	Logic "0" (HIN) & Logic "1" (\overline{LIN}) input voltage	—	—	0.8		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.05	0.2		$I_O = 2\text{ mA}$
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 200\text{ V}$
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		$V_{IN} = 0\text{ V or }5\text{ V}$
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		
I_{IN+}	Logic "1" input bias current	—	3	10		
I_{IN-}	Logic "0" input bias current	—	—	5		HIN = 0 V, $\overline{LIN} = 5\text{ V}$
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	290	—	mA	$V_O = 0\text{ V}$, $V_{IN} = V_{IH}$ $PW \leq 10\text{ }\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	270	600	—		$V_O = 15\text{ V}$, $V_{IN} = V_{IL}$ $PW \leq 10\text{ }\mu\text{s}$

Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high-side gate driver output (HO), in phase
$\overline{\text{LIN}}$	Logic input for low-side gate driver output (LO), out of phase
VB	High-side floating supply
HO	High-side gate drive output
VS	High-side floating supply return
VCC	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments

<p>8 Lead PDIP</p>	<p>8 Lead SOIC</p>
IRS2003PbF	IRS2003SPbF

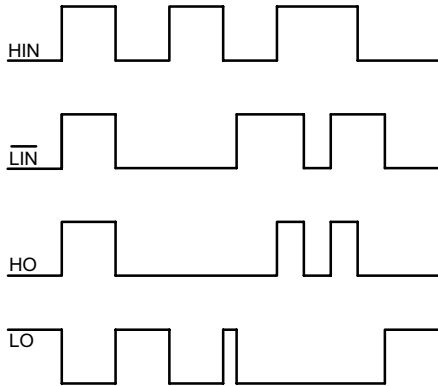


Figure 1. Input/Output Timing Diagram

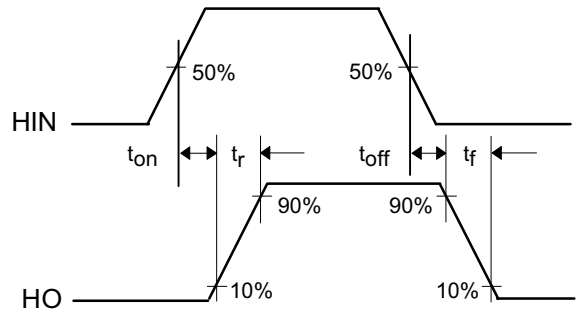
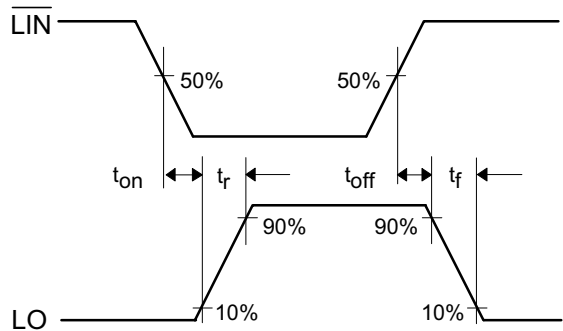


Figure 2. Switching Time Waveform Definitions

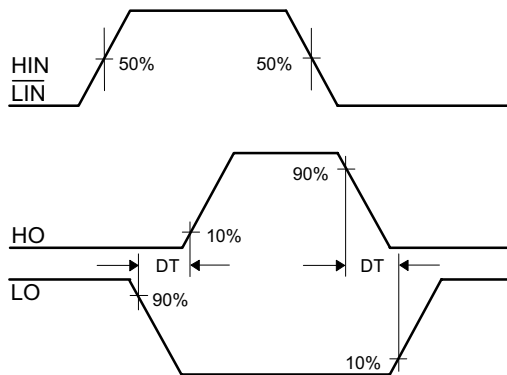


Figure 3. Deadtime Waveform Definitions

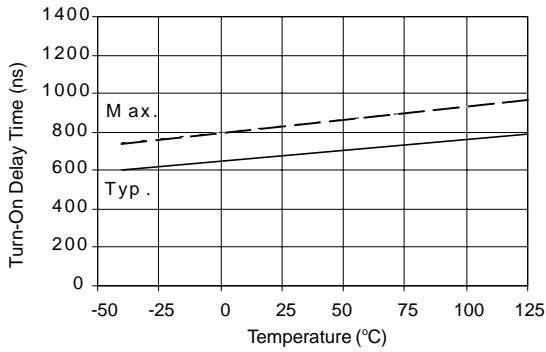


Figure 4A. Turn-On Time vs. Temperature

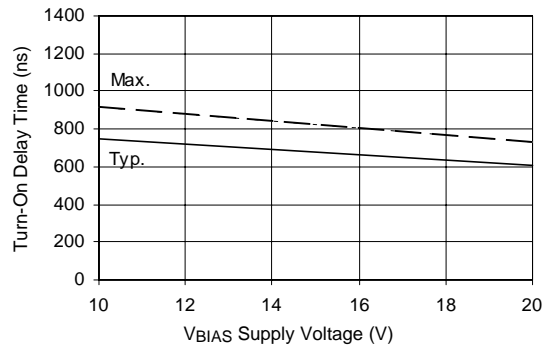


Figure 4B. Turn-On Time vs. Supply Voltage

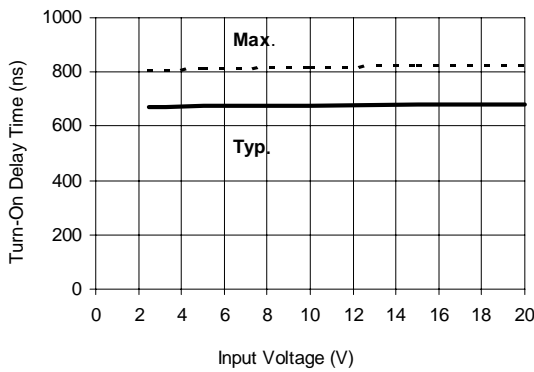


Figure 4C. Turn-On Time vs. Input Voltage

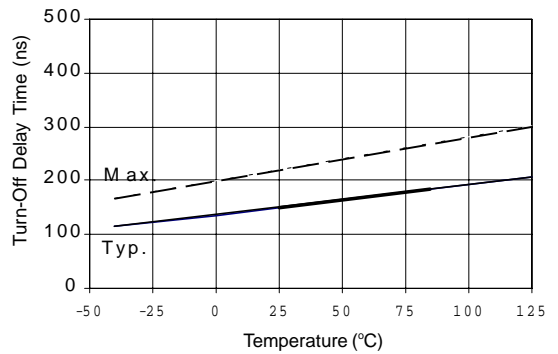


Figure 5A. Turn-Off Time vs. Temperature

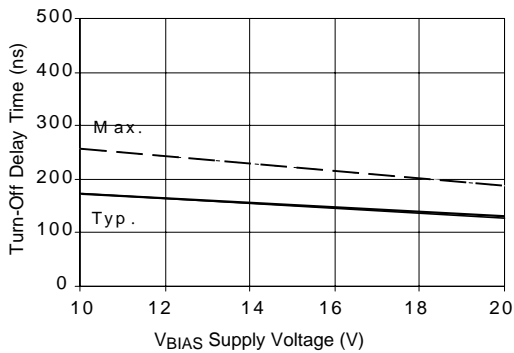


Figure 5B. Turn-Off Time vs. Supply Voltage

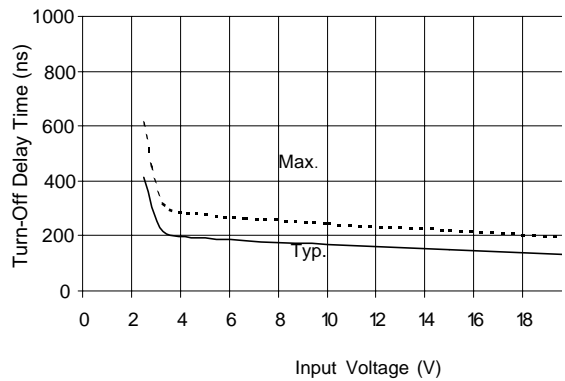


Figure 5C. Turn-Off Time vs. Input Voltage

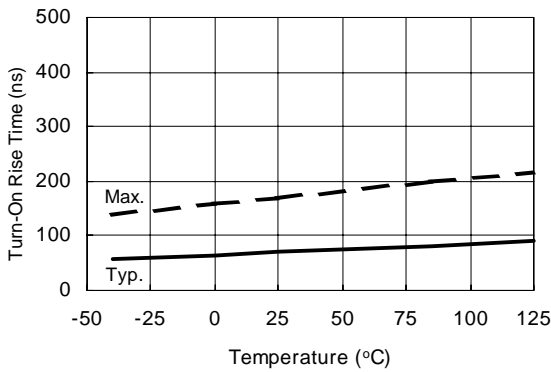


Figure 6A. Turn-On Rise Time vs. Temperature

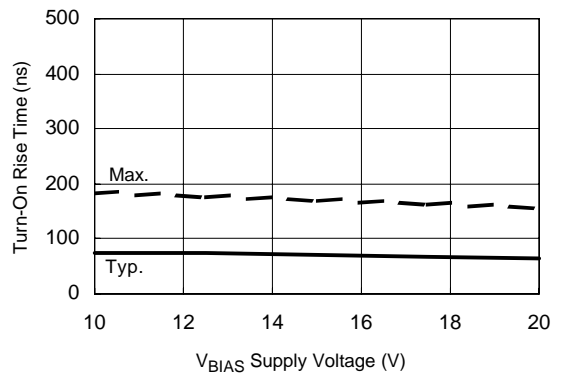


Figure 6B. Turn-On Rise Time vs. Voltage

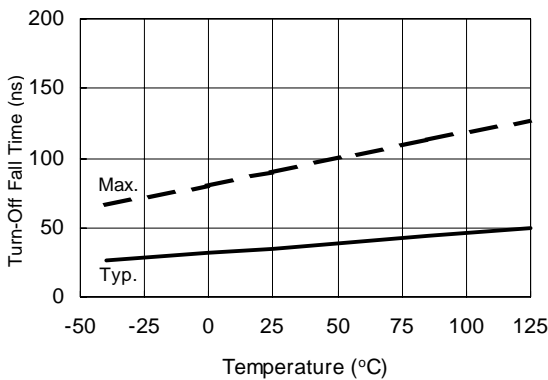


Figure 7A. Turn-Off Fall Time vs. Temperature

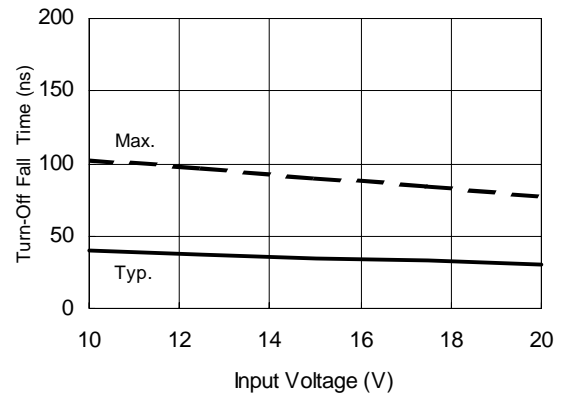


Figure 7B. Turn-Off Fall Time vs. Voltage

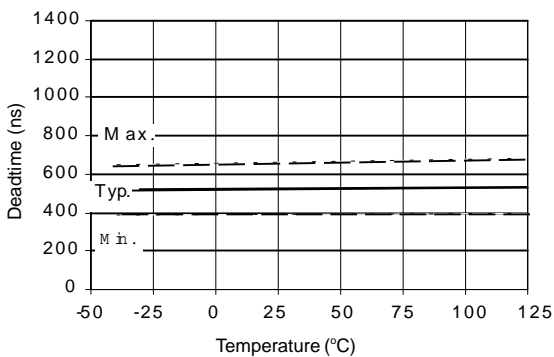


Figure 8A. Deadtime vs. Temperature

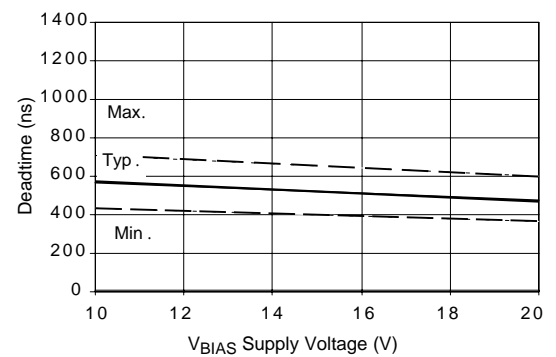


Figure 8B. Deadtime vs. Voltage

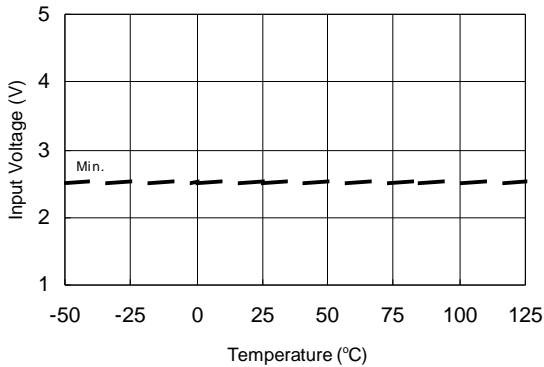


Figure 9A. Logic "1" Input Voltage vs. Temperature

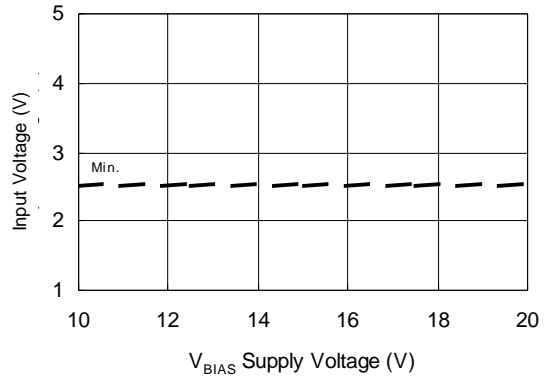


Figure 9B. Logic "1" Input Voltage vs. Supply Voltage

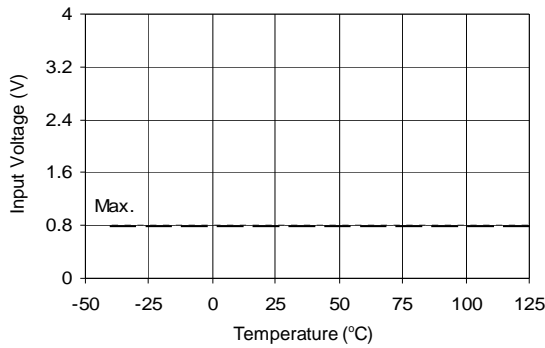


Figure 10A. Logic "0" (HIN) & Logic "1" (LIN) Input Voltage vs. Temperature

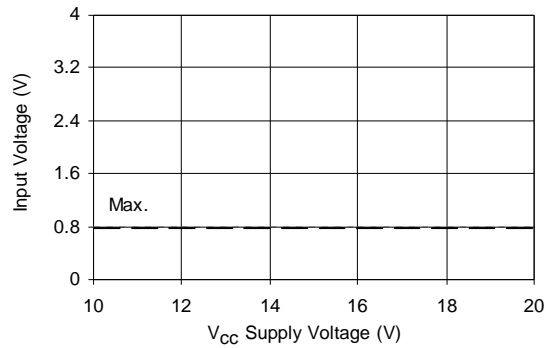


Figure 10B. Logic "0" (HIN) & Logic "1" (LIN) Input Voltage vs. Voltage

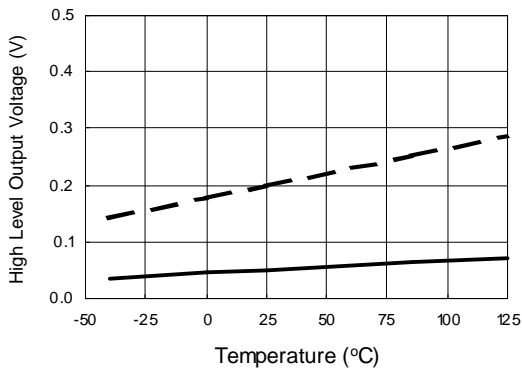


Figure 11A. High Level Output Voltage vs. Temperature

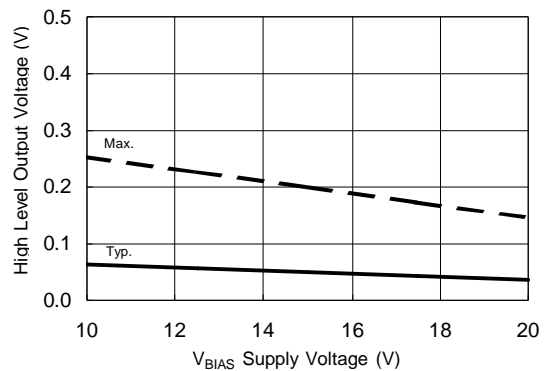


Figure 11B. High Level Output Voltage vs. Supply Voltage

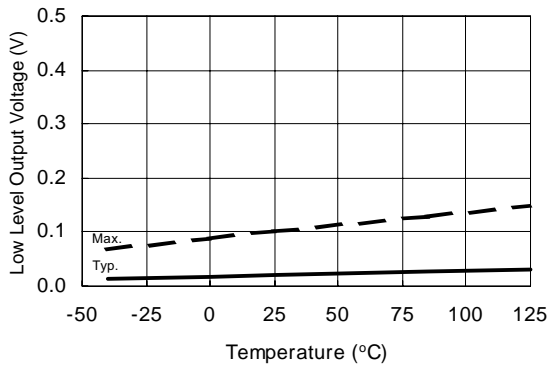


Figure 12A. Low Level Output Voltage vs. Temperature

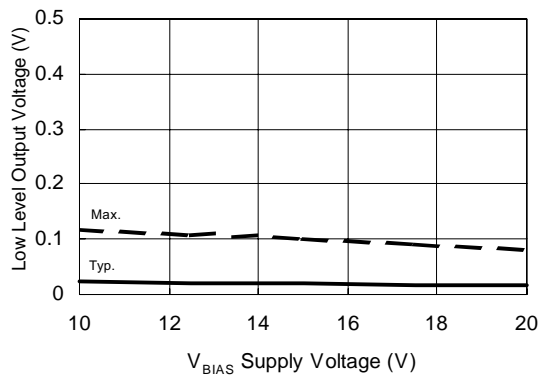


Figure 12B. Low Level Output Voltage vs. Supply Voltage

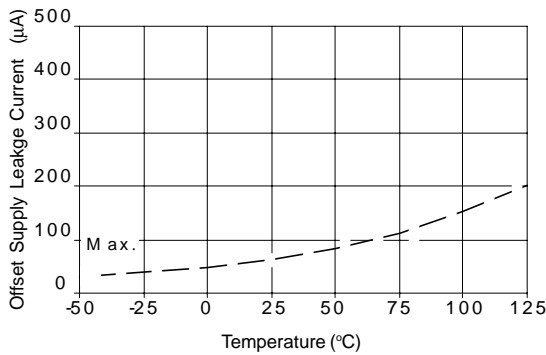


Figure 13A. Offset Supply Current vs. Temperature

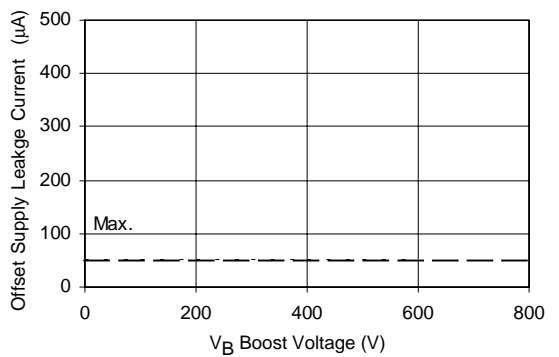


Figure 13B. Offset Supply Current vs. Voltage

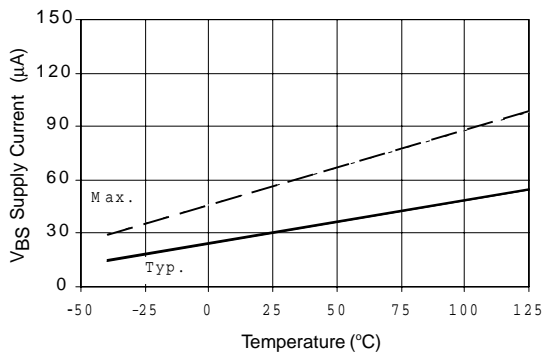


Figure 14A. VBS Supply Current vs. Temperature

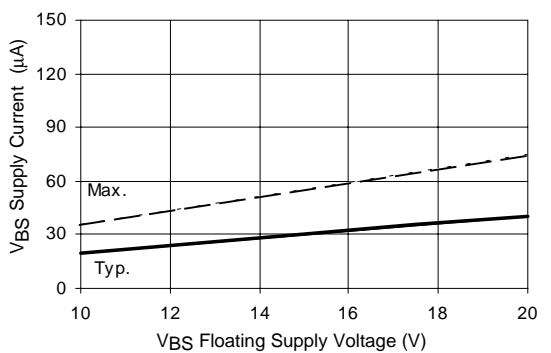


Figure 14B. VBS Supply Current vs. Voltage

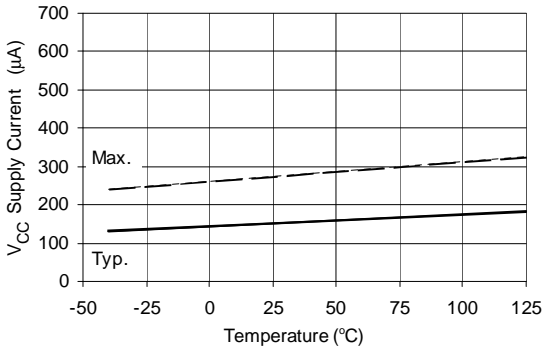


Figure 15A. V_{CC} Supply Current vs. Temperature

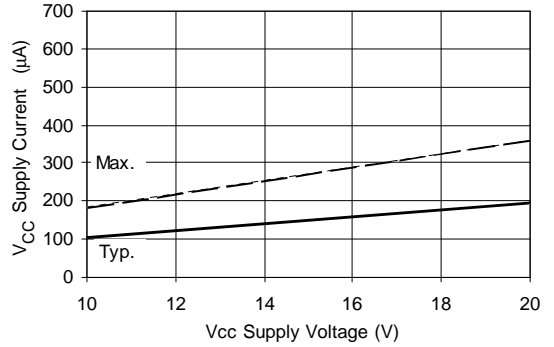


Figure 15B. V_{CC} Supply Current vs. Voltage

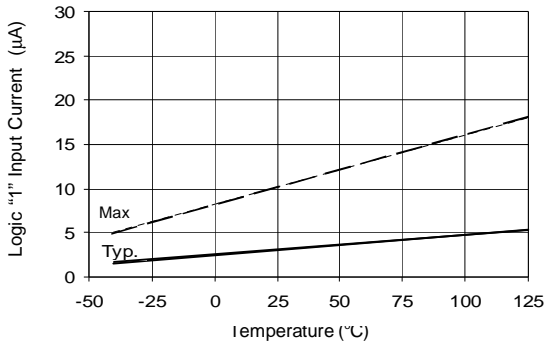


Figure 16A. Logic "1" Input Current vs. Temperature

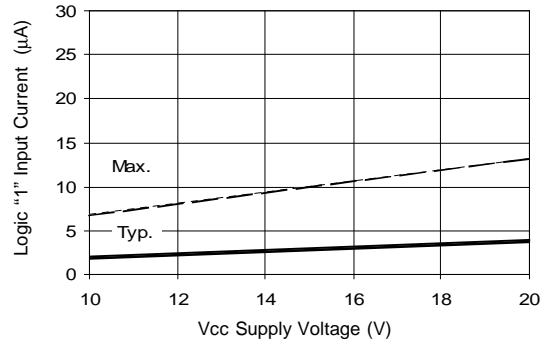


Figure 16B. Logic "1" Input Current vs. Voltage

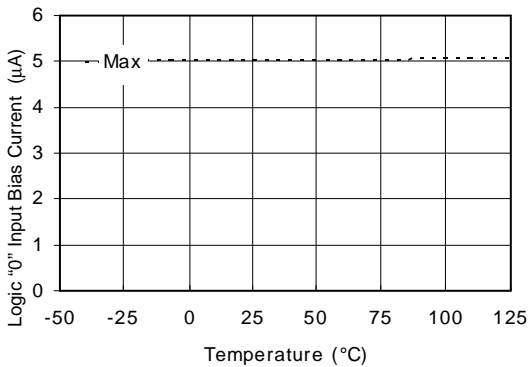


Figure 17A. Logic "0" Input Bias Current vs. Temperature

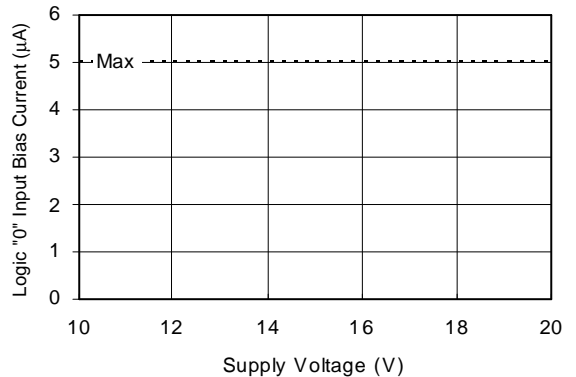


Figure 17B. Logic "0" Input Bias Current vs. Voltage

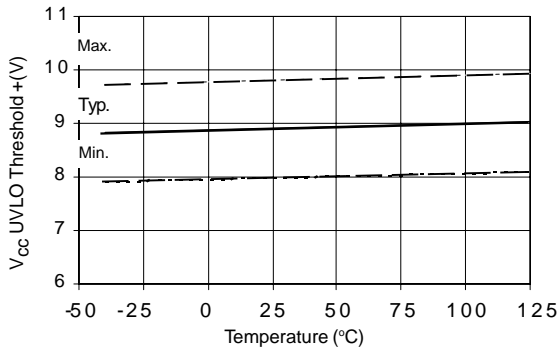


Figure 18A. V_{CC} Undervoltage Threshold(+) vs. Temperature

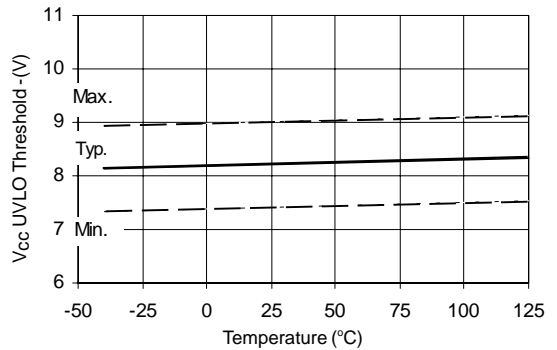


Figure 18B. V_{CC} Undervoltage Threshold (-) vs. Temperature

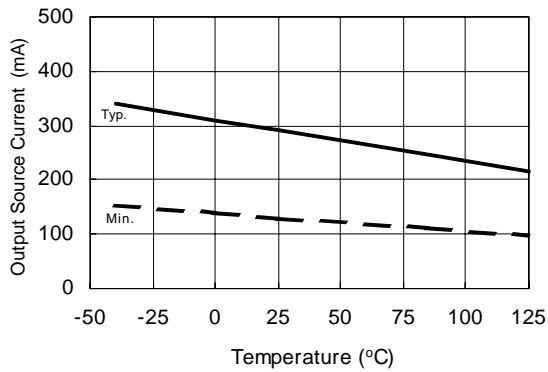


Figure 19A. Output Source Current vs. Temperature

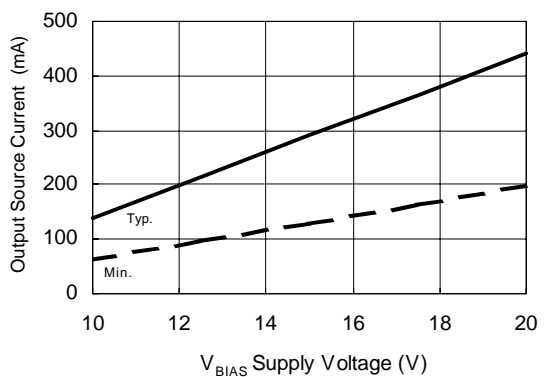


Figure 19B. Output Source Current vs. Supply Voltage

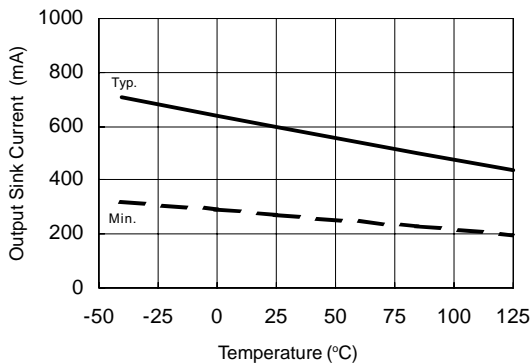


Figure 20A. Output Sink Current vs. Temperature

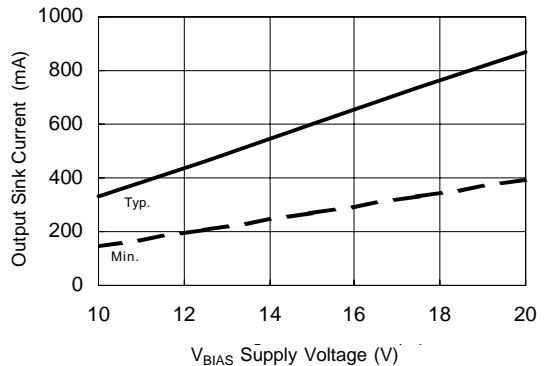


Figure 20B. Output Sink Current vs. Supply Voltage

Case Outlines

Technical drawing of an 8-Lead PDIP package. The drawing includes a top view showing lead positions 1-8, a side view showing lead height and package height, and a lead view showing lead width and pitch. Dimensions are provided in millimeters [inches].

Dimensions:

- Top view: 10.92 [.430] (total width), 8.84 [.348] (lead width), 7.11 [.280] (package width), 6.10 [.240] (lead width).
- Side view: 1.77 [.070] (lead height), 1.15 [.045] (lead height), 1.27 [.050] (lead height), 5.33 [.210] MAX (package height).
- Lead view: 0.39 [.015] MIN (lead thickness), 4.06 [.160] (lead length), 2.93 [.115] (lead length), 2.54 [.100] 6X (lead length), 0.558 [.022] 8X (lead pitch), 0.356 [.014] (lead pitch).
- Lead view: 7.62 [.300] 5 (lead length), 0.381 [.015] 8X (lead length), 0.204 [.008] (lead length).

Notes:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
- 5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

8-Lead PDIP 01-6014
01-3003 01 (MS-001AB)

Technical drawing of an 8-Lead SOIC package. The drawing includes a top view showing lead positions 1-8, a side view showing lead height and package height, and a footprint view showing lead pitch and length. Dimensions are provided in millimeters and inches.

Dimensions:

- Top view: D (total width), B (lead width), H (package height), 0.25 [.010] (lead pitch), A (lead length), E (lead length), 6X e (lead length).
- Side view: e1 (lead height), A (lead height), C (lead height), 0.10 [.004] (lead height), 8X b (lead length), A1 (lead length).
- Footprint: 8X 0.72 [.028] (lead pitch), 6.46 [.255] (lead length), 3X 1.27 [.050] (lead length), 8X 1.78 [.070] (lead length), K x 45° (lead angle), 8X L (lead length), 8X c (lead length).

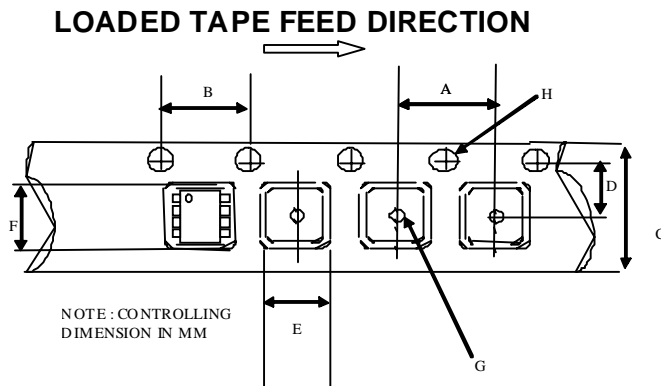
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

Notes:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- 5 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.15 [.006].
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.25 [.010].
- 7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

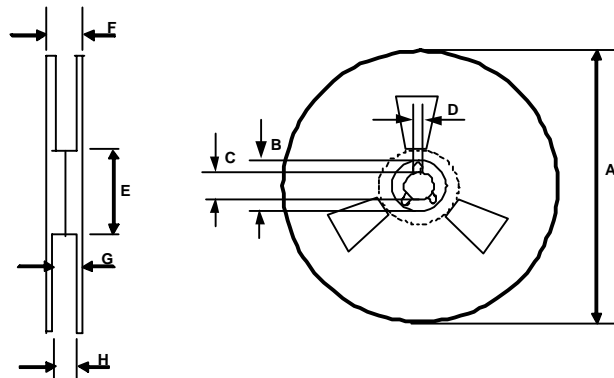
8-Lead SOIC 01-6027
01-0021 11 (MS-012AA)

Tape & Reel 8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

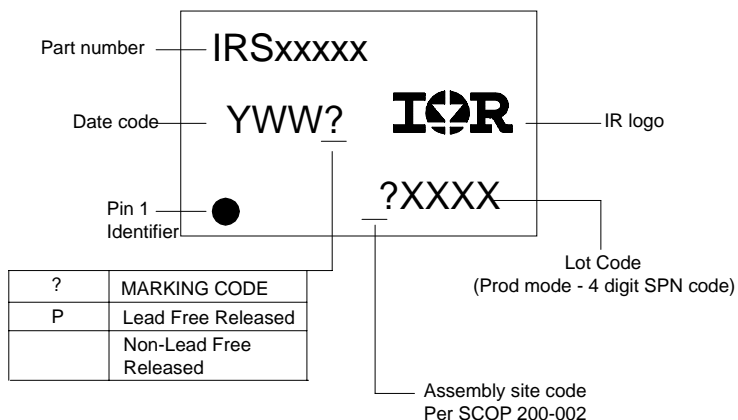
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

8-Lead PDIP IRS2003PbF
 8-Lead SOIC IRS2003SPbF
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