

# TVS Diodes

Transient Voltage Suppressor Diodes

## ESD5V5U5ULC

Ultra-low Capacitance ESD / Transient / Surge Protection Array

ESD5V5U5ULC

## Data Sheet

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Final

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# 1 Ultra-low Capacitance ESD / Transient / Surge Protection Array

## 1.1 Features

- ESD / Transient protection of high speed data lines exceeding
  - IEC61000-4-2 (ESD):  $\pm 25$  kV (air / contact)
  - IEC61000-4-4 (EFT):  $\pm 2.5$  kV /  $\pm 50$  A (5/50 ns)
  - IEC61000-4-5 (surge):  $\pm 6$  A (8/20  $\mu$ s)
- Maximum working voltage:  $V_{RWM} = 5.5$  V
- Extremely low capacitance  $C_L = 0.45$  pF I/O to GND (typical)
- Very low dynamic resistance:  $R_{DYN}$  I/O to GND =  $0.2 \Omega$  (typical)
- Very low reverse clamping voltage:  $V_{CL} = 9$  V (typical) at  $I_{PP} = 16$  A
- Protection of  $V_{BUS}$  with one line freely selectable
- Pb-free (RoHS compliant) package



## 1.2 Application Examples

- Protection of all I/O and  $V_{BUS}$  lines in dual USB2.0 ports
- 10/100/1000 Ethernet
- DVI, HDMI, FireWire

## 1.3 Product Description

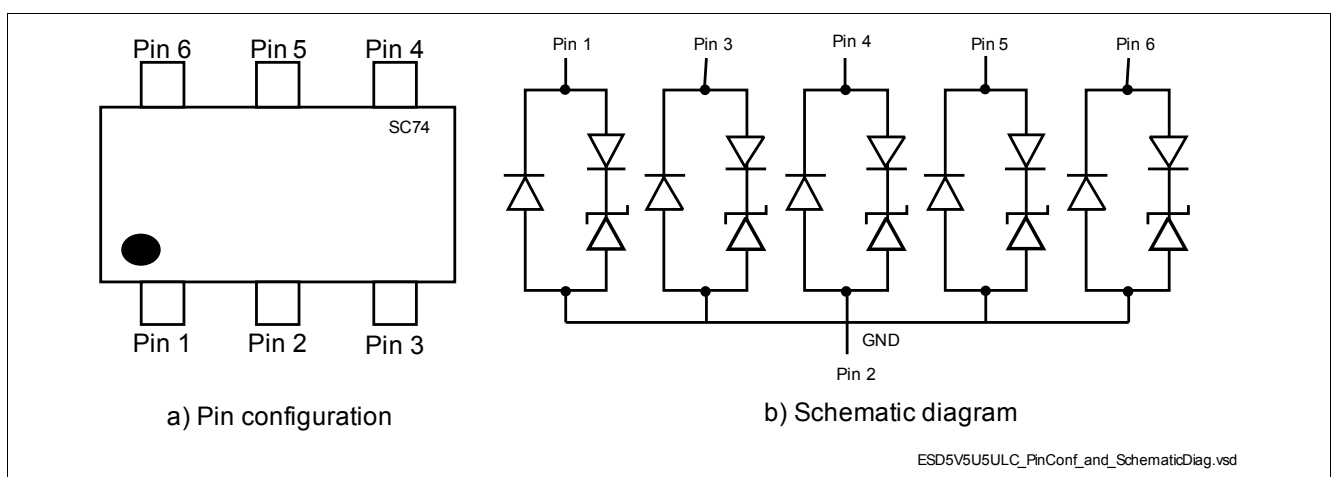


Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD5V5U5ULC	SC74	5 lines, uni-directional	20

## 2 Characteristics

**Table 2** Maximum Rating at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

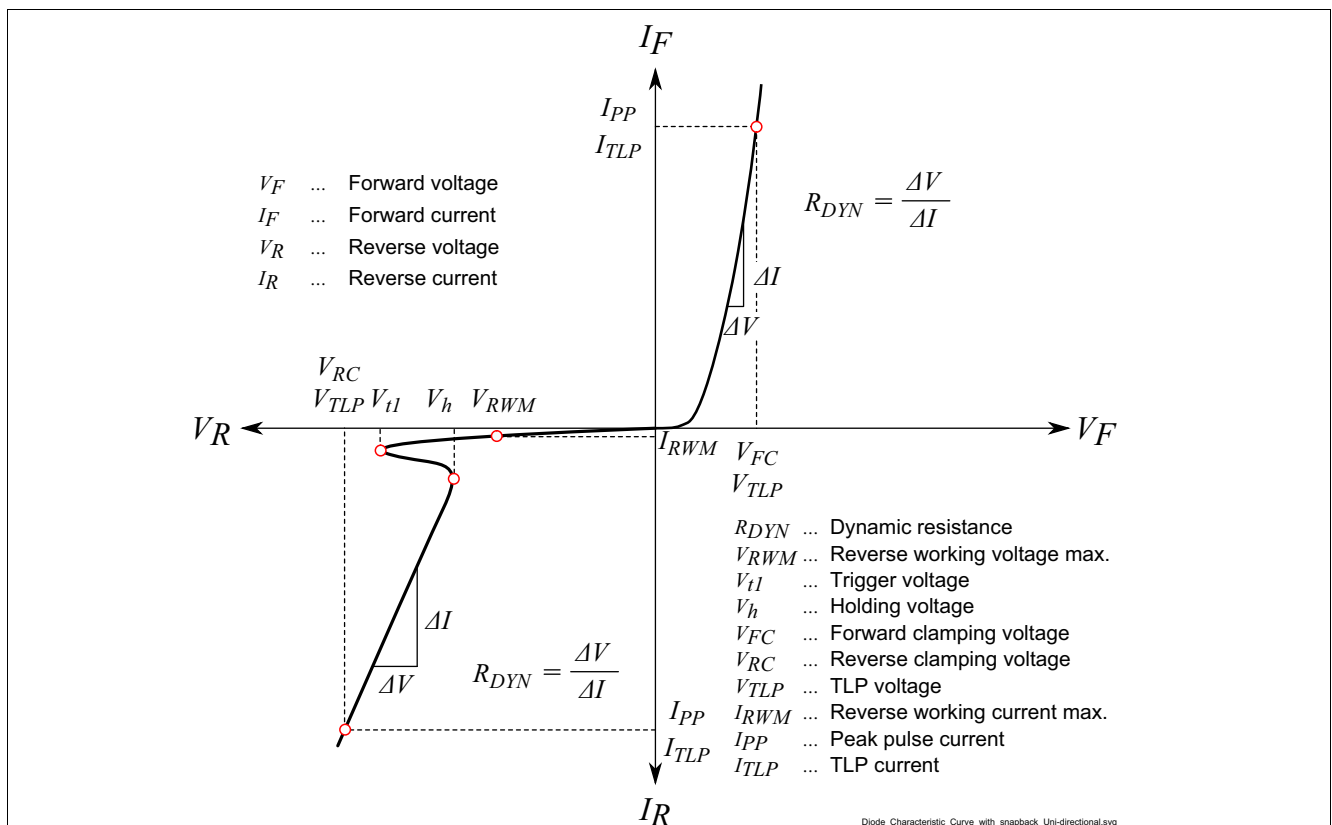
Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge <sup>1)</sup>	$V_{ESD}$	-25	–	25	kV
Peak pulse current ( $t_p = 8/20\text{ }\mu\text{s}$ ) <sup>2)</sup>	$I_{PP}$	-6	–	6	A
Operating temperature range	$T_{OP}$	-40	–	125	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65	–	150	$^\circ\text{C}$

1)  $V_{ESD}$  according to IEC61000-4-2

2)  $I_{PP}$  according to IEC61000-4-5

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

### 2.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified



**Figure 2** Definitions of Electrical Characteristics[1]

**Characteristics**
**Table 3 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	–	–	5.5	V	I/O to GND
Reverse current	$I_R$	–	<1	100	nA	$V_R = 5.5\text{ V}$ , I/O to GND

**Table 4 RF Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	–	0.45	1	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to GND
		–	0.23	0.5	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to I/O
Line capacitance	$C_L$	–	0.25	–	pF	$V_R = 0\text{ V}$ , $f = 825\text{ MHz}$ , I/O to GND
		–	0.13	–	pF	$V_R = 0\text{ V}$ , $f = 825\text{ MHz}$ , I/O to I/O
Capacitance variation between I/O and GND	$\Delta C_{i/o-GND}$	–	0.02	–	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to GND
Capacitance variation between I/O	$\Delta C_{i/o-i/o}$	–	0.01	–	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to I/O

**Table 5 ESD Characteristics at  $T_A = 25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse clamping voltage <sup>1)</sup>	$V_{CL}$	–	9	–	V	$I_{PP} = 1\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , I/O pin to GND
		–	12	–	V	$I_{PP} = 3\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , I/O pin to GND
Reverse clamping voltage <sup>2)</sup> [2]	$V_{CL}$	–	8.9	–	V	$I_{PP} = 16\text{ A}$ , $t_p = 100\text{ ns}$ , I/O pin to GND
		–	11.5	–	V	$I_{PP} = 30\text{ A}$ , $t_p = 100\text{ ns}$ , I/O pin to GND
Forward clamping voltage <sup>1)</sup>	$V_{FC}$	–	1.75	–	V	$I_{PP} = 1\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , GND pin to I/O
		–	2.5	–	V	$I_{PP} = 3\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , GND pin to I/O
Forward clamping voltage <sup>2)</sup> [2]	$V_{FC}$	–	5.4	–	V	$I_{PP} = 16\text{ A}$ , $t_p = 100\text{ ns}$ , GND pin to I/O
		–	9.2	–	V	$I_{PP} = 30\text{ A}$ , $t_p = 100\text{ ns}$ , GND pin to I/O
Dynamic resistance I/O to GND <sup>2)</sup> [2]	$R_{DYN, I/O}$ to GND	–	0.2	–	$\Omega$	
Dynamic resistance GND to I/O <sup>2)</sup> [2]	$R_{DYN,}$ GND to I/O	–	0.3	–	$\Omega$	

1)  $I_{PP}$  according to IEC61000-4-5

2) Please refer to Application Note AN210[2]. TLP parameter:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{PP1} = 10\text{ A}$  and  $I_{PP2} = 40\text{ A}$ .

2.2 Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

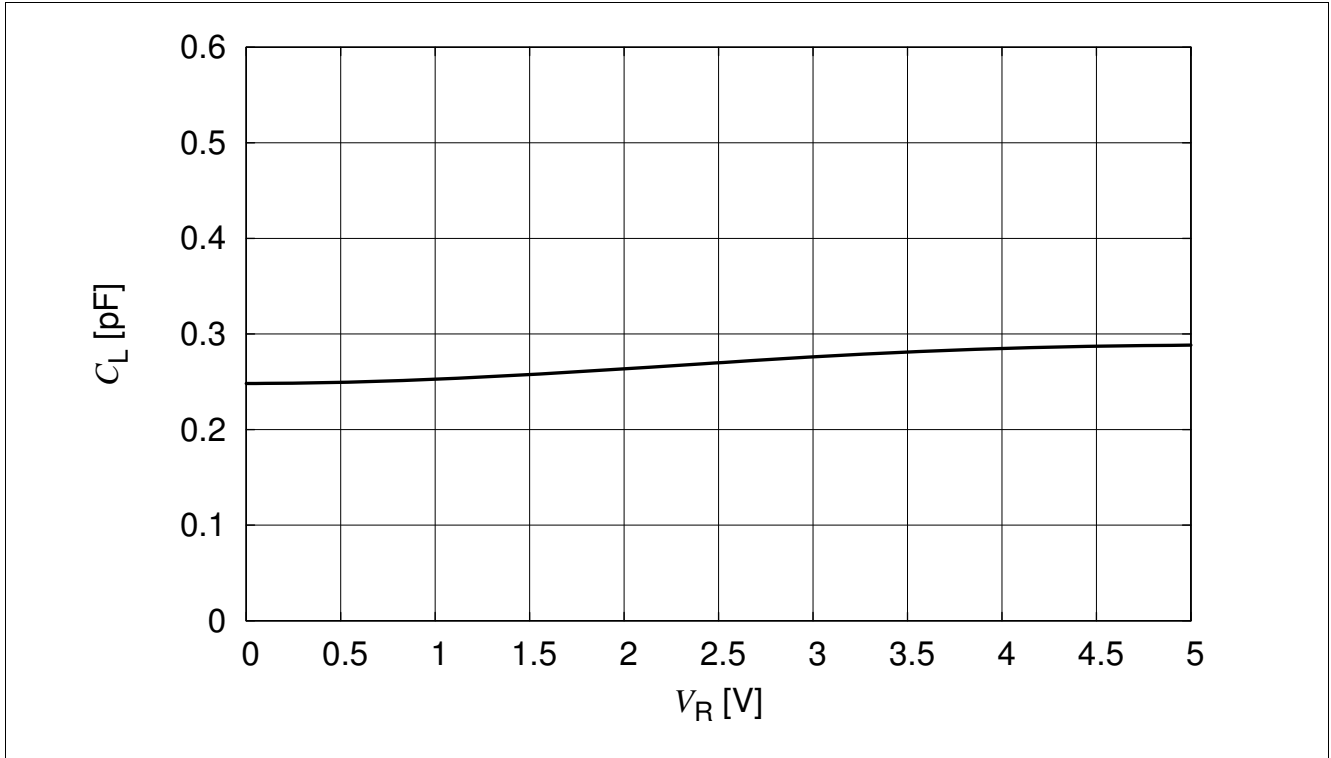


Figure 3 Line capacitance  $C_L = f(V_R)$  at  $f = 825\text{ MHz}$

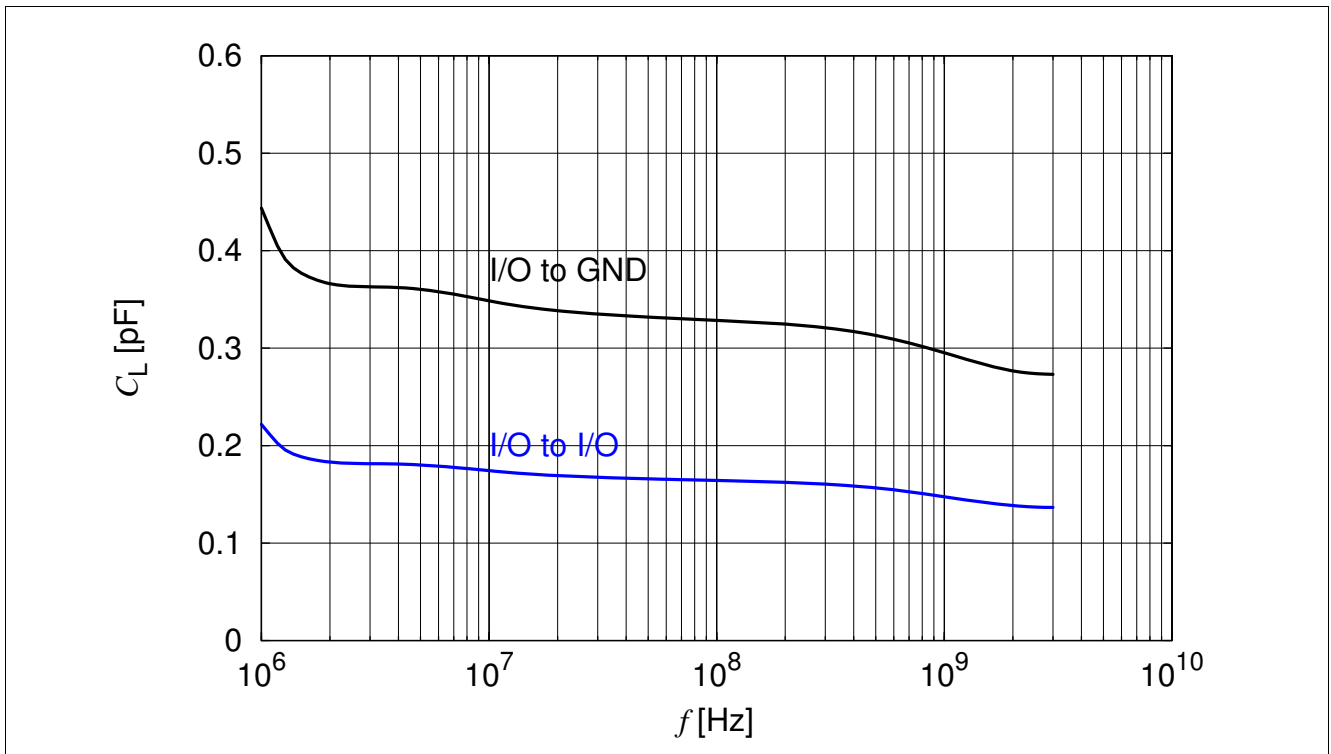


Figure 4 Line capacitance  $C_L = f(f)$ ,  $V_R = 0\text{ V}$

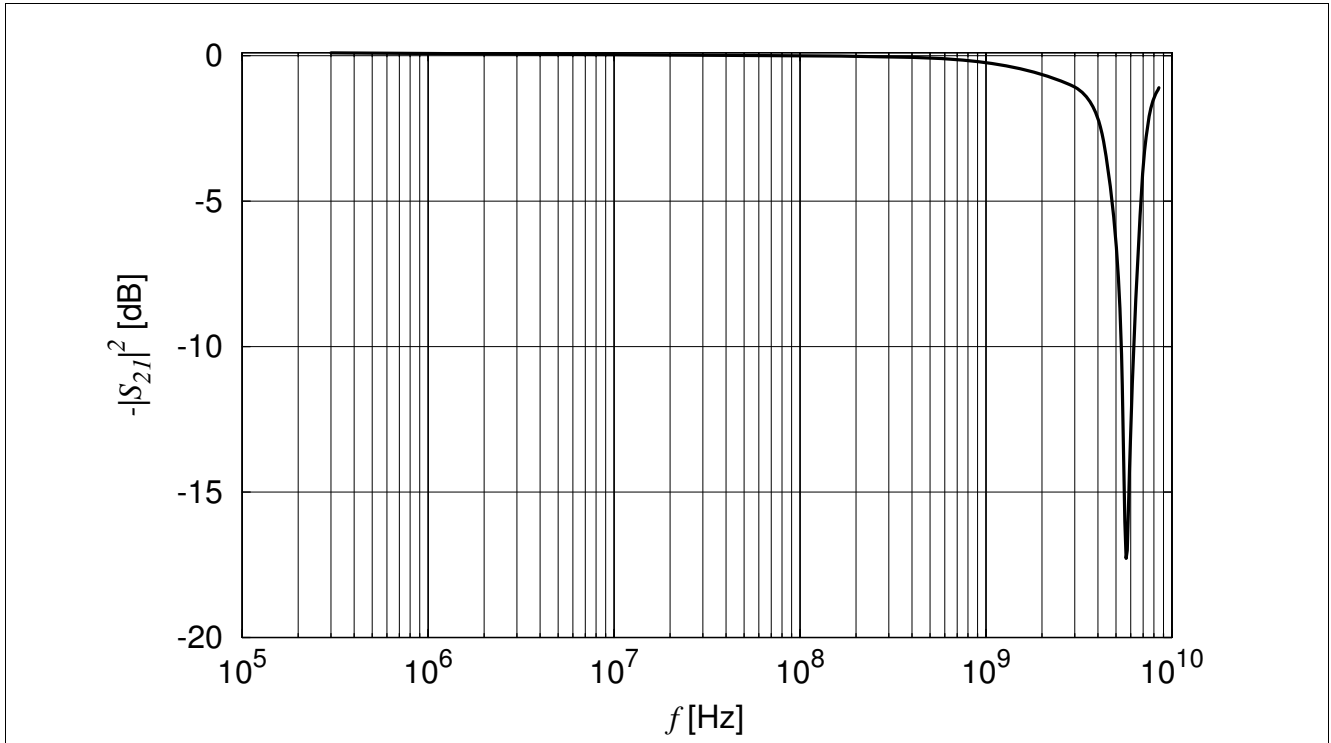


Figure 5 Insertion loss  $I_L = f(f)$ ,  $V_R = 0$  V

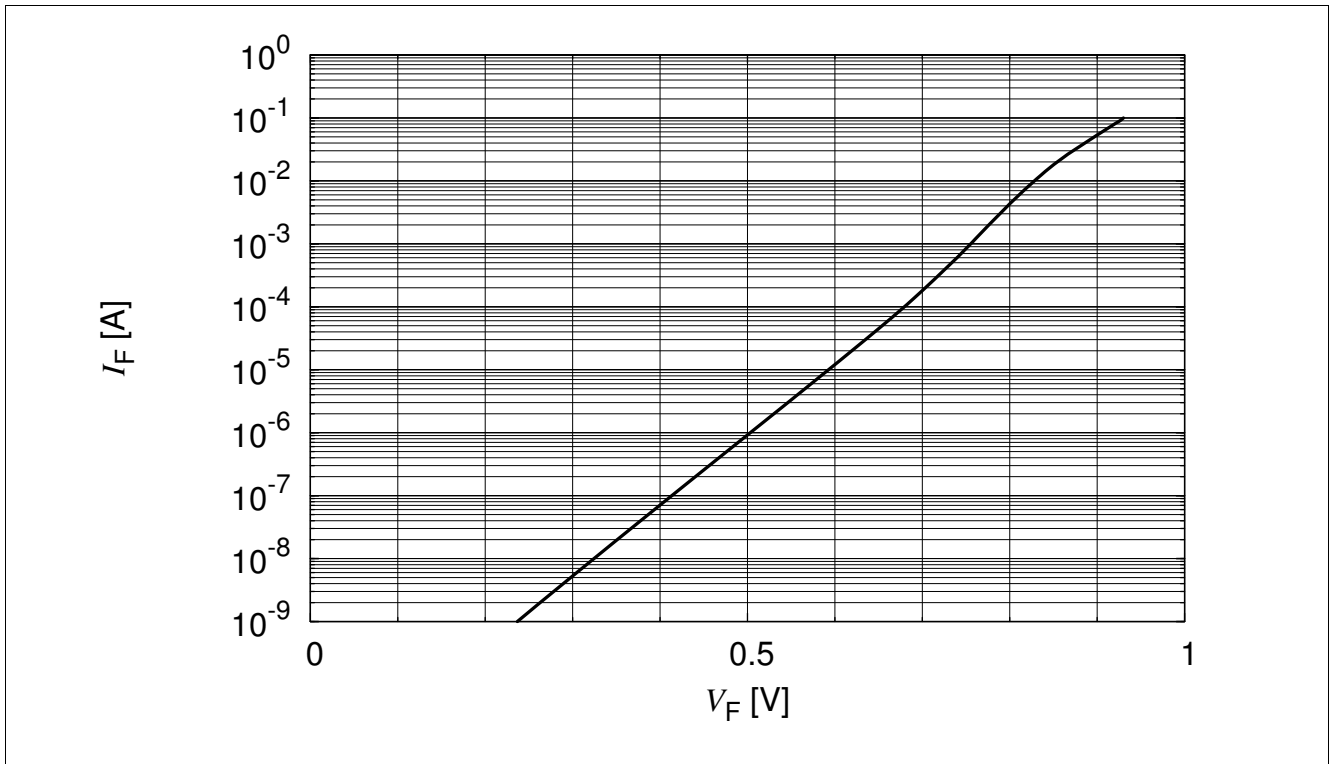


Figure 6 Forward characteristic,  $I_F = f(V_F)$ , current forced



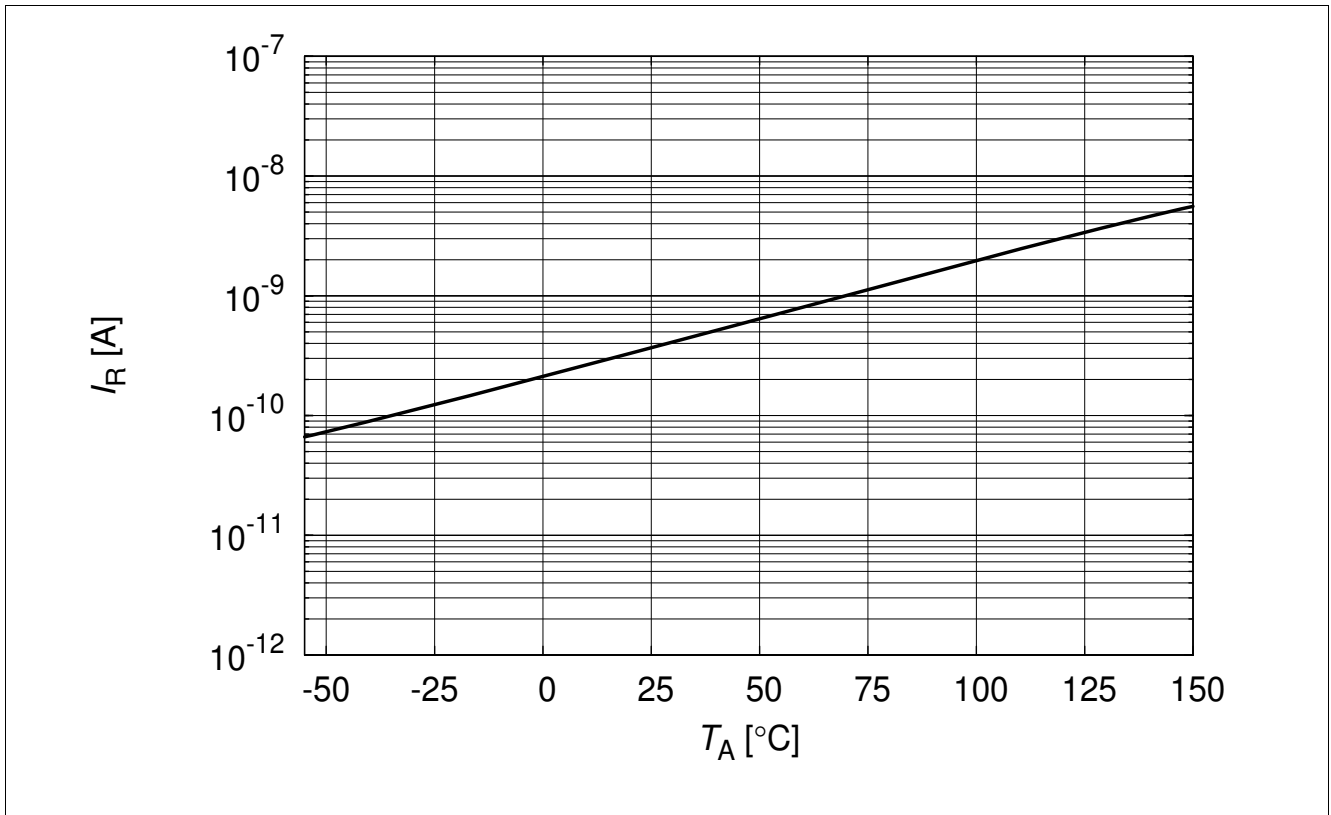


Figure 7 Reverse current  $I_R = f(T_A)$ ,  $V_R = 5.5$  V (typical)

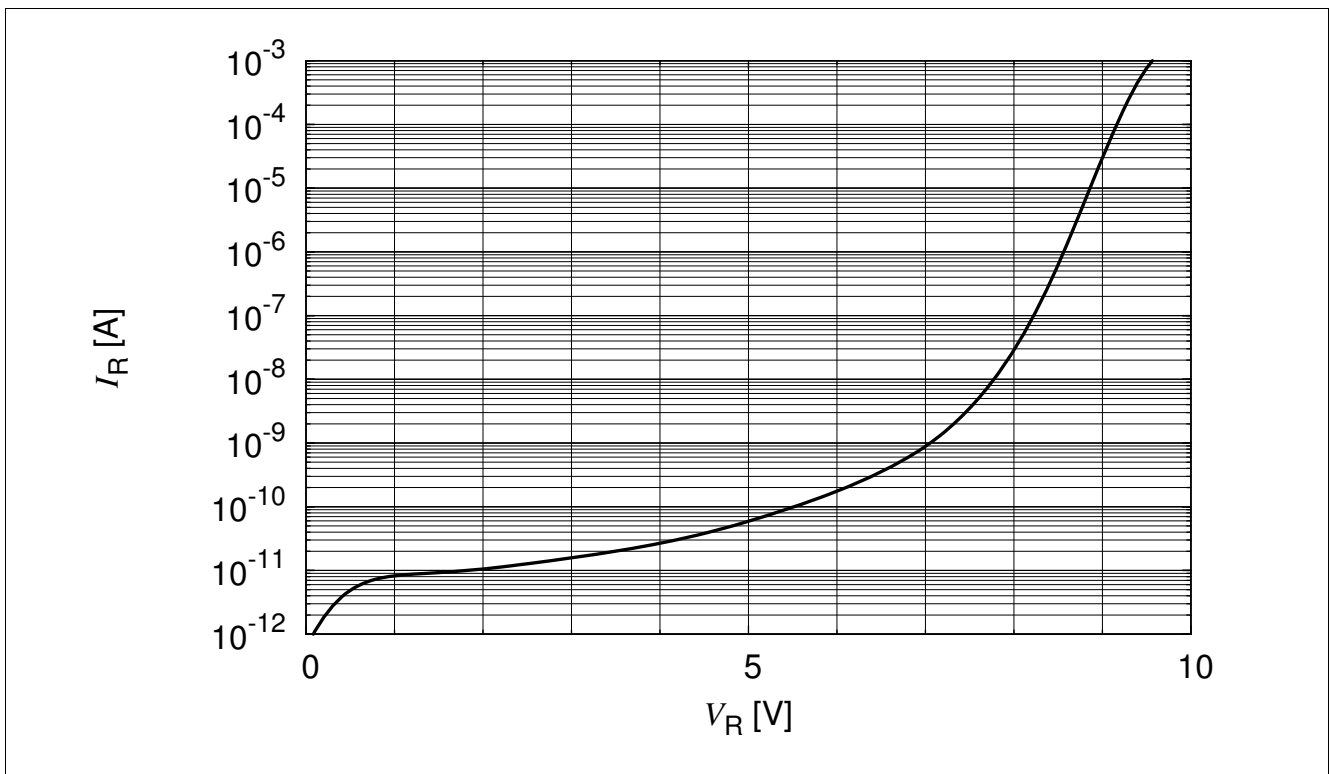


Figure 8 Reverse characteristic,  $I_R = (V_R)$ , voltage forced

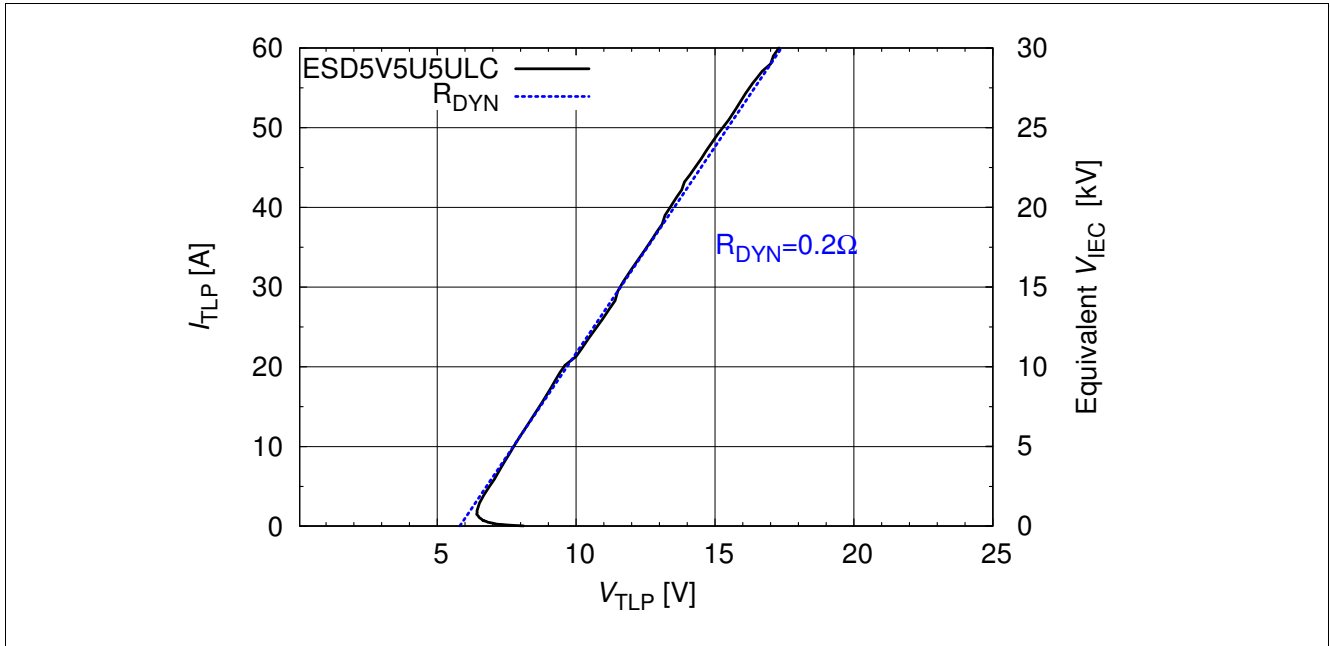


Figure 9 TLP characteristic I/O to GND <sup>Note: [2]</sup>

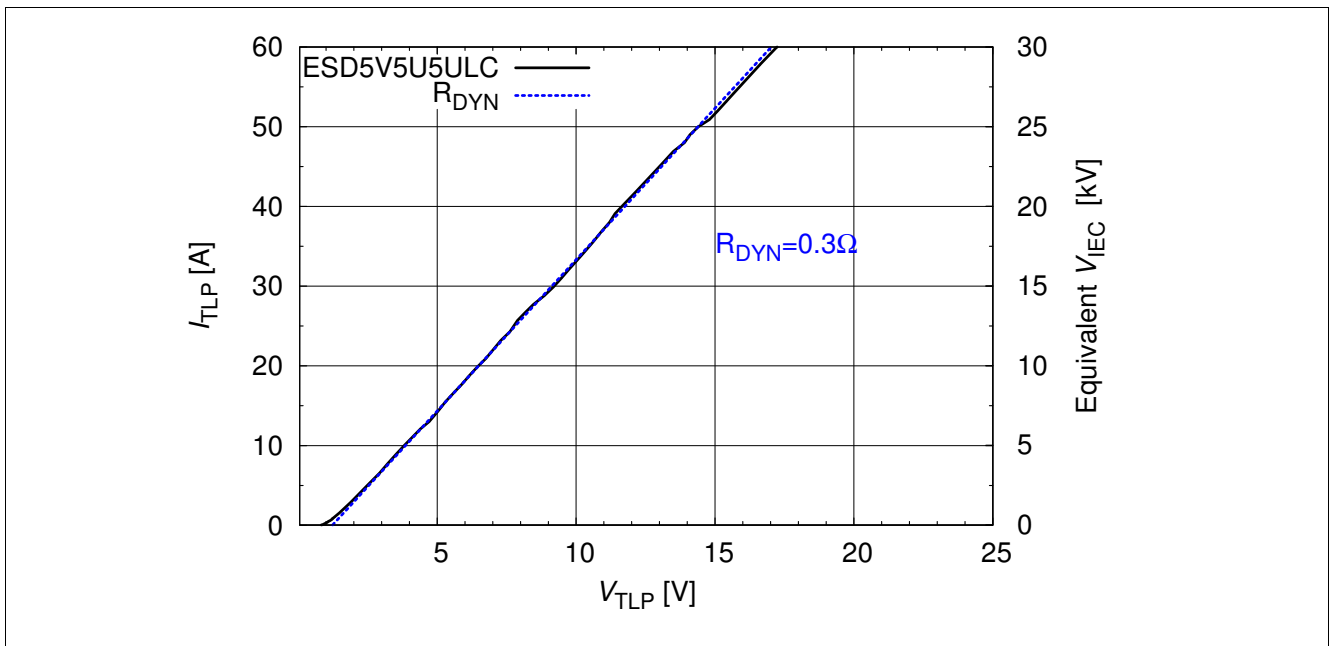


Figure 10 TLP characteristic GND to I/O <sup>Note: [2]</sup>

Note: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{PP1} = 10 \text{ A}$  and  $I_{PP2} = 40 \text{ A}$ . The equivalent stress level  $V_{IEC}$  according IEC 61000-4-2 ( $R = 330 \Omega$ ,  $C = 150 \text{ pF}$ ) is calculated at the broad peak of the IEC waveform at  $t = 30 \text{ ns}$  with  $2 \text{ A / kV}$

### 3 Application Information

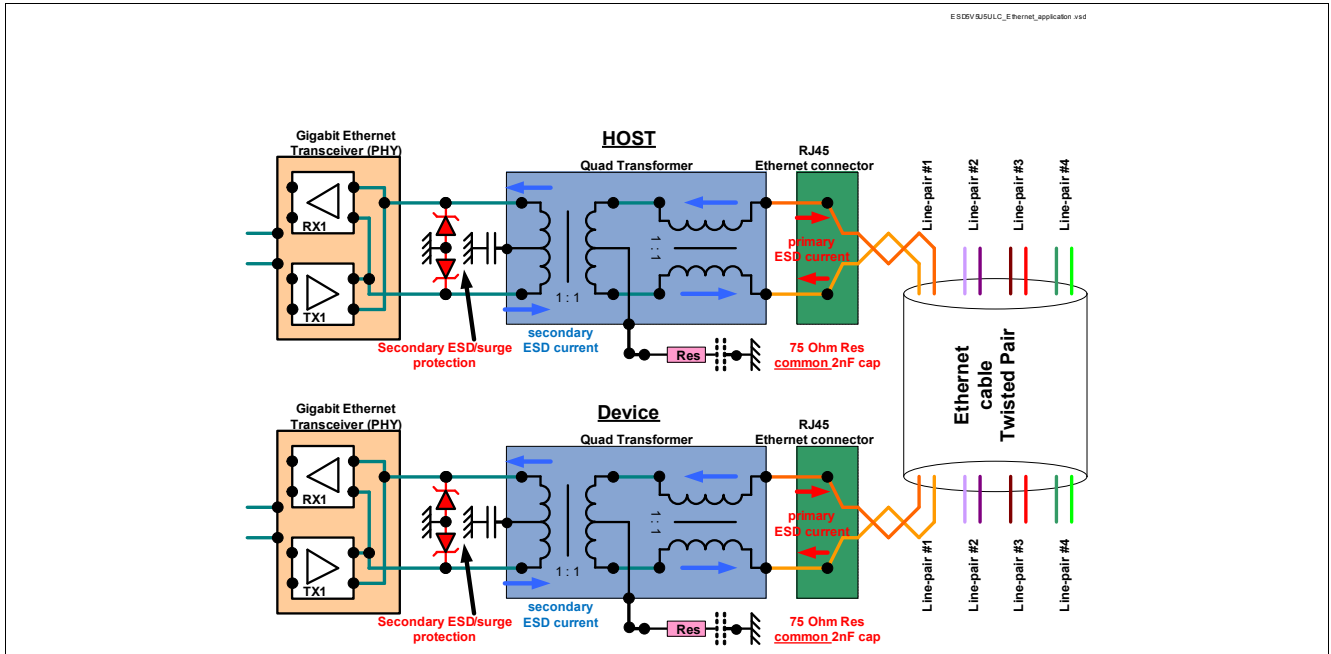


Figure 11 Ethernet

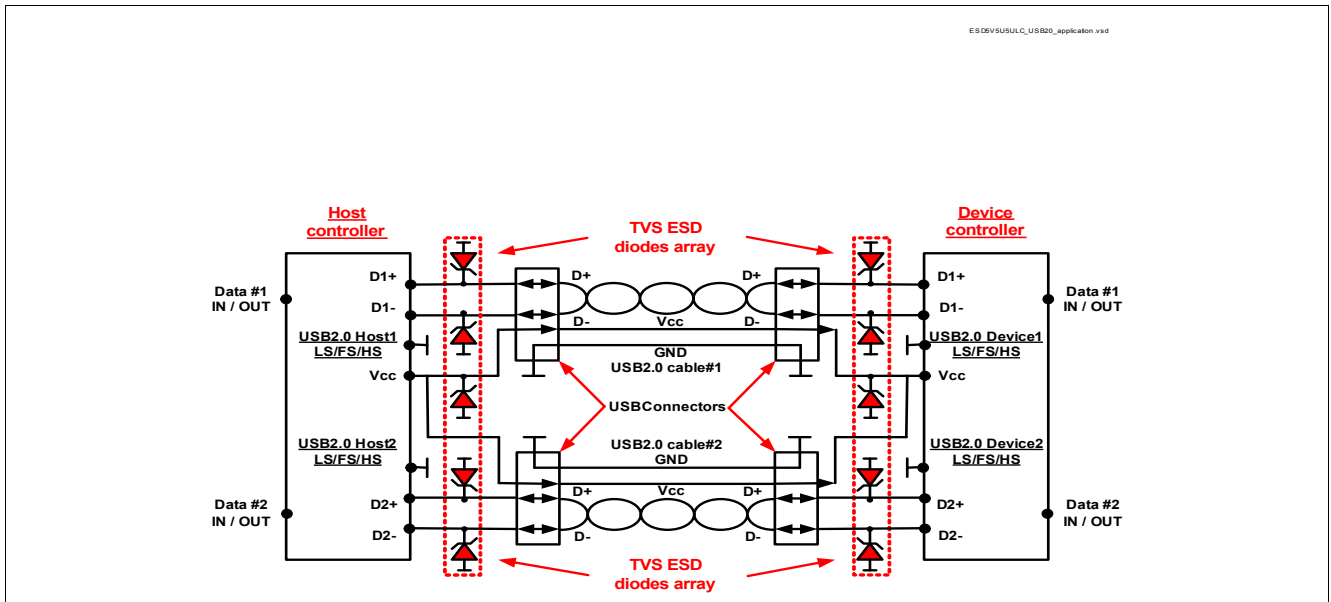


Figure 12 USB2.0

#### 4 Ordering Information Scheme (Examples)

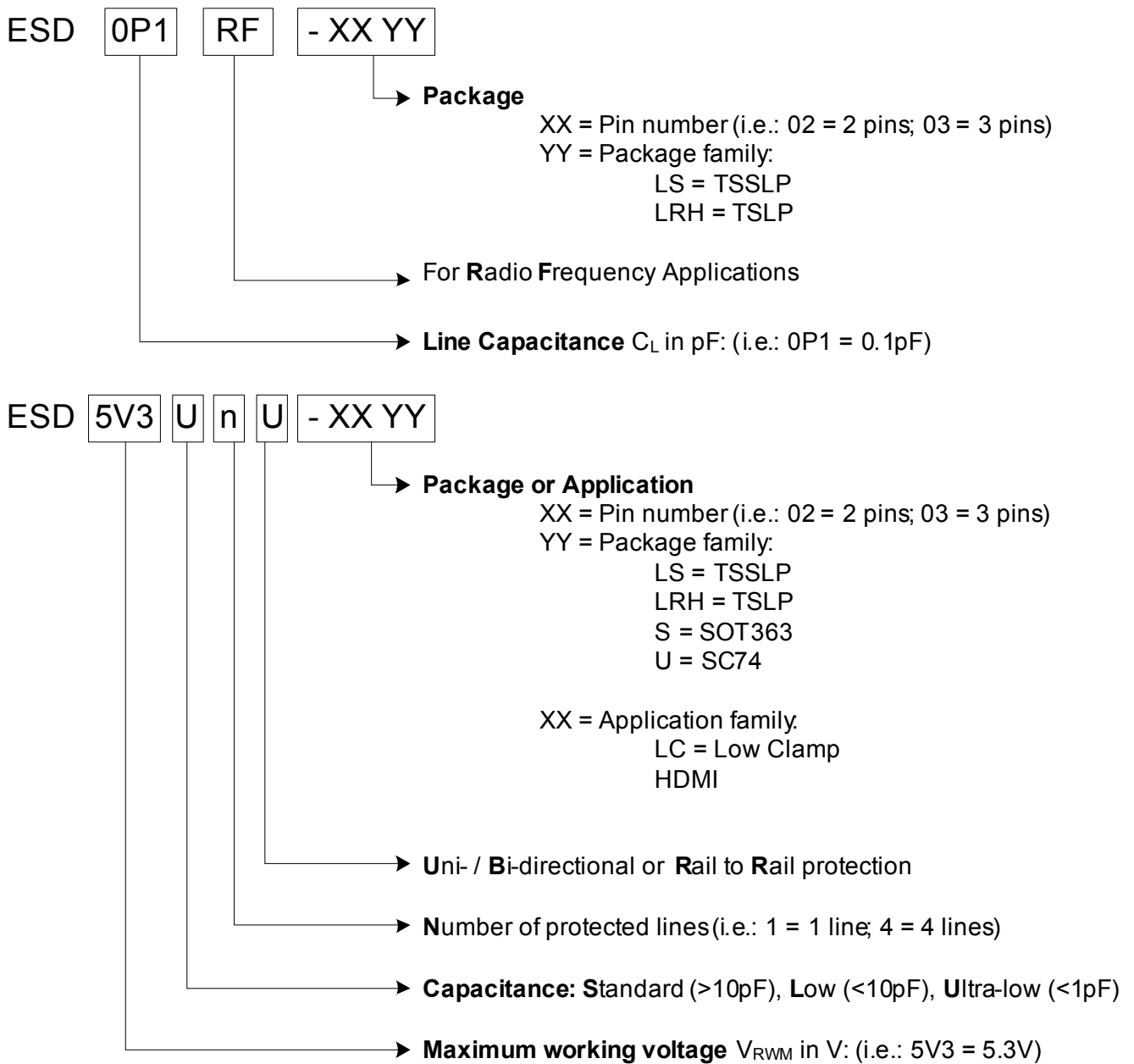


Figure 13 Ordering information scheme

## 5 Package Information

### 5.1 PG-SC74 (mm)

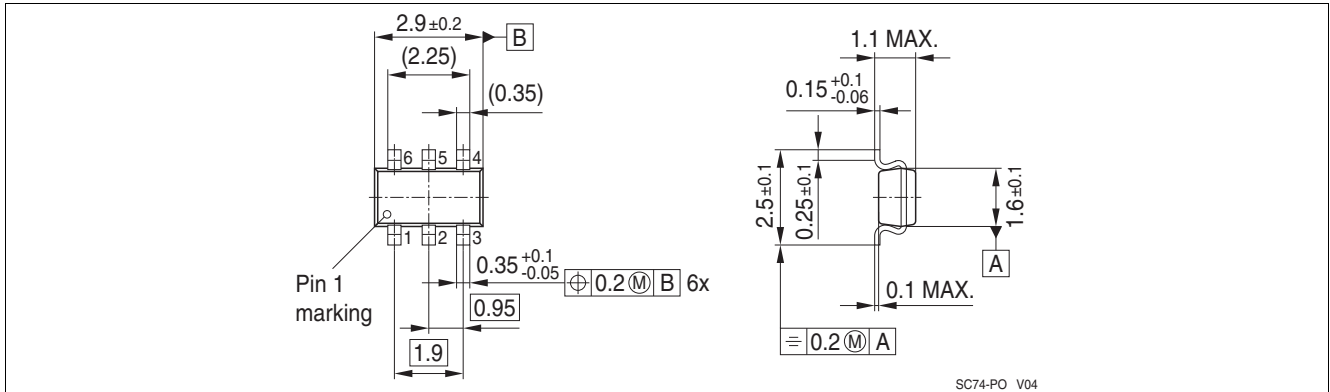


Figure 14 PG-SC74: Package overview

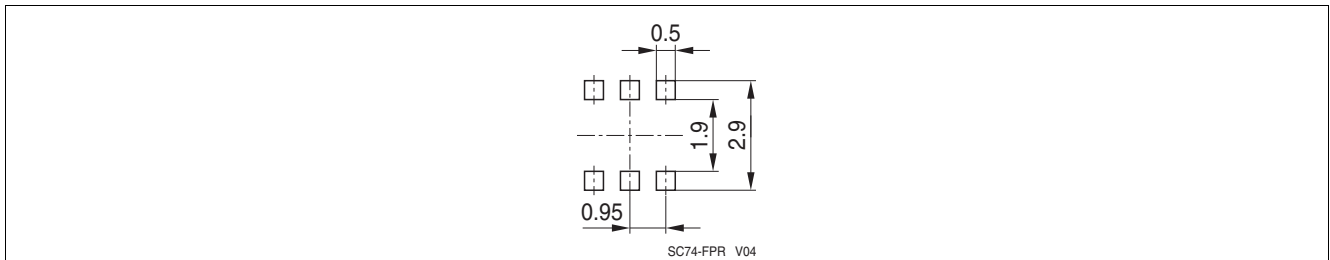


Figure 15 PG-SC74: Footprint

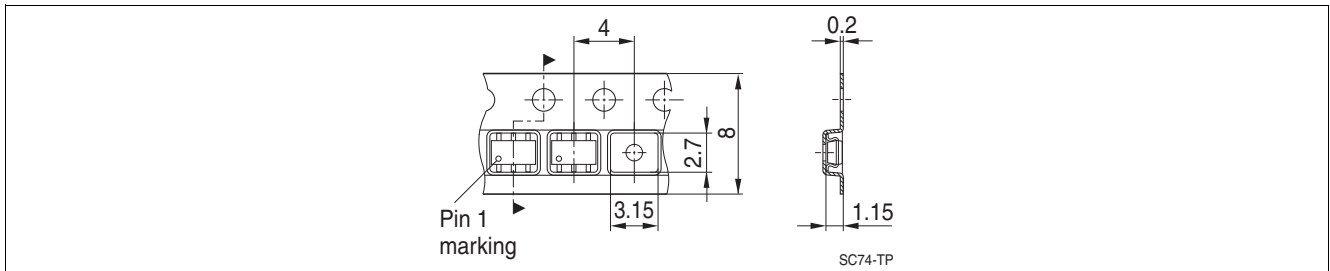


Figure 16 PG-SC74: Packing

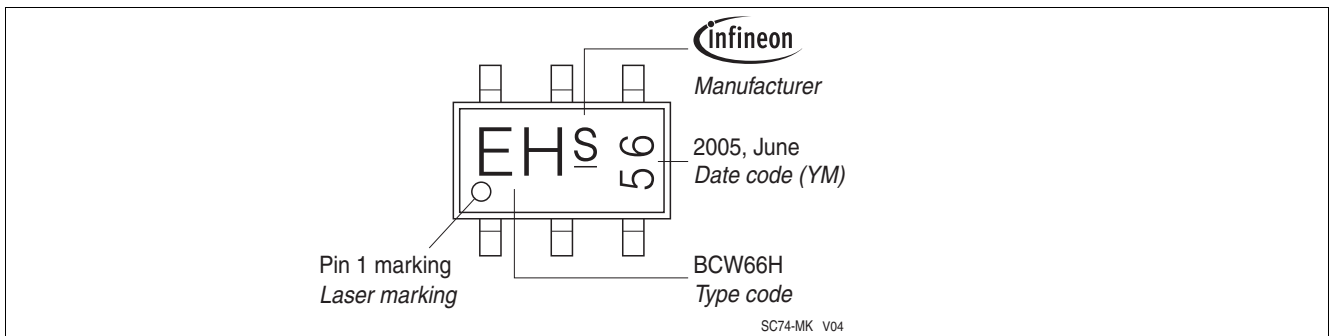


Figure 17 PG-SC74: Marking (example)

**References**

- [1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1
- [2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

**Revision History: Rev. 1.3, 2015-07-16**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.4, 2016-06-27</b>	
4	Correction of typing error

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