General Description

The MAX8969 is a simple 1A step-up converter in a small package that operates in any single-cell Li-ion application. This IC provides protection features such as input undervoltage lockout, short circuit, and overtemperature shutdown.

The IC transitions to skip mode seamlessly under light-load conditions to improve efficiency. Under these conditions, switching occurs only as needed, reducing switching frequency and supply current to maintain high efficiency.

For higher efficiency when input voltage is closer to the output voltage, two special modes of operation are available: track and automatic track. These modes allow users to balance quiescent current (I_Q) vs. transient response time into boost mode. In both modes, the p-channel MOSFET acts as a current-limited switch such that V_{OUT} follows V_{IN}. However, in track mode, the boost circuits are disabled and the system controls the boost function with the EN, TREN inputs (I_Q = 30µA). In automatic track mode (ATM), the boost circuits are enabled and the device automatically transitions into boost mode when V_{IN} falls to 95% of the target V_{OUT} (I_Q = 60µA).

The IC is available in a small, 1.25mm x 1.25mm, 9-bump WLP (0.4mm pitch) package.

Applications

- Cell Phones
- Smartphones
- Mobile Internet Devices
- GPS, PND
- eBooks

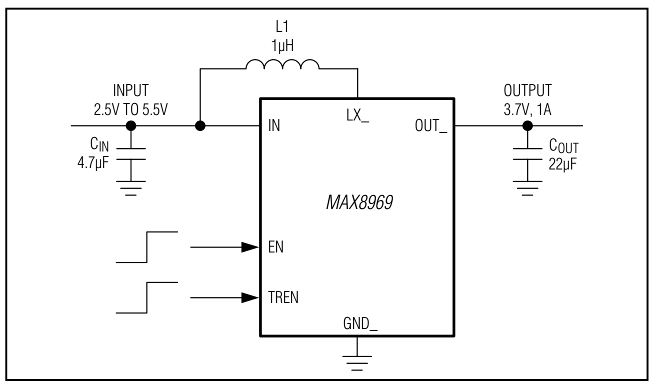
***Ordering Information* appears at end of data sheet.**

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Benefits and Features

- Flexible System Integration
  - Up to 1A Output Current
  - 2.5V to 5.5V Input Voltage Range
  - 3.3V to 5.7V Output Voltage Options
- Integrated Protection Increases System Robustness
  - Undervoltage Lockout (UVLO)
  - Short-Circuit Protection
  - Overtemperature Shutdown
- High Efficiency and Low Quiescent Current Extends Battery Life
  - Over 90% Efficiency with Internal Synchronous Rectifier
  - 60µA I_Q in Automatic Track Mode
  - 45µA I_Q in Step-Up Mode
  - 30µA I_Q in Track Mode
  - 1µA Shutdown Current
  - Skip Mode Under Light Load Condition Improves Efficiency
  - True Shutdown™ Prevents Current Flow from OUT_ to LX_
  - Soft-Start Limits Inrush Current to 480mA
- Small Package and High Frequency Operation Reduce Board Space
  - 9-Bump 1.25mm x 1.25mm WLP Package
  - 3MHz PWM Switching Frequency
  - Small External Components

Typical Operating Circuit



Absolute Maximum Ratings

IN, OUT_ to GND_ .... -0.3V to +6.0V
EN, TREN to GND_ .... -0.3V to lower of (V_{IN} + 0.3V) or 6V
Total LX_ RMS Current (Note 1) .... $3.2A_{RMS}$
OUT_ Short Circuit to GND_ .... Continuous
Continuous Power Dissipation (T_A = +70°C)
  WLP (derate 12mW/NC above +70°C) 960mW

Operating Temperature Range .... -40ºC to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow) (Note 2) .... +260°C

Note 1: LX_ has internal silicon diodes to GND_ and OUT_. It is normal for these diodes to briefly conduct during LX_ transitions. Avoid steady state conduction of these diodes.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile that the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 3)

WLP
  Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 83°C/W
  Junction-to-Case Thermal Resistance (θ_{JC}) .... 50°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 2.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage Range			2.5		5.5	V
Minimum Startup Voltage				2.3		V
Undervoltage Lockout Threshold (UVLO)	V_{IN} falling, 75mV hysteresis		2.1	2.2	2.3	V
Shutdown Supply Current	V_{EN} = V_{TREN} = V_{OUT} = 0V, V_{IN} = 4.8V	T_A = +25°C		0.8	5	µA
		T_A = +85°C		1		
Thermal Shutdown Temperature	T_J rising, 20°C hysteresis			+165		°C
BOOST MODE						
Peak Output Current	V_{IN} > 2.5V, pulse loading (Note 5)			1		A
Minimum Continuous Output Current	V_{IN} > 2.5V (Note 5)	V_{OUT} = 3.3V		0.9		A
		V_{OUT} = 3.5V		0.8		
		V_{OUT} = 3.7V		0.7		
		V_{OUT} = 4.25V		0.7		
		V_{OUT} = 5.0V		0.7		
		V_{OUT} = 5.5V		0.7		
		V_{OUT} = 5.7V		0.6		
Switching Frequency	(Note 6)			3		MHz

Electrical Characteristics (continued)

(V_{IN} = 2.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Accuracy	No load, V_{OUT_TARGET} = 3.3V		3.175	3.30	3.40	V
	No load, V_{OUT_TARGET} = 3.5V		3.40	3.50	3.60	
	No load, V_{OUT_TARGET} = 3.7V		3.64	3.75	3.85	
	No load, V_{OUT_TARGET} = 4.25V		4.10	4.25	4.35	
	No load, V_{OUT_TARGET} = 5V		4.85	5.00	5.10	
	No load, V_{OUT_TARGET} = 5.5V		5.39	5.5	5.65	
	No load, V_{OUT_TARGET} = 5.7V		5.53	5.7	5.81	
Steady-State Output Voltage	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 1A, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 3.3V		3.00		3.45	V
	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 1A, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 3.5V		3.15		3.65	
	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 1A, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 3.7V		3.35		3.85	
	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 600mA, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 4.25V		3.95		4.35	
	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 500mA, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 5V		4.50		5.10	
	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 400mA, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 5.5V		5.00		5.65	
	2.5V < V_{IN} < V_{ATMRT}, conditions emulating 0 < I_{OUT} < 400mA, C_{OUT} = 22µF, L = 1µH, V_{OUT_TARGET} = 5.7V		5.13		5.81	
LX_ Leakage Current	V_{LX} = 0V, 4.8V	T_A = +25°C		0.1	5	µA
		T_A = +85°C		0.2		
Skip-Mode Supply Current	EN = high, I_{OUT} = 0A, 1µH inductor (TREN is low, not switching)			45		µA
pMOS Turn-Off Current (Zero-Cross Current)				10		mA
LX_ nMOS Current Limit			2.1	2.6	3.2	A
Maximum Duty Cycle				83		%
Minimum Duty Cycle			0			%

Electrical Characteristics (continued)

(V_{IN} = 2.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
pMOS On-Resistance	V_{OUT} = 3.3V		120		mΩ
	V_{OUT} = 3.5V		115		
	V_{OUT} = 3.7V		110		
	V_{OUT} = 4.25V		100		
	V_{OUT} = 5V		91		
	V_{OUT} = 5.5V		79		
	V_{OUT} = 5.7V		77		
nMOS On-Resistance	V_{OUT} = 3.3V		65		mΩ
	V_{OUT} = 3.5V		63		
	V_{OUT} = 3.7V		60		
	V_{OUT} = 4.25V		55		
	V_{OUT} = 5V		51		
	V_{OUT} = 5.5V		43		
	V_{OUT} = 5.7V		42		
Minimum Output Capacitance for Stable Operation (Actual)			8		µF
Minimum P1 Soft-Start Current Limit	V_{OUT} = 5V		0.48		A
Output Voltage Ripple	I_{OUT} = 150mA, circuit of Figure 1		20		mV_{P-P}
TRACK MODE					
pMOSFET On-Resistance	I_{OUT} = 500mA, V_{IN} = 2.7V		130		mΩ
	I_{OUT} = 500mA, V_{IN} = 3.2V		110		
Track Current Limit	V_{OUT} = 3.6V	1	2		A
Track Mode Quiescent Current	EN = low, TREN = high		30		µA
AUTOMATIC TRACK MODE (ATM)					
ATM Supply Current	V_{IN} = 5.4V		65		µA
ATM V_{IN} Rising Threshold (V_{ATMRT})	V_{OUT_TARGET} = 3.3V		3.15		V
	V_{OUT_TARGET} = 3.5V		3.35		
	V_{OUT_TARGET} = 3.7V		3.55		
	V_{OUT_TARGET} = 4.25V		4.04		
	V_{OUT_TARGET} = 5V		4.74		
	V_{OUT_TARGET} = 5.5V		5.28		
	V_{OUT_TARGET} = 5.7V		5.44		

Electrical Characteristics (continued)

(V_{IN} = 2.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ATM V_{IN} Falling Threshold (V_{ATMFT})	V_{OUT_TARGET} = 3.3V		3.10		V
	V_{OUT_TARGET} = 3.5V		3.29		
	V_{OUT_TARGET} = 3.7V		3.5		
	V_{OUT_TARGET} = 4.25V		3.99		
	V_{OUT_TARGET} = 5V		4.69		
	V_{OUT_TARGET} = 5.5V		5.23		
	V_{OUT_TARGET} = 5.7V		5.39		
Boost to ATM Transition Time (t_{ATM_ENTER})	(Note 6)		1		µs
ATM to Boost Transition Time (t_{ATM_EXIT})			1		µs
LOGIC CONTROL					
EN, TREN Logic Input High Voltage	2.3V < V_{IN} < 5.5V	1.05			V
EN, TREN Logic Input Low Voltage	2.3V < V_{IN} < 5.5V			0.4	V
EN, TREN Leakage Current	V_{EN} = V_{TREN} = 0V, T_A = +25°C	-1	0.01	+1	µA
	V_{EN} = V_{TREN} = 0V, T_A = +85°C		0.1		

Note 4: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

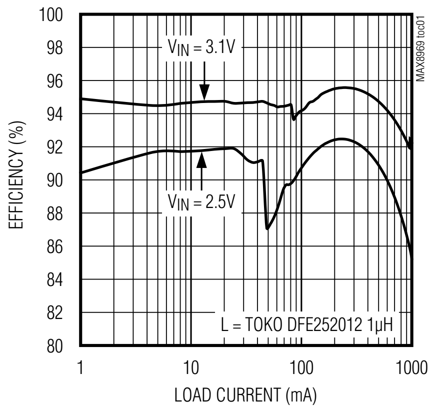
Note 5: The device supports a peak output current of 1A. Continuous operation with 1A output current at elevated temperature is not guaranteed. With sustained high current (> 100ms, > 1A), the junction temperature (T_J) rises to the thermal shutdown threshold. The stated Minimum Continuous Output Current values represent what the typical operating circuit can achieve when considering device and component variations. See the *Output Current* section for more information.

Note 6: Switching frequency decreases if input voltage is > 83% of the output voltage selected. This allows duty factor to drop to values necessary to boost output voltage less than 25% without the use of pulse widths less than 60ns.

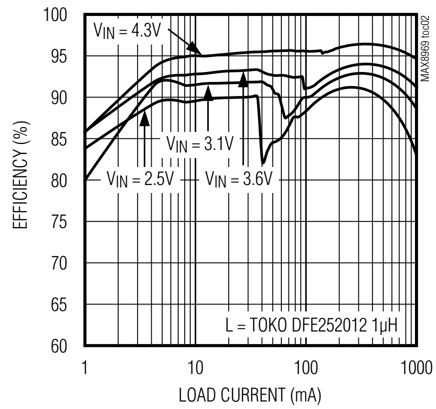
Typical Operating Characteristics

(V_{IN} = 3.6V, C_{OUT} = 22µF, X5R, 6.3V local and 10µF, X5R, 6.3V, 1µH inductor, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

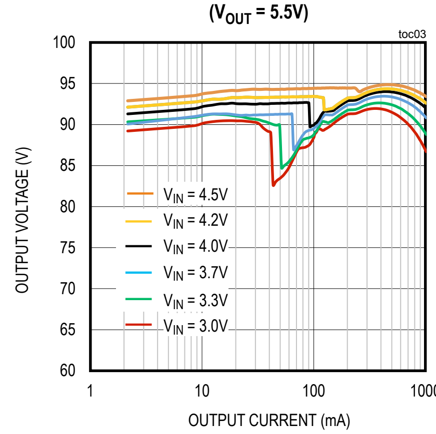
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.7V)



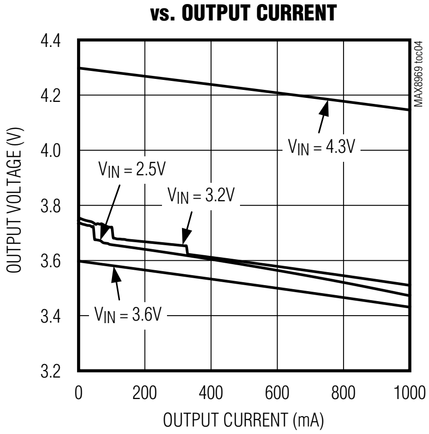
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5V)



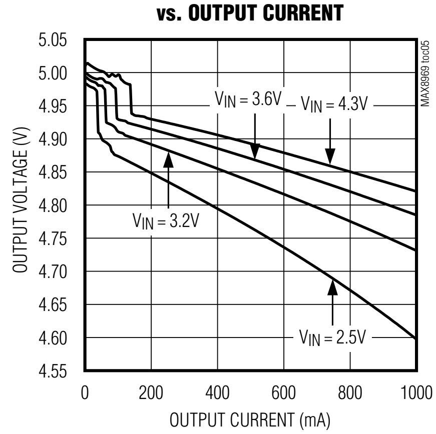
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5.5V)



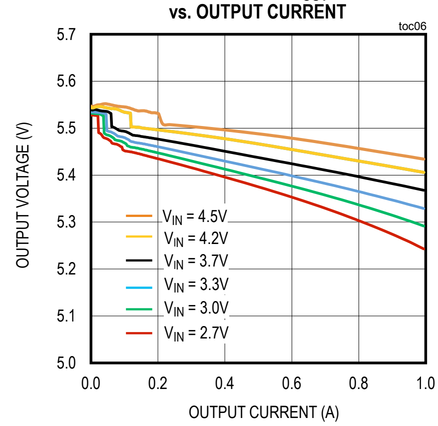
OUTPUT VOLTAGE (V_{OUT} = 3.7V) vs. OUTPUT CURRENT



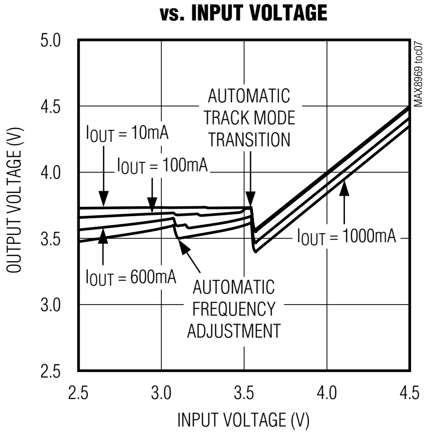
OUTPUT VOLTAGE (V_{OUT} = 5V) vs. OUTPUT CURRENT



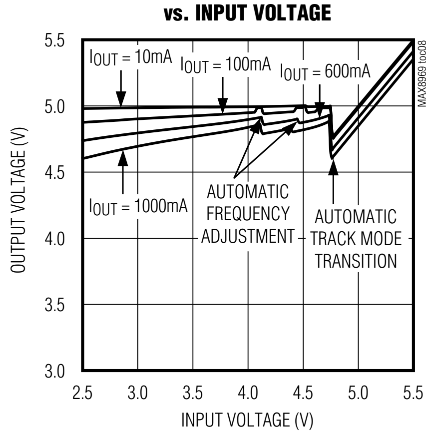
OUTPUT VOLTAGE (V_{OUT} = 5.5V) vs. OUTPUT CURRENT



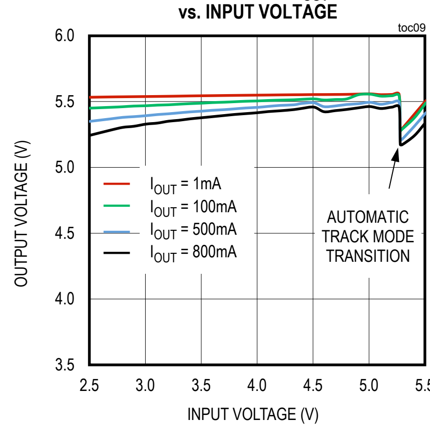
OUTPUT VOLTAGE (V_{OUT} = 3.7V) vs. INPUT VOLTAGE



OUTPUT VOLTAGE (V_{OUT} = 5V) vs. INPUT VOLTAGE



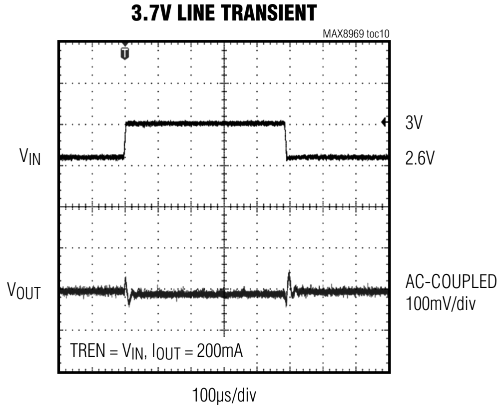
OUTPUT VOLTAGE (V_{OUT} = 5.5V) vs. INPUT VOLTAGE



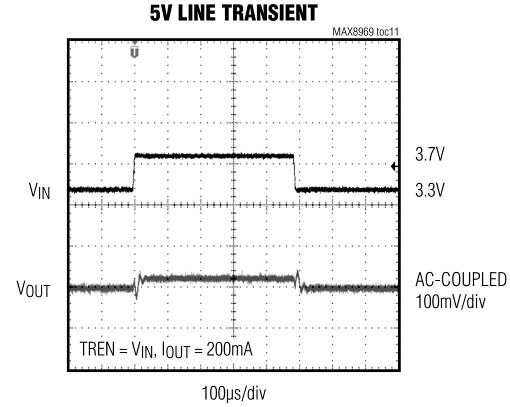
Typical Operating Characteristics (continued)

(V_{IN} = 3.6V, C_{OUT} = 22µF, X5R, 6.3V local and 10µF, X5R, 6.3V, 1µH inductor, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

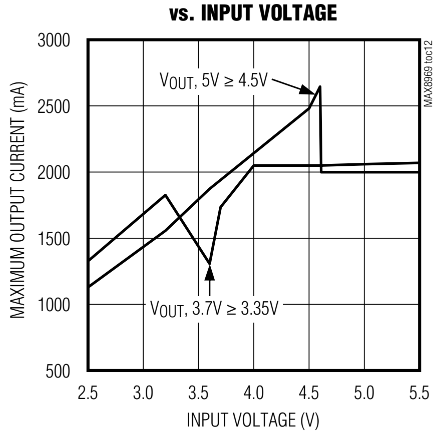
3.7V LINE TRANSIENT



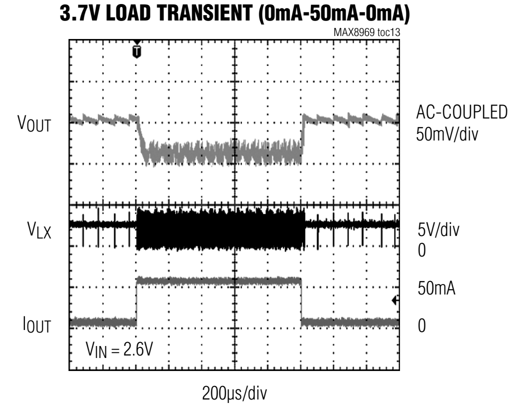
5V LINE TRANSIENT



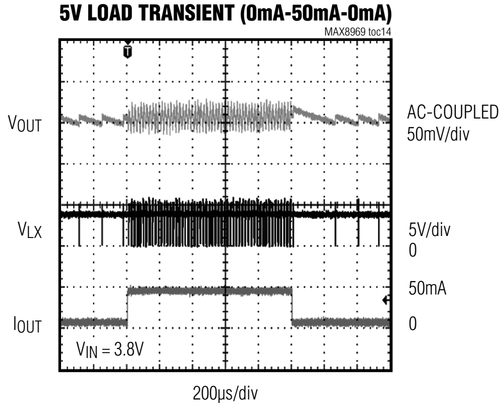
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



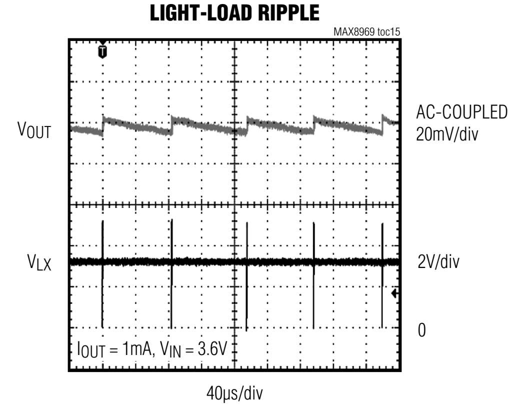
3.7V LOAD TRANSIENT (0mA-50mA-0mA)



5V LOAD TRANSIENT (0mA-50mA-0mA)



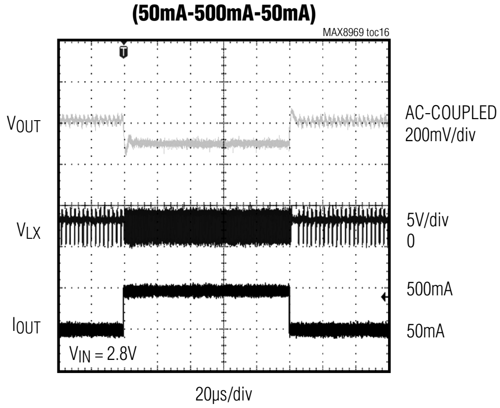
LIGHT-LOAD RIPPLE



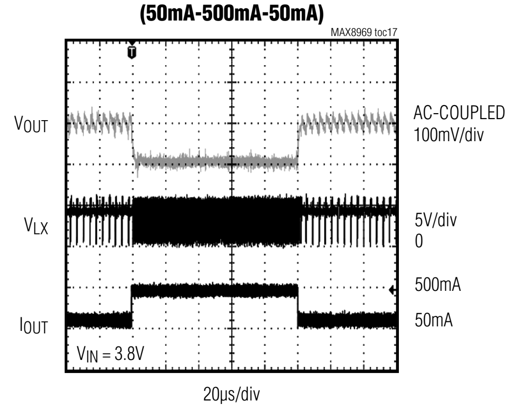
Typical Operating Characteristics (continued)

(V_{IN} = 3.6V, C_{OUT} = 22µF, X5R, 6.3V local and 10µF, X5R, 6.3V, 1µH inductor, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

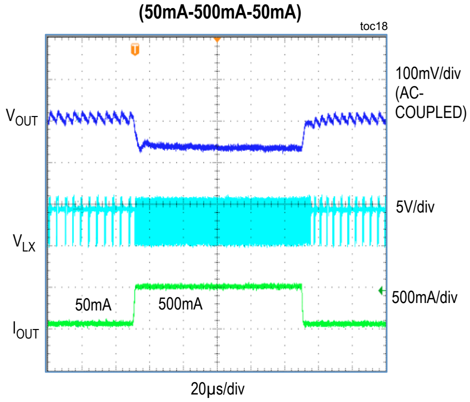
3.7V LOAD TRANSIENT (50mA-500mA-50mA)



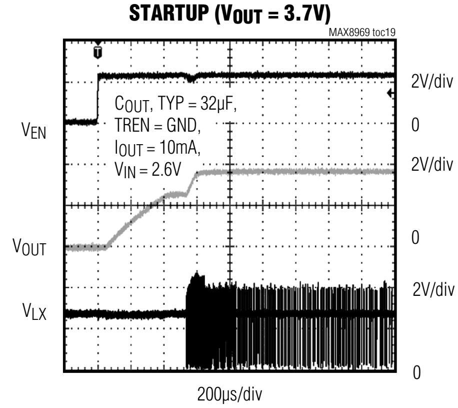
5V LOAD TRANSIENT (50mA-500mA-50mA)



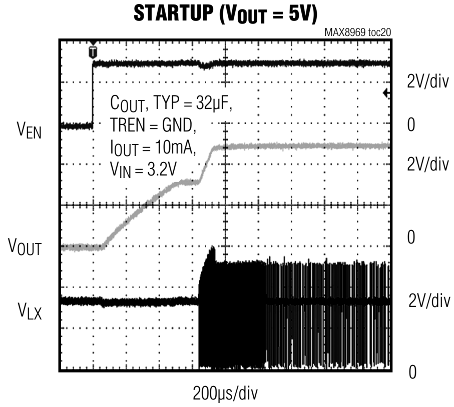
5.5V LOAD TRANSIENT (50mA-500mA-50mA)



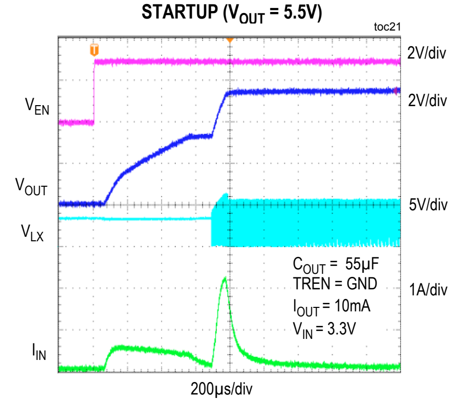
STARTUP (V_{OUT} = 3.7V)



STARTUP (V_{OUT} = 5V)

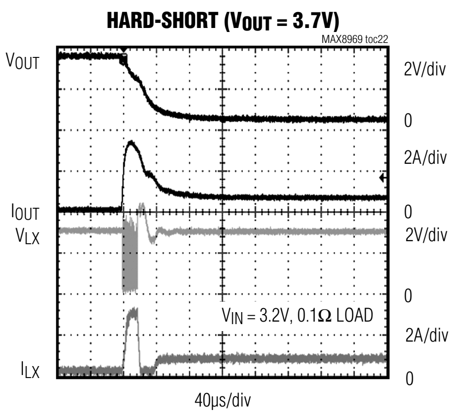


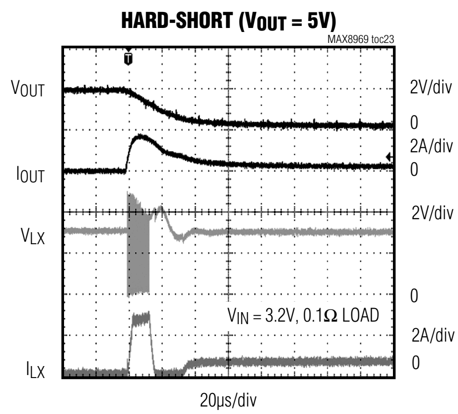
STARTUP (V_{OUT} = 5.5V)

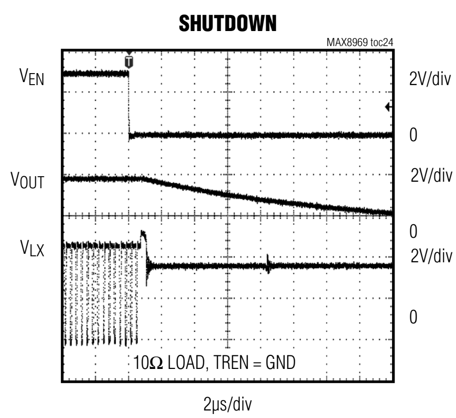


Typical Operating Characteristics (continued)

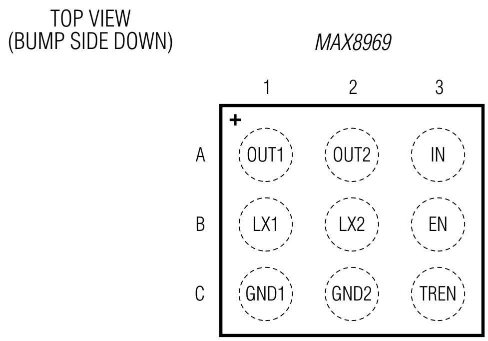
(V_{IN} = 3.6V, C_{OUT} = 22µF, X5R, 6.3V local and 10µF, X5R, 6.3V, 1µH inductor, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)







Pin Configuration



WLP
(1.25mm × 1.25mm)

Pin Description

PIN	NAME	FUNCTION
A1	OUT1	Power Output. Bypass OUT_ to ground with a 22µF rated ceramic capacitor. For optimal performance place the ceramic capacitor as close as possible to OUT_. OUT1 and OUT2 should be shorted together directly under the IC. In True Shutdown, the output voltage can fall to 0V, but OUT_ has a diode with its cathode connected to IN. See Figure 3. Connect OUT1 and OUT2 together directly under the IC.
A2	OUT2	
A3	IN	Input Supply Voltage. Bypass IN to GND_ with a 4.7µF ceramic capacitor. A larger capacitance may be required to reduce noise.
B1	LX1	Converter Switching Node. Connect a 1µH inductor from LX_ to IN. LX_ is high impedance in shutdown. Connect LX1 and LX2 together directly under the IC. Connect LX1 and LX2 together directly under the IC.
B2	LX2	
B3	EN	Enable Input. Drive EN logic-high to enable boost mode, regardless of the logic level of TREN. Connect EN to ground or drive logic-low to allow TREN to select either True Shutdown or track mode. See Table 1.
C1	GND1	Ground. Connect GND_ to a large ground plane. Connect GND1 and GND2 together directly under the IC.
C2	GND2	
C3	TREN	Track Enable Input. Drive TREN logic-high to enable track mode. Connect TREN to ground or drive logic-low to place the IC in True Shutdown. See Table 1.

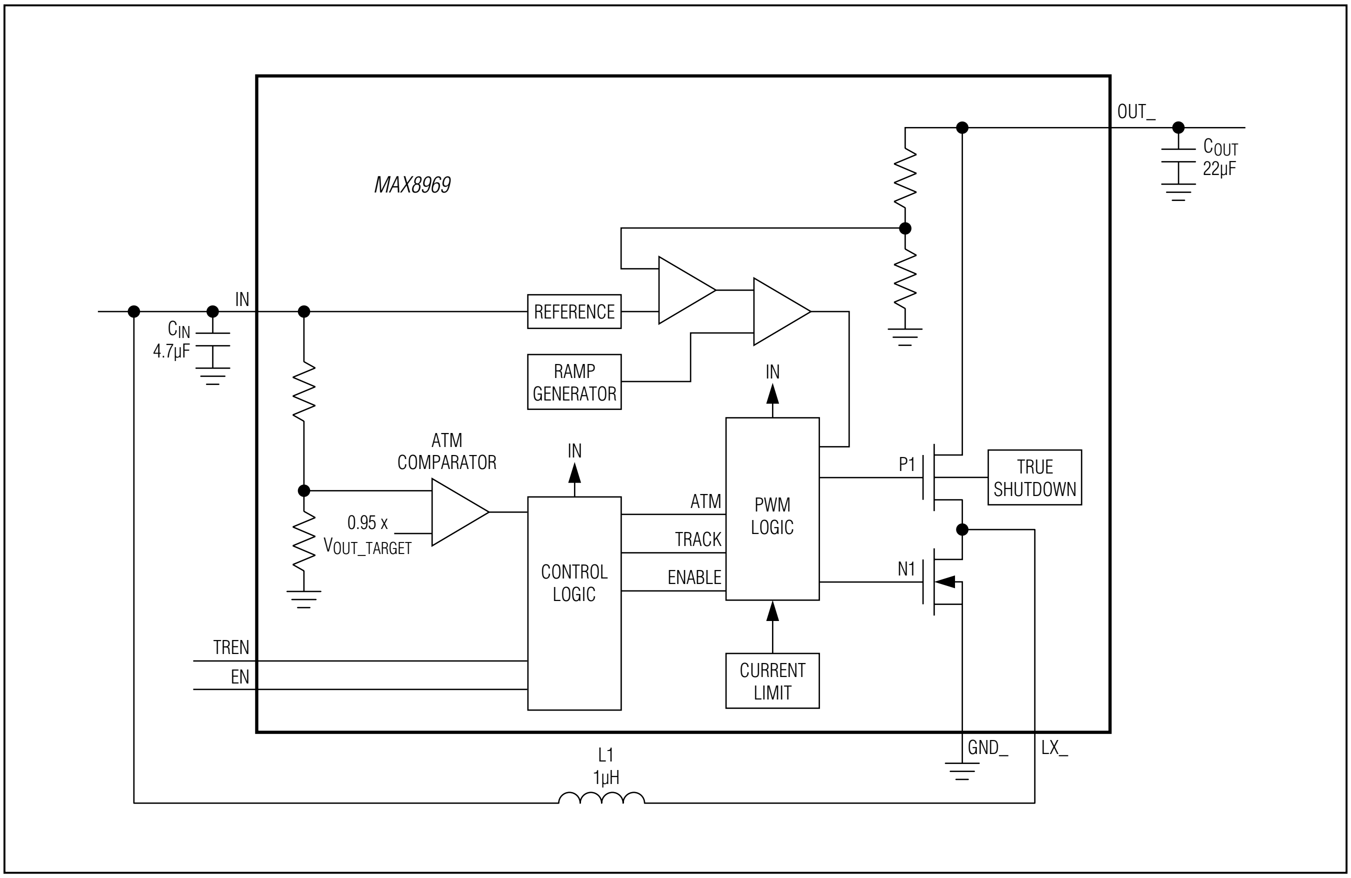


Figure 1. Functional Diagram

Detailed Description

The MAX8969 is a step-up DC-DC switching converter that utilizes a fixed-frequency PWM architecture with True Shutdown. With an advanced voltage-positioning control scheme and high 3MHz switching frequency, the IC is inexpensive to implement and compact, using only a few small easily obtained external components. Under light-load conditions, the IC switches only when needed, consuming only 45µA (typ) of quiescent current. The IC is highly efficient with an internal switch and synchronous rectifier. Shutdown typically reduces the quiescent current to 1µA (typ). Low quiescent current and high efficiency make this device ideal for powering portable equipment.

Internal soft-start limits inrush current to less than 480mA (typ), while output voltage is less than input voltage. Once output voltage approaches input voltage approaches input voltage after a brief delay, output voltage is boosted to its final value at a rate of approximately 25mV/µs. During this period, as well as being limited by the voltage, ramp rate current is limited by the normal 2.6A boost mode current limit.

In boost mode, the step-up converter boosts to V_{OUT_TARGET} from battery input voltages ranging from 2.5V to V_{OUT_TARGET}. When the input voltage ranges from 0.95 x V_{OUT_TARGET} to 5.5V, the IC enters ATM and the output voltage approximately follows the input voltage. During boost mode, the input current limit is set to 2.6A to guarantee delivery of the rated out current (e.g., 1A output current when boosting from a 2.5V input supply to a 3.7V output).

Control Scheme

The step-up converter uses a load/line control scheme. The load/line control scheme allows the output voltage to sag under load, but prevents overshoot when the load is suddenly removed. The load/line control scheme reduces the total range of voltages reached during transients at the expense of DC output impedance.

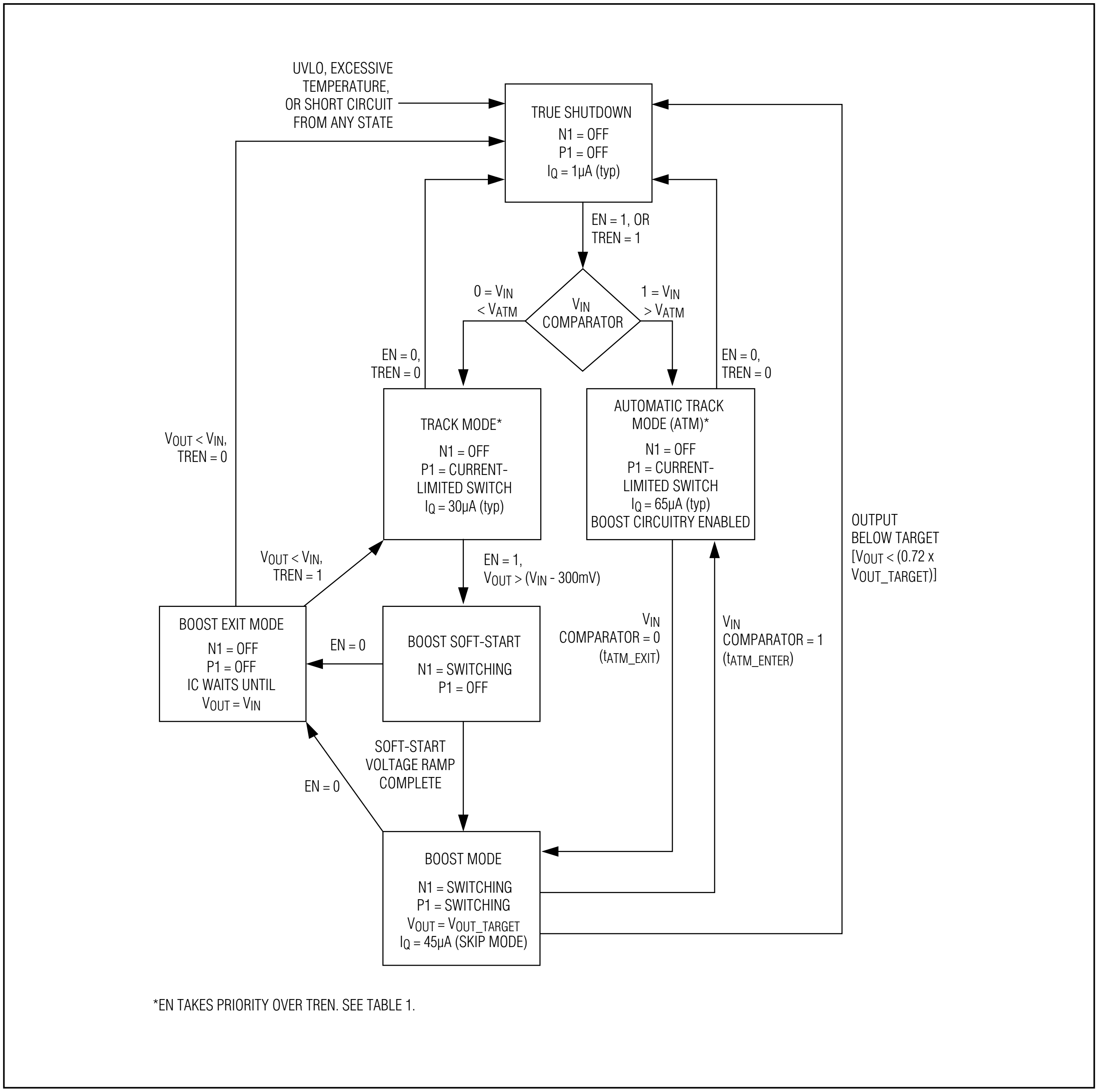


Figure 2. State Diagram

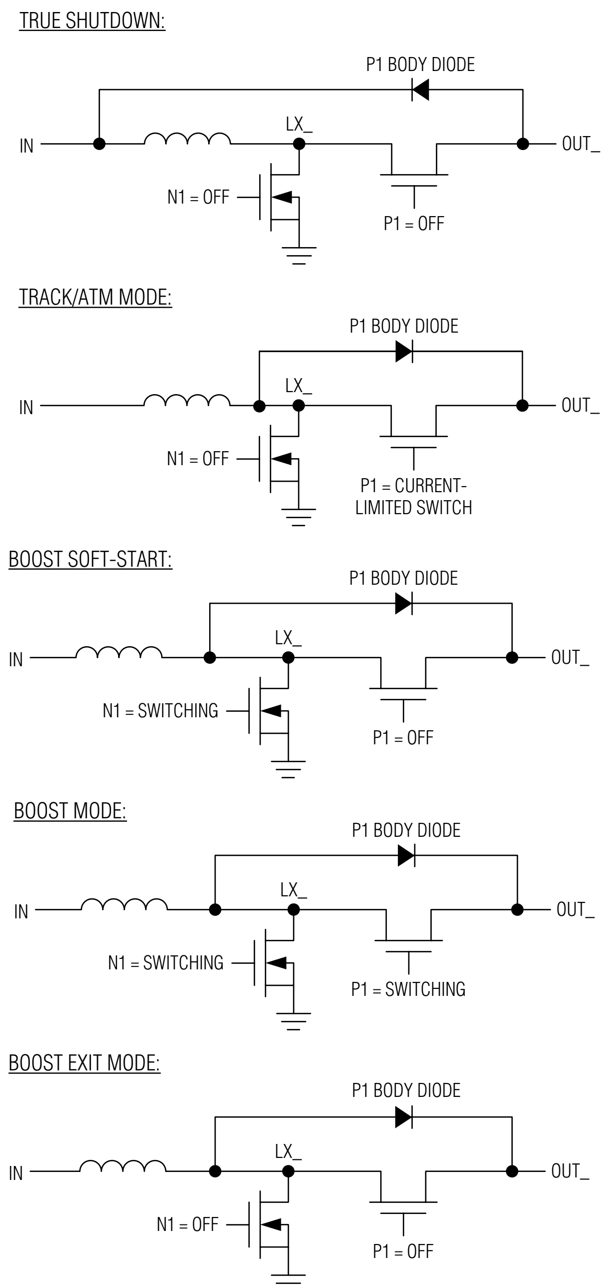


Figure 3. Modes of Operation

The IC is designed to operate with the input voltage range straddling its output voltage set point. Two techniques are used to accomplish this. The first technique is to activate ATM if the input voltage exceeds 95% of the output set point; see the Automatic Track Mode (ATM) section. The second technique is automatic frequency adjustment.

Automatic Track Mode (ATM)

ATM is entered when an internal comparator signals that the input voltage has exceeded the ATM threshold. The ATM threshold is 95% of the output voltage target. At this point, the IC enters ATM, with the pMOS switch turned on, regardless of the status of TREN. Note that EN must be high to enable ATM mode. This behavior is summarized in Table 1.

Automatic Frequency Adjustment

Automatic frequency adjustment is used to maintain stability if the input voltage is above 80% and below 95% of the output set point. Frequency adjustment is required because the n-channel has a minimum on-time of approximately 60ns. At 3MHz, this would lead to the p-channel having a maximum duty factor of 82%. With an input voltage more than 82% of the output set point, the p-channel's duty factor must be increased by reducing operating frequency either through cycle skipping or adjusting the clock's frequency. The IC adjusts its clock frequency rather than simply skipping cycles. This adjustment is done in two steps. The first step occurs if the input voltage exceeds approximately 83% of the output voltage and reduces clock speed to approximately 1.6MHz. The second step occurs if the input voltage is greater than output voltage less 460mV. If this condition is met, clock frequency is reduced to approximately 1MHz. Frequency adjustment allows the converter to operate at a known frequency under all conditions.

Fault Protection

In track, ATM, and boost modes, the IC has protection against overload and overheating.

- In track and ATM, current is limited to prevent excessive inrush current during soft-start and to protect against overload conditions. If the die temperature exceeds +165°C in track/ATM, the switch turns off until the die temperature has cooled to +145°C.
- In boost mode, during each 3MHz switching cycle, if the inductor current exceeds 2.6A, the n-channel MOSFET is shut off and the p-channel MOSFET is switched on. The end result is that LX_ current is regulated to 2.6A or less. A 2.6A inductor current is a large enough current to guarantee a 1A output load current under all intended operating conditions. The IC can operate indefinitely while regulating the inductor current to 2.6A or less.

However, if a short circuit or extremely heavy load is applied to the output, the output voltage decreases since the inductor current is limited to 2.6A.

If the output voltage decreases to less than 72% of the regulation voltage target (i.e., 2.8V with V_{OUT_TARGET} of 3.7V), a short circuit is assumed, and the IC returns to the shutdown state. The IC then attempts to start up if the output short is removed. Even if the output short persists indefinitely, the IC thermal protection ensures that the die is not damaged.

True Shutdown

During operation in boost mode, the p-channel MOSFET prevents current from flowing from OUT_ to LX_. In all other modes of operation, it is desirable to block current flowing from LX_ to OUT_. True Shutdown prevents current from flowing from LX_ to OUT_ while the IC is shut down by reversing the internal body diode of the p-channel MOSFET. This feature is also active during track/ATM to allow current limit to function as anticipated.

Upon leaving boost mode, the p-channel MOSFET continues to prevent current from flowing from OUT_ to LX_ until OUT_ and IN are approximately the same voltage. After this condition has been met, track/ATM and shutdown operate normally.

Table 1. Modes of Operation

V_{IN} COMPARATOR	EN	TREN	MODE OF OPERATION
X	0	0	True Shutdown
X	0	1	Track
$0 = V_{IN} < V_{ATM}$	1	X	Boost
$1 = V_{IN} > V_{ATM}$	1	X	ATM

X = Don't care.

Thermal Considerations

In most applications, the IC does not dissipate much heat due to its high efficiency. But in applications where the IC runs at high ambient temperature with heavy loads, the heat dissipated may cause the temperature to exceed the maximum junction temperature of the part. If the junction temperature reaches approximately +165°C, the thermal overload protection is activated.

The maximum power dissipation depends on the thermal resistance of the IC package and circuit board. The power dissipated (P_D) in the device is:

$$P_D = P_{OUT} \times (1/\eta - 1)$$

where η is the efficiency of the converter and P_{OUT} is the output power of the step-up converter. The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

where (T_{JMAX} - T_A) is the temperature difference between the IC's maximum rated junction temperature and the surrounding air, and θ_{JA} is the thermal resistance of the junction through the PCB, copper traces, and other materials to the surrounding air.

Applications Information

Step-Up Inductor Selection

Due to the small size of the recommended capacitor, the inductor's value is limited to approximately 1μH. Inductors of approximately 1μH guarantee stable operation of the converter with capacitance as small as 8μF (actual) present on the converter's output. If the inductor's value is reduced significantly below 1μH, ripple can become excessive.

Output Capacitor Selection

An output capacitor (C_{OUT}) is required to keep the output-voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors are highly recommended due to their small size and low ESR. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well. One 22μF (with a minimum actual capacitance of 6μF under operating conditions) is recommended. This capacitor along with an additional 10μF of bypass capacitance, associated with the load, guarantee proper performance of the IC. The minimum combined capacitance is required to be 8μF or larger. These capacitors can be found with case size 0603 or larger.

The output capacitor derating with output voltage naturally have a larger effect for higher output voltage versions of the device (> 5V). For these higher output voltages, more output capacitance is generally needed to maintain the required 8μF effective capacitance; use 2x 22μF (0603) for the local output capacitor and 1x 10μF (0402) for the point of load bypass capacitor.

Input Capacitor Selection

The input capacitor (CIN) reduces the current peaks drawn from the battery or input power source. The impedance of CIN at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided. A 4.7μF input capacitor is recommended for most applications. This assumes that the input power source has at least 22μF of additional capacitance near the IC. For optimum noise immunity and low input-voltage ripple, the input capacitor value can be increased.

Output Current

The device supports a peak output current of 1A. Continuous operation with 1A output current at elevated temperature is not guaranteed. With sustained high current (> 100ms, > 1A), the junction temperature (T_J) rises to the thermal shutdown threshold. The electrical characteristics table lists Minimum Continuous Output Current values that represent what the typical operating circuit can achieve when considering device and component variations. Note that a typical part on the EV kit can achieve more current than listed. The listed currents are calculations that consider normal variation for inductor DCR, inductance, input and output capacitor ESR, switching frequency, MOSFET RDS_{ON}, thermal effects, and LX_ nMOS. To calculate the Minimum Continuous Output Currents for a given system, refer to the **spreadsheet calculator**.

Recommended PCB Layout and Routing

Poor layout can affect the IC performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance, ground bounce, and voltage losses. Poor layout can also affect regulation and stability.

A good layout is implemented using the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short traces. These components carry high switching frequencies and large traces act like antennas. The output capacitor placement is the most important in the PCB layout and should be placed directly next to the IC. The inductor and input capacitor placement are secondary to the output capacitor's placement but should remain close to the IC.
- Route the output voltage path away from the inductor and LX_ switching node to minimize noise and magnetic interference.
- Maximize the size of the ground metal on the component side to help with thermal dissipation. Use a ground plane with several vias connecting to the component-side ground to further reduce noise interference on sensitive circuit nodes.

Refer to the MAX8969 Evaluation Kit for more details.

Chip Information

PROCESS: BiCMOS

Ordering Information

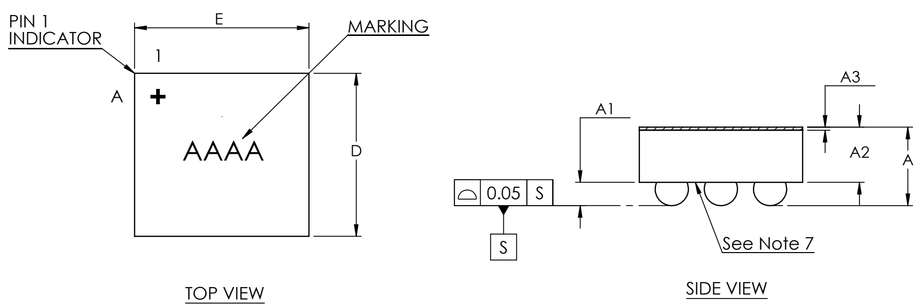
PART	V_{OUT} (V)	TEMP RANGE	PIN-PACKAGE
MAX8969EWL33+	3.3	-40°C to +85°C	9 WLP
MAX8969EWL35+	3.5	-40°C to +85°C	9 WLP
MAX8969EWL37+	3.7	-40°C to +85°C	9 WLP
MAX8969EWL42+	4.25	-40°C to +85°C	9 WLP
MAX8969EWL50+	5.0	-40°C to +85°C	9 WLP
MAX8969EWL55+	5.5	-40°C to +85°C	9 WLP
MAX8969EWL57+	5.7	-40°C to +85°C	9 WLP

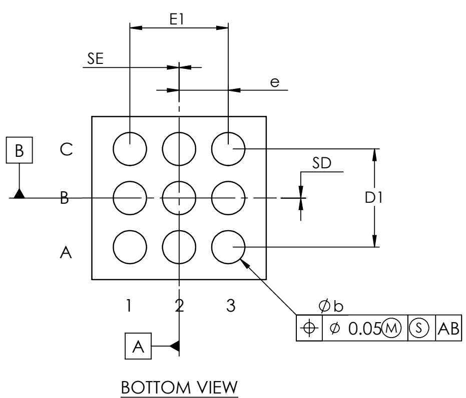
Note: *The output voltage range is from 3.3V to 5.7V. Contact the factory for output options and availability.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91B1+7	21-0459	Refer to Application Note 1891





COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.19	±0.03
A2	0.45	REF
A3	0.025	BASIC
b	Ø0.27	±0.03
D1	0.80	BASIC
E1	0.80	BASIC
e	0.40	BASIC
SD	0.00	BASIC
SE	0.00	BASIC

PKG. CODE	E	D	DEPOPULATED BUMPS
W91B1+7	1.260±0.040	1.260±0.040	NONE
W91C1+1	1.595±0.035	1.415±0.035	NONE
W91F1+1	1.435±0.015	1.345±0.015	NONE
W91G1+1	1.465±0.015	1.455±0.015	NONE
W91J1+1	1.238±0.015	1.238±0.015	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

maxim integrated™

TITLE: PACKAGE OUTLINE 9 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0459 | REV. G | 1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—
1	5/12	Updated *Electrical Characteristics* table	2
2	5/15	Updated *Benefits and Features* section	1
3	3/16	Updated *General Description*, *Ordering Information*, *Absolute Maximum Ratings*, *Package Thermal Characteristics*, *Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Description*, *Detailed Description*, *Output Capacitor Selection* sections, Figure 2, Table 1, and added *Output Current* section	1–12, 14–17

