

## Positive Doubling Charge Pumps with Shutdown in a SOT-23 Package

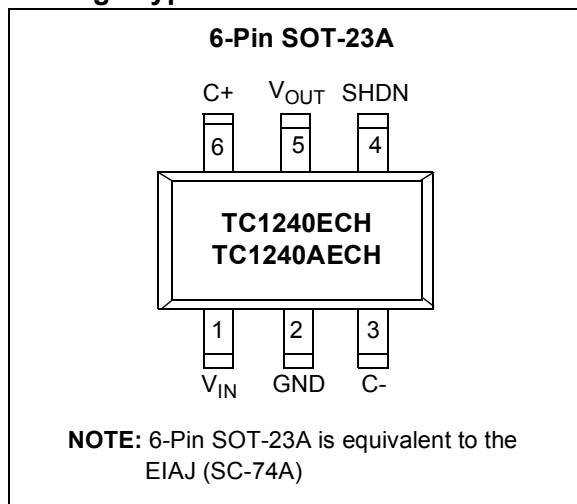
### Features

- Charge Pumps in 6-Pin SOT-23A Package
- >99% Typical Voltage Conversion Efficiency
- Voltage Doubling
- Input Voltage Range, TC1240: +2.5V to +4.0V,  
TC1240A: +2.5V to +5.5V
- Low Output Resistance, TC1240: 17Ω (Typical)  
TC1240A: 12Ω (Typical)
- Only Two External Capacitors Required
- Low Supply Current, TC1240: 180 μA (Typical)  
TC1240A: 550 μA (Typical)
- Power-Saving Shutdown Mode (1 μA Maximum)
- Shutdown Input Fully Compatible with 1.8V Logic Systems

### Applications

- Cellular Phones
- Pagers
- PDAs, Portable Data Loggers
- Battery Powered Devices
- Handheld Instruments

### Package Type

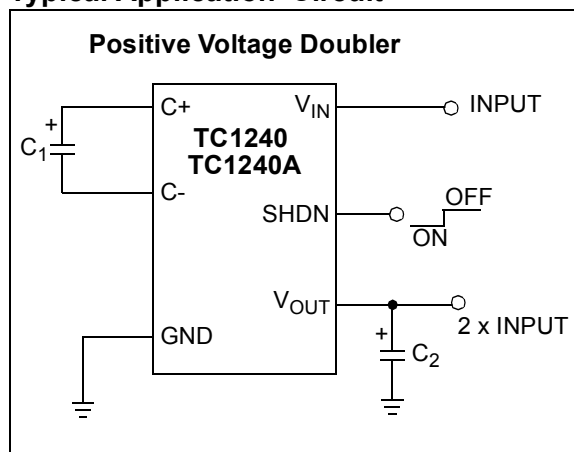


### General Description

The TC1240/TC1240A is a doubling CMOS charge pump voltage converter in a small 6-Pin SOT-23A package. The TC1240 doubles an input voltage that can range from +2.5V to +4.0V, while the TC1240A doubles an input voltage that can range from +2.5V to +5.5V. Conversion efficiency is typically >99%. Internal oscillator frequency is 160 kHz for both devices. The TC1240 and TC1240A have an active-high shutdown that limits the current consumption of the devices to less than 1 μA.

External component requirement is only two capacitors for standard voltage doubler applications. All other circuitry (including control, oscillator and power MOSFETs) are integrated on-chip. Typical supply current is 180 μA for the TC1240 and 550 μA for the TC1240A. Both devices are available in a 6-Pin SOT-23A surface mount package.

### Typical Application Circuit



# TC1240/TC1240A

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Input Voltage ( $V_{IN}$ to GND)	
TC1240 .....	+4.5V, -0.3V
TC1240A .....	+5.8V, -0.3V
Output Voltage ( $V_{OUT}$ to GND)	
TC1240 .....	+9.0V, $V_{IN}$ -0.3V
TC1240A .....	+11.6V, $V_{IN}$ -0.3V
Current at $V_{OUT}$ Pin.....	50 mA
Short-Circuit Duration: $V_{OUT}$ to GND .....	Indefinite
Thermal Resistance .....	210°C/W
Power Dissipation ( $T_A = +25^\circ\text{C}$ ).....	600 mW
Operating Temperature Range.....	-40°C to +85°C
Storage Temperature (Unbiased).....	-65°C to +150°C

† Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### TC1240 ELECTRICAL SPECIFICATIONS

**Electrical Specifications:** Unless otherwise noted, typical values apply at  $T_A = +25^\circ\text{C}$ . Minimum and maximum values apply for  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , and  $V_{IN} = +2.8\text{V}$ ,  $C_1 = C_2 = 3.3 \mu\text{F}$ , SHDN = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Current	$I_{DD}$	—	180	300	$\mu\text{A}$	$R_{LOAD} = \infty$
Shutdown Supply Current	$I_{SHDN}$	—	0.1	1.0	$\mu\text{A}$	SHDN = $V_{IN}$
Minimum Supply Voltage	$V_{MIN}$	2.5	—	—	V	$R_{LOAD} = 1.0 \text{ k}\Omega$
Maximum Supply Voltage	$V_{MAX}$	—	—	4.0	V	$R_{LOAD} = 1.0 \text{ k}\Omega$
Oscillator Frequency	$F_{OSC}$	—	160	—	kHz	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
Switching Frequency ( <b>Note 1</b> )	$F_{SW}$	40	80	125	kHz	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
Shutdown Input Logic High	$V_{IH}$	1.4	—	—	V	$V_{IN} = V_{MIN}$ to $V_{MAX}$
Shutdown Input Logic Low	$V_{IL}$	—	—	0.4	V	$V_{IN} = V_{MIN}$ to $V_{MAX}$
Power Efficiency	$P_{EFF}$	86	93	—	%	$R_{LOAD} = 1.0 \text{ k}\Omega$
Voltage Conversion Efficiency	$V_{EFF}$	97.5	99.96	—	%	$R_{LOAD} = \infty$
Output Resistance ( <b>Note 2</b> )	$R_{OUT}$	—	17	—	$\Omega$	$R_{LOAD} = 1.0 \text{ k}\Omega$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
		—	—	30		

**Note 1:** Switching frequency is one-half internal oscillator frequency.

**Note 2:** Capacitor contribution is approximately 26% of the output impedance [ $\text{ESR} = 1 / \text{switching frequency} \times \text{capacitance}$ ].

## TC1240A ELECTRICAL SPECIFICATIONS

**Electrical Specifications:** Unless otherwise noted, typical values apply at  $T_A = +25^\circ\text{C}$ . Minimum and maximum values apply for  $T_A = -40^\circ$  to  $+85^\circ\text{C}$ , and  $V_{IN} = +5.0\text{V}$ ,  $C_1 = C_2 = 3.3 \mu\text{F}$ ,  $\text{SHDN} = \text{GND}$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Current	$I_{DD}$	—	550	900	$\mu\text{A}$	$R_{LOAD} = \infty$
Shutdown Supply Current	$I_{SHDN}$	—	0.01	1.0	$\mu\text{A}$	$\text{SHDN} = V_{IN}$
Minimum Supply Voltage	$V_{MIN}$	2.5	—	—	V	
Maximum Supply Voltage	$V_{MAX}$	—	—	5.5	V	
Output Current	$I_{LOAD}$	20	—	—	mA	
Sum of the $R_{DS(ON)}$ of the internal MOSFET Switches	$R_{SW}$	—	4	8	$\Omega$	$I_{LOAD} = 20 \text{ mA}$
Oscillator Frequency	$F_{OSC}$	—	160	—	kHz	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
Switching Frequency ( <b>Note 1</b> )	$F_{SW}$	40	80	125	kHz	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
Shutdown Input Logic High	$V_{IH}$	1.4	—	—	V	$V_{IN} = V_{MIN}$ to $V_{MAX}$
Shutdown Input Logic Low	$V_{IL}$	—	—	0.4	V	$V_{IN} = V_{MIN}$ to $V_{MAX}$
Power Efficiency	$P_{EFF}$	86	94	—	%	$I_{LOAD} = 5 \text{ mA}$
Voltage Conversion Efficiency	$V_{EFF}$	99	99.96	—	%	$R_{LOAD} = \infty$
Output Resistance ( <b>Note 2</b> )	$R_{OUT}$	—	12	—	$\Omega$	$I_{LOAD} = 20 \mu\text{A}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

**Note 1:** Switching frequency is one-half internal oscillator frequency.

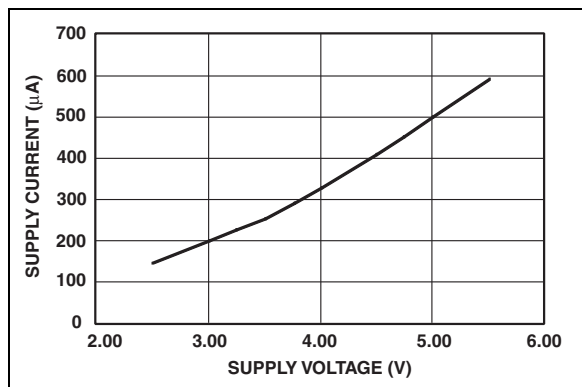
**2:** Capacitor contribution is approximately 26% of the output impedance [ $\text{ESR} = 1 / \text{switching frequency} \times \text{capacitance}$ ].

# TC1240/TC1240A

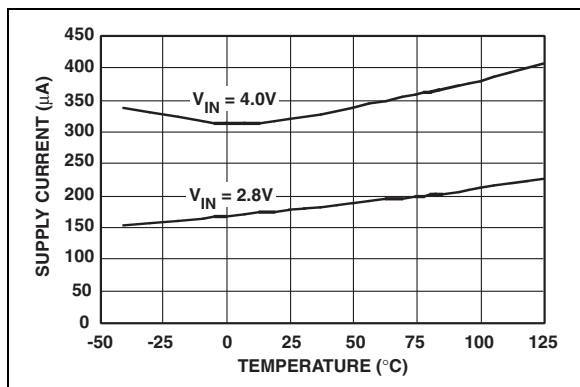
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

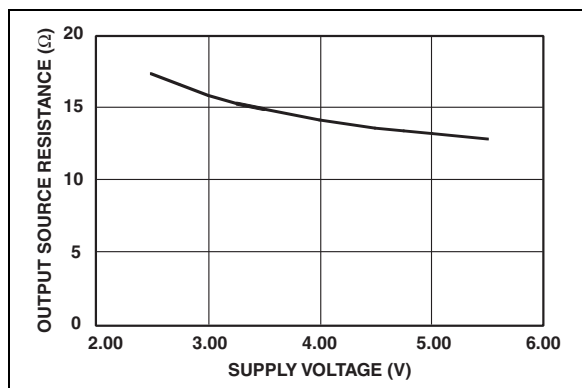
**Note:** Unless otherwise indicated, typical values apply at  $T_A = +25^\circ\text{C}$ .



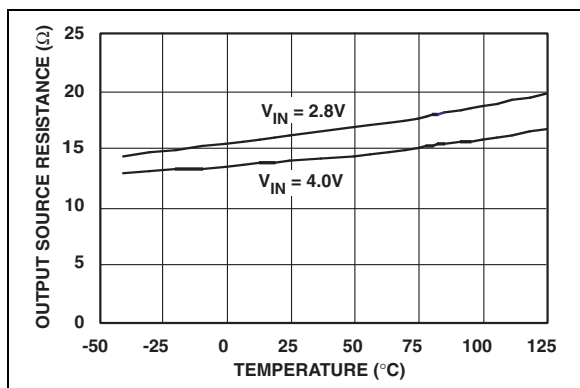
**FIGURE 2-1:** Supply Current vs. Supply Voltage (No Load).



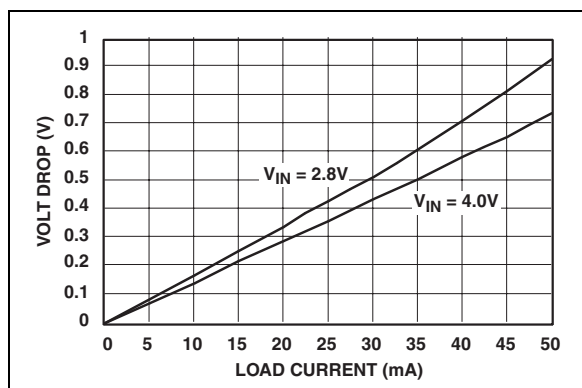
**FIGURE 2-4:** Supply Current vs. Temperature (No Load).



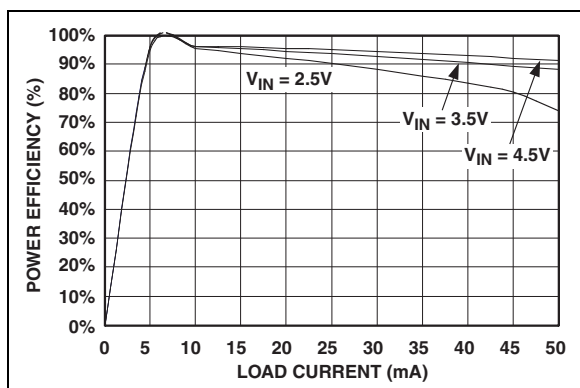
**FIGURE 2-2:** Output Source Resistance vs. Supply Voltage (with  $R_{LOAD} = 1\text{ k}\Omega$ )



**FIGURE 2-5:** Output Source Resistance vs. Temperature (with  $R_{LOAD} = 1\text{ k}\Omega$ ).

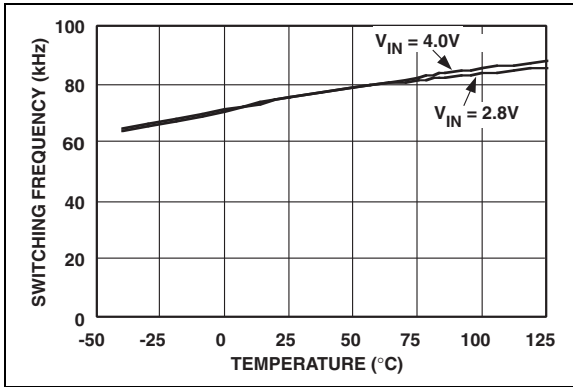


**FIGURE 2-3:** Output Voltage Drop vs. Load Current.



**FIGURE 2-6:** Power Efficiency vs. Load Current.

**Note:** Unless otherwise indicated, typical values apply at  $T_A = +25^\circ\text{C}$ .



**FIGURE 2-7:** Switching Frequency vs. Temperature.

# TC1240/TC1240A

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## 3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

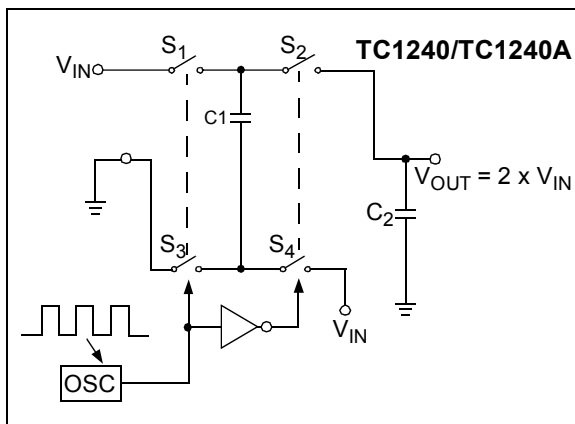
**TABLE 3-1: PIN FUNCTION TABLE**

Pin No.	Symbol	Description
1	$V_{IN}$	Power supply input
2	GND	Ground
3	C-	Commutation capacitor negative terminal
4	SHDN	Shutdown input (active high)
5	$V_{OUT}$	Doubled output voltage
6	C+	Commutation capacitor positive terminal

## 4.0 DETAILED DESCRIPTION

The TC1240/TC1240A charge pump converter doubles the voltage applied to the  $V_{IN}$  pin. Conversion consists of a two-phase operation (Figure 4-1). During the first phase, switches  $S_2$  and  $S_4$  are open and  $S_1$  and  $S_3$  are closed. During this time,  $C_1$  charges to the voltage on  $V_{IN}$  and load current is supplied from  $C_2$ . During the second phase,  $S_2$  and  $S_4$  are closed, while  $S_1$  and  $S_3$  are open.

During this second phase,  $C_1$  is level-shifted upward by  $V_{IN}$  volts. This connects  $C_1$  to the reservoir capacitor  $C_2$ , allowing energy to be delivered to the output as needed. The actual voltage is slightly lower than  $2 \times V_{IN}$  since the four switches ( $S_1$ - $S_4$ ) have an on-resistance and the load drains charge from reservoir capacitor  $C_2$ .



**FIGURE 4-1:** Ideal Switched Capacitor Charge Pump Doubler.

## 5.0 TYPICAL APPLICATIONS

### 5.1 Output Voltage Considerations

The TC1240/TC1240A performs voltage doubling but does not provide regulation. The output voltage will droop in a linear manner with respect to load current. The value of this equivalent output resistance is approximately  $12\Omega$  nominal at  $+25^\circ\text{C}$  and  $V_{IN} = +5.0\text{V}$  for the TC1240A and  $17\Omega$  nominal at  $+25^\circ\text{C}$  and  $V_{IN} = +2.8\text{V}$  for the TC1240.  $V_{OUT}$  is approximately  $+10.0\text{V}$  at light loads for the TC1240A and  $+5.6\text{V}$  for the TC1240, and droops according to the equation below:

### EQUATION

$$V_{DROOP} = I_{OUT} \times R_{OUT}$$

$$V_{OUT} = 2 \times V_{IN} - V_{DROOP}$$

### 5.2 Charge Pump Efficiency

The overall power efficiency of the charge pump is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. (which vary with input voltage, temperature and oscillator frequency).
2.  $I^2R$  losses due to the on-resistance of the MOSFET switches on-board the charge pump.
3. Charge pump capacitor losses due to effective series resistance (ESR).
4. Losses that occur during charge transfer (from commutation capacitor to the output capacitor) when a voltage difference between the two capacitors exist.

Most of the conversion losses are due to factors (2) and (3) above. These losses are given by Equation 5-1.

### EQUATION 5-1:

$$\text{a) } P_{LOSS(2,3)} = I_{OUT}^2 \times R_{OUT}$$

$$\text{b) } R_{OUT} = \left[ \frac{I}{F_{SW}(C_1)} \right] + 8R_{SWITCH} + 4ESR_{C1} + ESR_{C2}$$

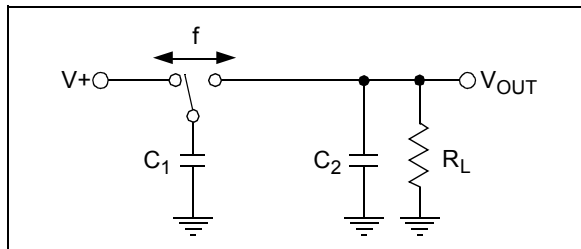
# TC1240/TC1240A

The switching frequency in Equation 5-1b is defined as one-half the oscillator frequency (i.e.,  $F_{SW} = F_{OSC}/2$ ). The  $1/(F_{SW})(C_1)$  term in Equation 5-1b is the effective output resistance of an ideal switched capacitor circuit (Figure 5-1 and Figure 5-2).

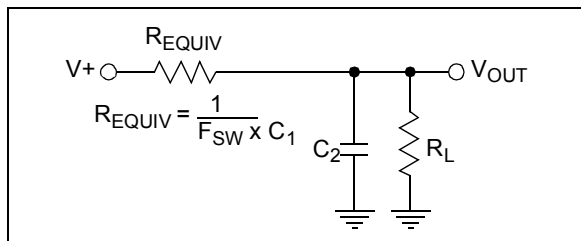
The output voltage ripple is given by Equation 5-2.

## EQUATION 5-2:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(F_{SW})(C_2)} + 2(I_{OUT})(ESR_{C_2})$$



**FIGURE 5-1:** Ideal Switched Capacitor Model.



**FIGURE 5-2:** Equivalent Output Resistance.

## 5.3 Capacitor Selection

In order to maintain the lowest output resistance and output ripple voltage, it is recommended that low ESR capacitors be used. Additionally, larger values of  $C_1$  will lower the output resistance and larger values of  $C_2$  will reduce output ripple (see Equation 5-1b).

Table 5-1 shows various values of  $C_1$  and the corresponding output resistance values @ +25°C. It assumes a  $0.1\Omega$   $ESR_{C_1}$  and  $0.9\Omega$   $R_{SW}$ . Table 5-2 shows the output voltage ripple for various values of  $C_2$ . The  $V_{RIPPLE}$  values assume 5mA output load current and  $0.1\Omega$   $ESR_{C_2}$ .

**TABLE 5-1: OUTPUT RESISTANCE VS.  $C_1$  (ESR = 0.1Ω)**

$C_1$ (μF)	TC1240 $R_{OUT}(\Omega)$	TC1240A $R_{OUT}(\Omega)$
0.47	47	35
1	28.5	20.5
2.2	19.5	14
3.3	17	12
4.7	15.5	10.5
10	13.6	9.3
47	12.5	8.3
100	12.2	8.1

**TABLE 5-2: OUTPUT VOLTAGE RIPPLE VS.  $C_2$  (ESR = 0.1Ω)  $I_{OUT}$  5 mA**

$C_1$ (μF)	TC1240/TC1240A $V_{RIPPLE}$ (mV)
0.47	142
1	67
2.2	30
3.3	20
4.7	14
10	6.7
47	2.5
100	1.6



## 5.4 Input Supply Bypassing

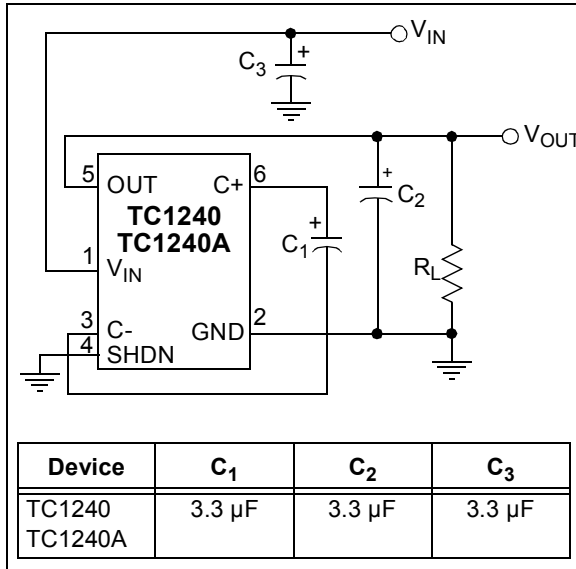
The  $V_{IN}$  input should be capacitively bypassed to reduce AC impedance and minimize noise effects due to the switching internal to the device. The recommended capacitor should be a large value (at least equal to  $C_1$ ) connected from the input to GND.

## 5.5 Shutdown Input

The TC1240 and TC1240A are disabled when SHDN is high, and enabled when SHDN is low. This input cannot be allowed to float.

## 5.6 Voltage Doubler

The most common application for charge pump devices is the doubler (Figure 5-3). This application uses two external capacitors –  $C_1$  and  $C_2$  (plus a power supply bypass capacitor, if necessary). The output is equal to  $2 \times V_{IN}$  minus any voltage drops due to loading. Refer to Table 5-1 and Table 5-2 for capacitor selection.



**FIGURE 5-3:** Test Circuit.

# TC1240/TC1240A

## 5.7 Cascading Devices

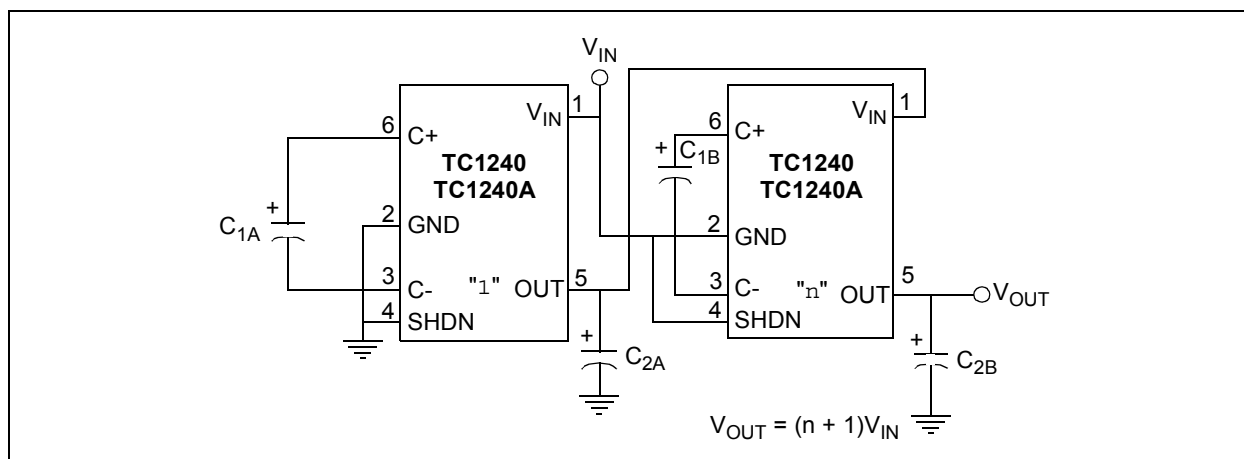
Two or more TC1240/TC1240As can be cascaded to increase output voltage (Figure 5-4). If the output is lightly loaded, it will be close to  $((n + 1) \times V_{IN})$ , but will droop at least by  $R_{OUT}$  of the first device multiplied by the  $I_Q$  of the second. It can be seen that the output resistance rises rapidly for multiple cascaded devices. For the case of the two-stage 'tripler', output resistance can be approximated as  $R_{OUT} = 2 \times R_{OUT1} + R_{OUT2}$ , where  $R_{OUT1}$  is the output resistance of the first stage and  $R_{OUT2}$  is the output resistance of the second stage.

## 5.8 Paralleling Devices

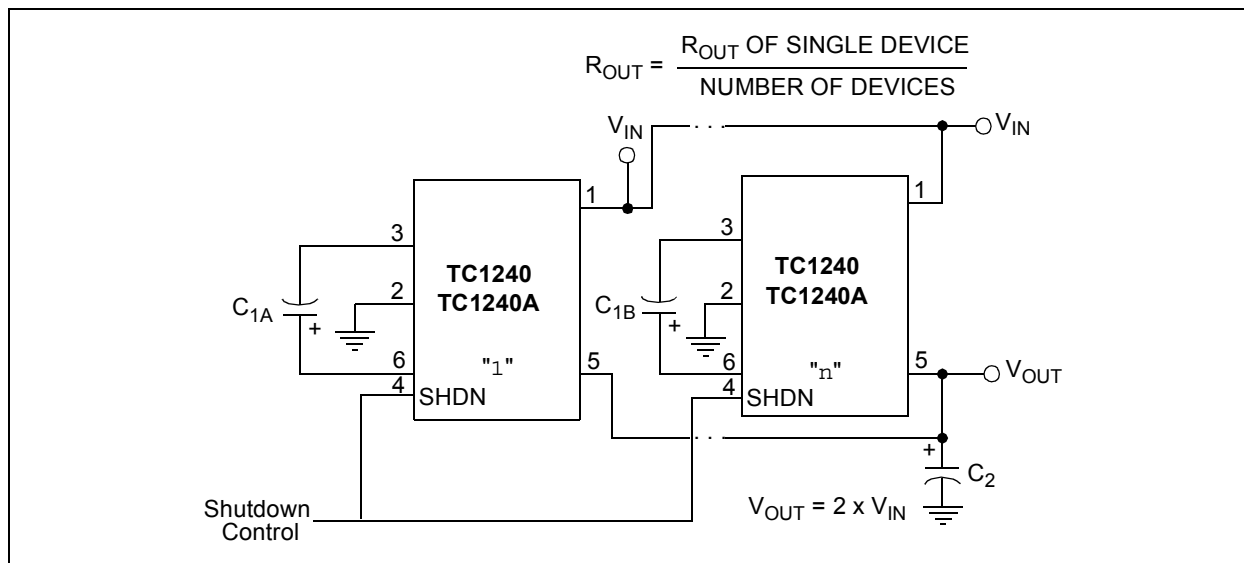
To reduce the value of  $R_{OUT}$ , multiple TC1240/TC1240As can be connected in parallel (Figure 5-5). The output resistance will be reduced by a factor of N, where N is the number of TC1240/TC1240As. Each device will require its own pump capacitor ( $C_{1x}$ ), but all devices may share one reservoir capacitor ( $C_2$ ). However, to preserve ripple performance, the value of  $C_2$  should be scaled according to the number of paralleled TC1240/TC1240As, respectively.

## 5.9 Layout Considerations

As with any switching power supply circuit good layout practice is recommended. Mount components as close together as possible to minimize stray inductance and capacitance. Also use a large ground plane to minimize noise leakage into other circuitry.



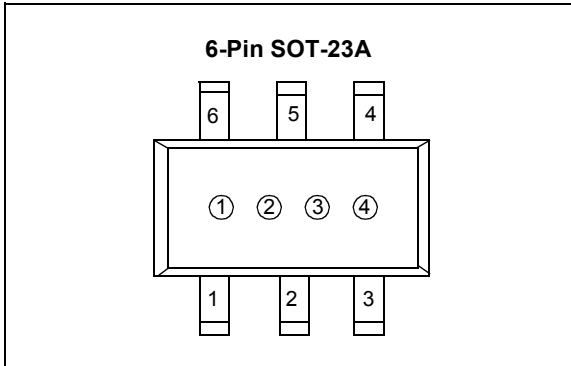
**FIGURE 5-4:** Cascading Multiple Devices To Increase Output Voltage.



**FIGURE 5-5:** Paralleling Multiple Devices To Reduce Output Resistance.

## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information



① & ② = part number code + temperature range  
(two-digit code)

Device	Code
TC1240	DN
TC1240A	EN

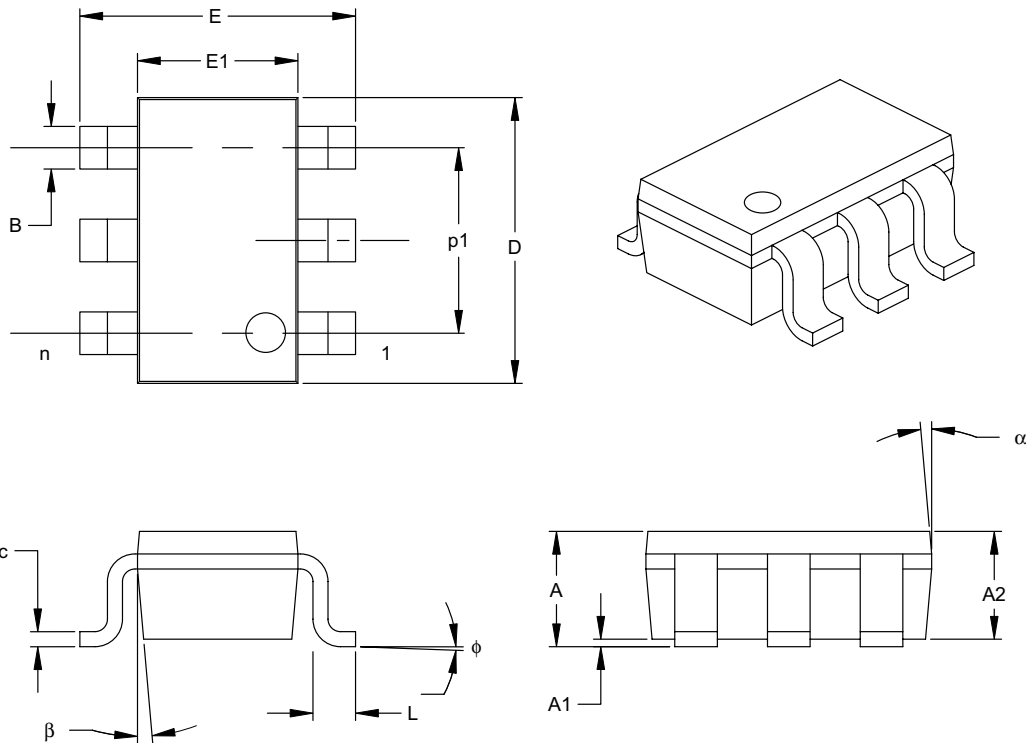
ex: 1240AECH = ① ② ③ ④

③ represents year and 2-month code

④ represents production lot ID code

# TC1240/TC1240A

## 6-Lead Plastic Small Outline Transistor (CH) (SOT-23)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device	TC1240: Positive Doubling Charge Pump with Shutdown TC1240A Positive Doubling Charge Pump with Shutdown	
Temperature Range	I = -40°C to +85°C (Industrial)	
Package	CHTR: = 6L SOT-23, Tape and Reel	

**Examples:**

- a) TC1240ECHTR: Tape and Reel, 6L SOT-23 (EIAJ)
- b) TC1240AECHTR: Tape and Reel, 6L SOT-23 (EIAJ)

## Sales and Support

### **Data Sheets**

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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# TC1240/TC1240A

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NOTES:

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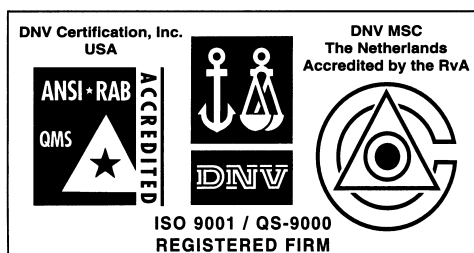
Accuron, Application Maestro, dsPIC, dsPICDEM, dsPICDEM.net, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICC, PICkit, PICDEM, PICDEM.net, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rPIC, Select Mode, SmartSensor, SmartShunt, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

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*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*



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