# N-Channel Enhancement-Mode Vertical DMOS FETs

## Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low $C_{ISS}$ and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

## Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

## General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Ordering Information

| Part Number | Package Option | Packing |
|---|---|---|
| VN3205N3-G | 3-Lead TO-92 | 1000/Bag |
| VN3205N3-G P002 | 3-Lead TO-92 | 2000/Reel |
| VN3205N3-G P003 | | |
| VN3205N3-G P005 | | |
| VN3205N3-G P013 | | |
| VN3205N3-G P014 | | |
| VN3205N8-G | 3-Lead TO-243AA (SOT-89) | 2000/Reel |
| VN3205NW | Die in wafer form | --- |
| VN3205NJ | Die on adhesive tape | --- |
| VN3205ND | Die in waffle pack | --- |

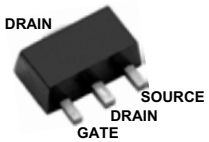
*For packaged products, -G indicates package is RoHS compliant ('Green').*
*TO-92 taping specifications and winding styles per EIA-468 Standard.*
*Devices in Wafer / Die form are RoHS compliant ('Green').*
*Refer to Die Specification VF32 for layout and dimensions.*

## Product Summary

| $BV_{DSS}/BV_{DGS}$ (V) | $R_{DS(ON)}$ (max) (Ω) | $V_{GS(th)}$ (max) (V) |
|---|---|---|
| 50 | 0.3 | 2.4 |

## Pin Configuration


**TO-92 (N3)**




**TO-243AA (SOT-89) (N8)**

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain-to-source voltage | $BV_{DSS}$ |
| Drain-to-gate voltage | $BV_{DGS}$ |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

## Typical Thermal Resistance

| Package | $\theta_{ja}$ |
|---|---|
| 3-Lead TO-92 | 132°C/W |
| 3-Lead TO-243AA (SOT-89) | 133°C/W |

## Product Marking


YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

*Package may or may not include the following marks: Si or*

**TO-92 (N3)**


W = Code for week sealed
_____ = "Green" Packaging

*Package may or may not include the following marks: Si or*

**TO-243AA (SOT-89) (N8)**

## Thermal Characteristics

| Package | $I_D$ (continuous)* (A) | $I_D$ (pulsed) (A) | Power Dissipation @$T_C$ = 25°C (W) | $I_{DR}$† (A) | $I_{DRM}$ (A) |
|---|---|---|---|---|---|
| TO-92 | 1.2 | 8.0 | 1.0 | 1.2 | 8.0 |
| TO-243AA | 1.5 | 8.0 | 1.6 ($T_A$ = 25°) | 1.5 | 8.0 |

***Notes:***

* $I_D$ (continuous) is limited by max rated $T_j$, $T_a$ = 25°C.

† Total for package.

‡ Mounted on FR5 board, 25mm x 25mm x 1.57mm.

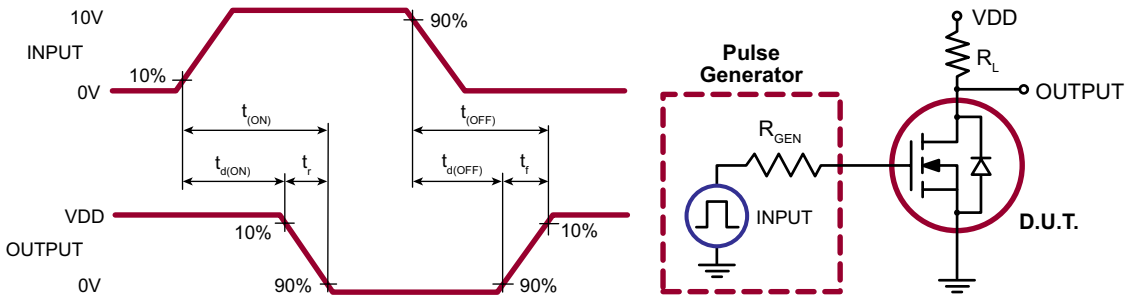
## Electrical Characteristics ($T_j$ = 25°C unless otherwise specified)

| Sym | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source breakdown voltage | | 50 | - | - | V | $V_{GS}$ = 0V, $I_D$ = 10mA |
| $V_{GS(th)}$ | Gate threshold voltage | | 0.8 | - | 2.4 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 10mA |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with temperature | | - | -4.3 | -5.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = 10mA |
| $I_{GSS}$ | Gate body leakage current | | - | 1.0 | 100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero Gate voltage drain current | | - | - | 10 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Max Rating |
| | | | - | - | 1.0 | mA | $V_{DS}$ = 0.8 Max Rating, $V_{GS}$ = 0V, $T_A$ = 125°C |
| $I_{D(ON)}$ | ON-state Drain current | | 3.0 | 14 | - | A | $V_{GS}$ = 10V, $V_{DS}$ = 5.0V |
| $R_{DS(ON)}$ | Static Drain-to-Source ON-state resistance | TO-92 | - | - | 0.45 | Ω | $V_{GS}$ = 4.5V, $I_D$ = 1.5A |
| | | TO-243AA | - | - | 0.45 | | $V_{GS}$ = 4.5V, $I_D$ = 0.75A |
| | | TO-92 | - | - | 0.3 | | $V_{GS}$ = 10V, $I_D$ = 3.0A |
| | | TO-243AA | - | - | 0.3 | | $V_{GS}$ = 10V, $I_D$ = 1.5A |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | | - | 0.85 | 1.2 | %/°C | $V_{GS}$ = 10V, $I_D$ = 3.0A |
| $G_{FS}$ | Forward transconductance | | 1.0 | 1.5 | - | mho | $V_{DS}$ = 25V, $I_D$ = 2.0A |
| $C_{ISS}$ | Input capacitance | | - | 220 | 300 | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1.0MHz |
| $C_{OSS}$ | Common Source output capacitance | | - | 70 | 120 | | |
| $C_{RSS}$ | Reverse transfer capacitance | | - | 20 | 30 | | |
| $t_{d(ON)}$ | Turn-on delay time | | - | - | 10 | ns | $V_{DD}$ = 25V, $I_D$ = 2.0A, $R_{GEN}$ = 10Ω |
| $t_r$ | Rise time | | - | - | 15 | | |
| $t_{d(OFF)}$ | Turn-off delay time | | - | - | 25 | | |
| $t_f$ | Fall time | | - | - | 25 | | |
| $V_{SD}$ | Diode forward voltage drop | | - | - | 1.6 | V | $V_{GS}$ = 0V, $I_{SD}$ = 1.5A |
| $t_{rr}$ | Reverse recovery time | | - | 300 | - | ns | $V_{GS}$ = 0V, $I_{SD}$ = 1.0A |

***Notes:***

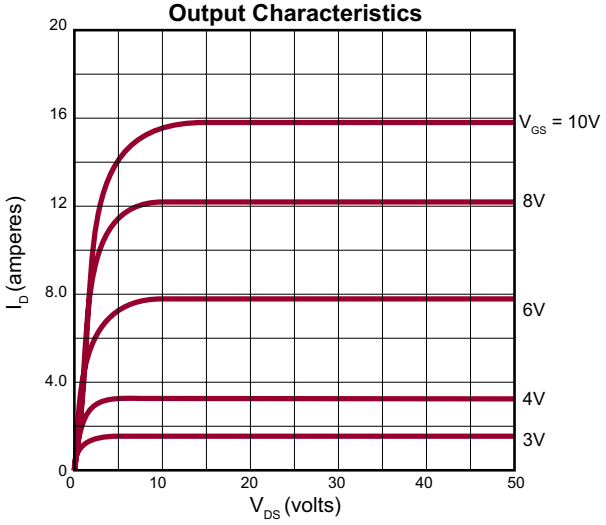
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

## Switching Waveforms and Test Circuit

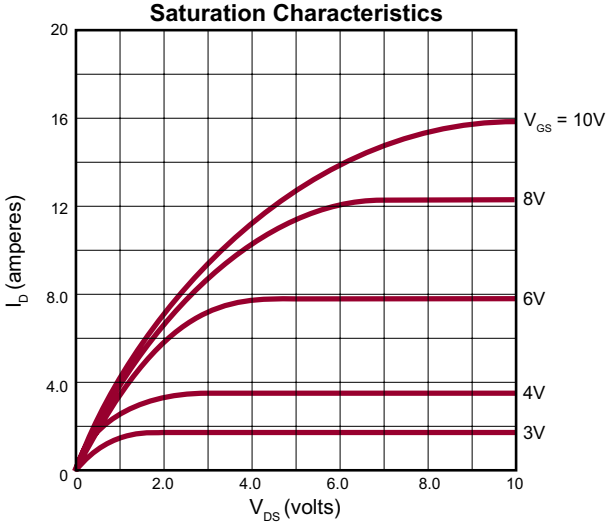


## Typical Performance Curves

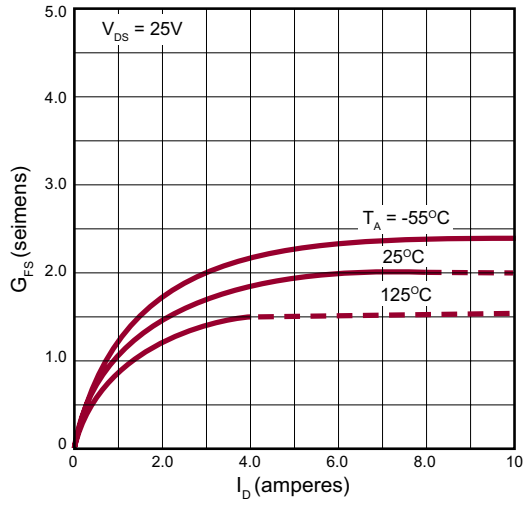
Output Characteristics



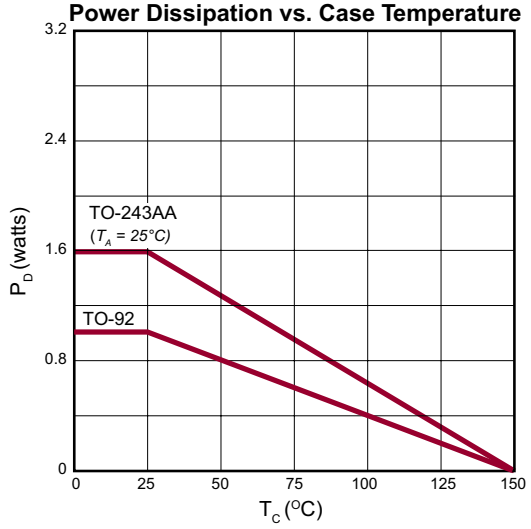

Saturation Characteristics



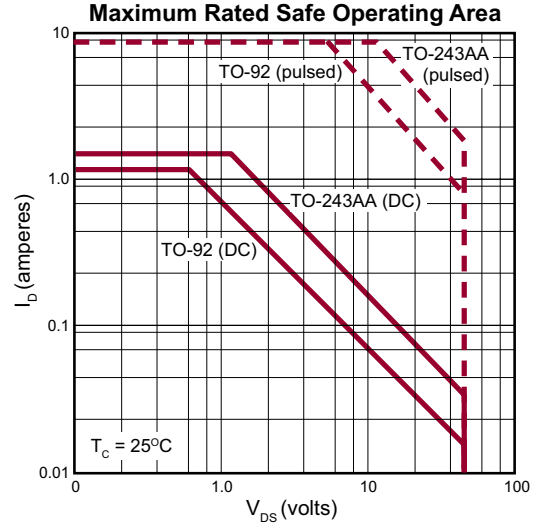

Transconductance vs. Drain Current



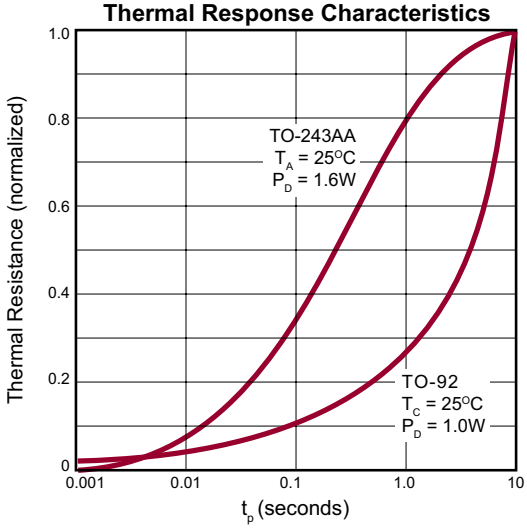

Power Dissipation vs. Case Temperature




Maximum Rated Safe Operating Area

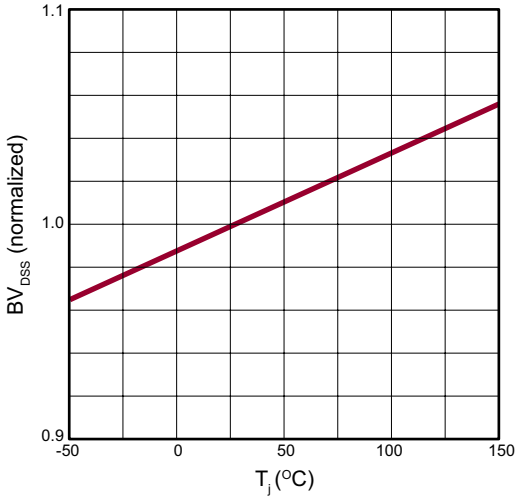



Thermal Response Characteristics

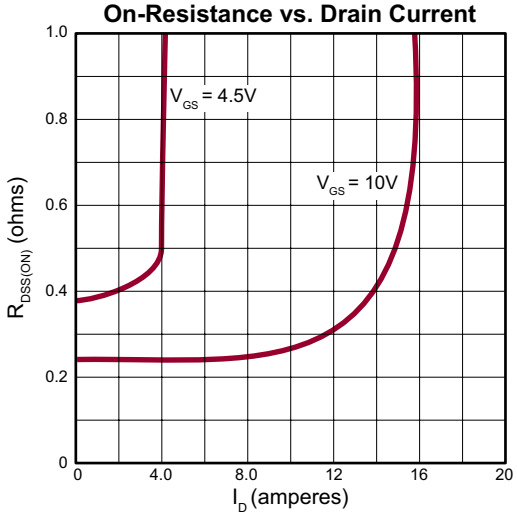


## Typical Performance Curves *(cont.)*

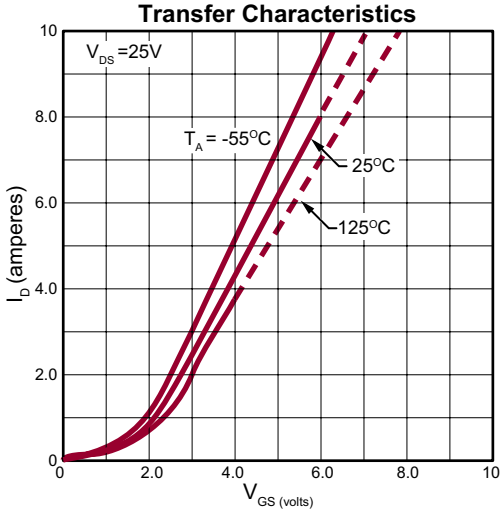
**$BV_{DSS}$ Variation with Temperature**



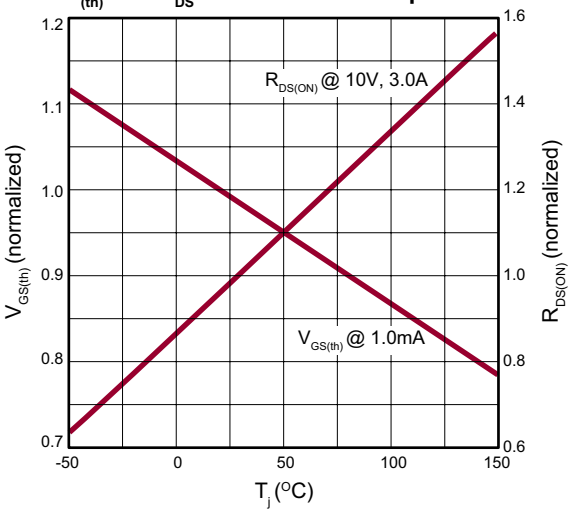

**On-Resistance vs. Drain Current**



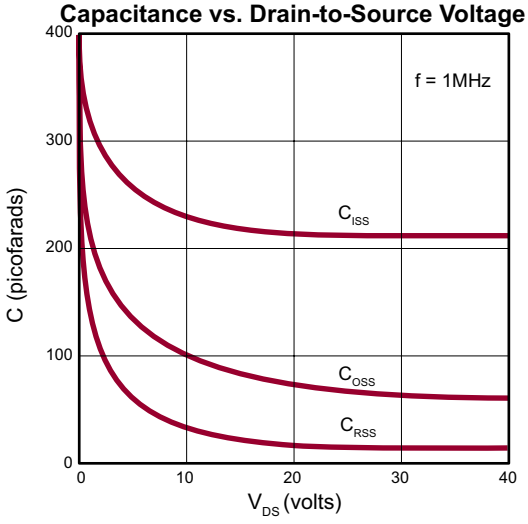

**Transfer Characteristics**



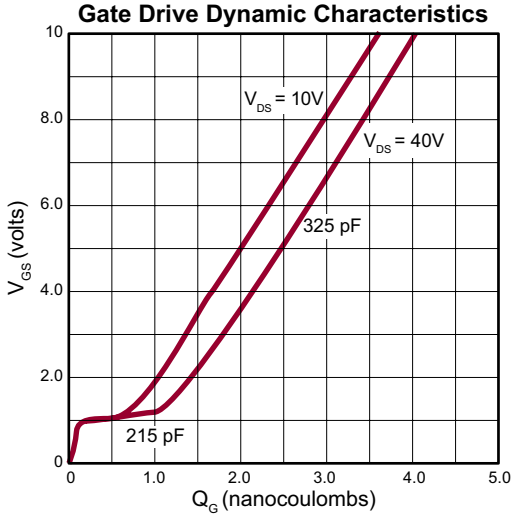

**$V_{(th)}$ and $R_{DS}$ Variation with Temperature**



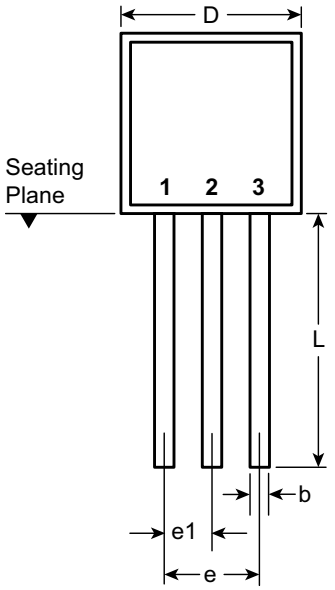

**Capacitance vs. Drain-to-Source Voltage**



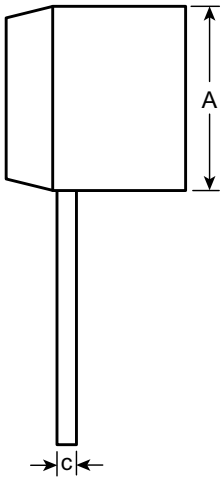

**Gate Drive Dynamic Characteristics**



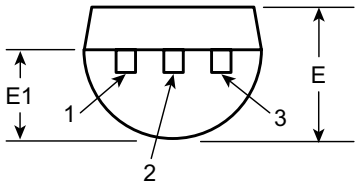
# 3-Lead TO-92 Package Outline (N3)




**Front View**




**Side View**

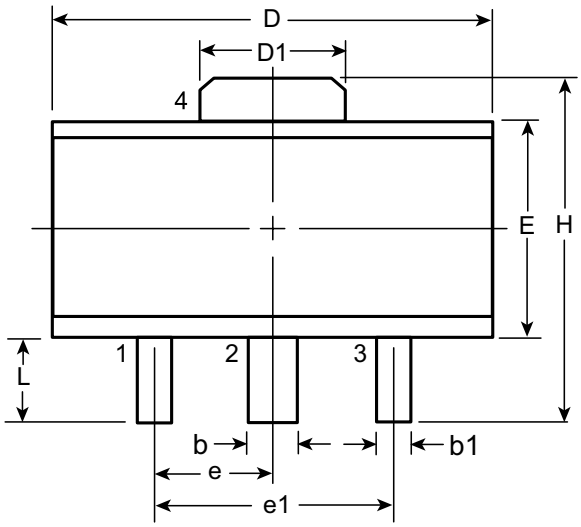



**Bottom View**

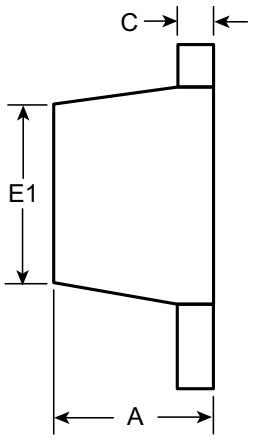
| Symbol | | A | b | c | D | E | E1 | e | e1 | L |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (inches) | MIN | .170 | .014† | .014† | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022† | .022† | .205 | .165 | .105 | .105 | .055 | .610* |

*JEDEC Registration TO-92.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

# 3-Lead TO-243AA (SOT-89) Package Outline (N8)




**Top View**




**Side View**

| Symbol | | A | b | b1 | C | D | D1 | E | E1 | e | e1 | H | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (mm) | MIN | 1.40 | 0.44 | 0.36 | 0.35 | 4.40 | 1.62 | 2.29 | 2.00† | 1.50 BSC | 3.00 BSC | 3.94 | 0.73† |
| | NOM | - | - | - | - | - | - | - | - | | | - | - |
| | MAX | 1.60 | 0.56 | 0.48 | 0.44 | 4.60 | 1.83 | 2.60 | 2.29 | | | 4.25 | 1.20 |

*JEDEC Registration TO-243, Variation AA, Issue C, July 1986.*
***†*** *This dimension differs from the JEDEC drawing*
***Drawings not to scale.***
***Supertex Doc. #:*** *DSPD-3TO243AAN8, Version F111010.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*

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