

NX18P3001

Bidirectional high-side power switch for charger and USB-OTG combined applications

Rev. 1 — 24 September 2013

Product data sheet

1. General description

The NX18P3001 is an advanced bidirectional power switch and ESD- protection device for combined USB-OTG and charger port applications. It includes undervoltage lockout, overvoltage lockout and overtemperature protection circuits designed to automatically isolate the power switch terminals when a fault condition occurs.

The device features two power switch input/output terminals (VBUSI and VBUSO), an open-drain acknowledge output (ACK), an enable input which includes logic level translation ($\overline{\text{EN}}$) and low capacitance Transient Voltage Suppression (TVS) type ESD clamps for USB data and ID pins.

When $\overline{\text{EN}}$ is set HIGH the device enters a low-power mode, disabling all protection circuits. When used in combined charger and USB-OTG applications the 30 V tolerant VBUSI switch terminal is used as the supply and switch input when charging, for USB-OTG the VBUSO switch terminal is used as the supply and switch input.

Designed for operation from 3.2 V to 17.5 V, it is used in battery charging and power domain isolation applications to reduce power dissipation and extend battery life.

2. Features and benefits

- 30 V tolerant VBUSI supply pin
- Wide supply voltage range from 3.2 V to 17.5 V
- Automatic switch operation for charging within the supply range
- I_{SW} maximum 3 A continuous current
- Low ON resistance: 62 m Ω (typical) at a supply voltage of 5.0 V
- 1.8 V control logic input to open the switch
- Soft start turn-on slew rate
- Protection circuitry
 - ◆ Overtemperature protection
 - ◆ Overvoltage lockout
 - ◆ Undervoltage lockout
- ESD protection:
 - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - ◆ CDM AEC standard Q100-01 (JESD22-C101E)
 - ◆ IEC61000-4-2 contact discharge exceeds 8 kV for pins VBUSI, D-, D+ and ID
- Specified from -40 °C to +85 °C



3. Applications

- Smart and feature phones
- Tablets, eBooks

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|---------|--|-----------|
| | Temperature range | Name | Description | |
| NX18P3001UK | -40 °C to +85 °C | WLCSP12 | wafer level chip-scale package, 12 bumps; body 1.36 × 1.66 × 0.51 mm (Backside Coating included) | NX18P3001 |

5. Marking

Table 2. Marking codes

| Type number | Marking code |
|-------------|--------------|
| NX18P3001UK | X18P3 |

6. Functional diagram

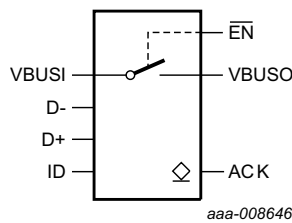


Fig 1. Logic symbol

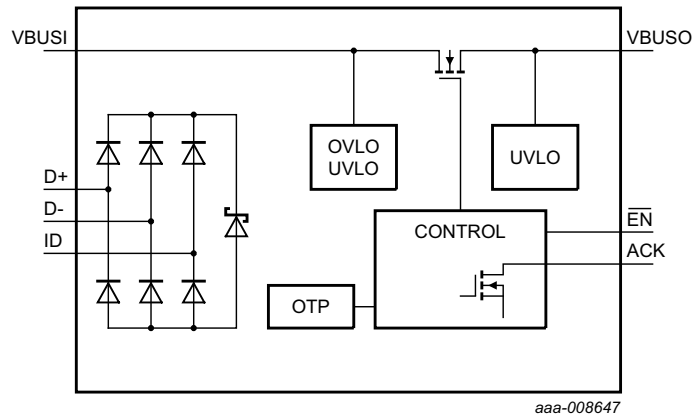


Fig 2. Logic diagram (simplified schematic)

7. Pinning information

7.1 Pinning

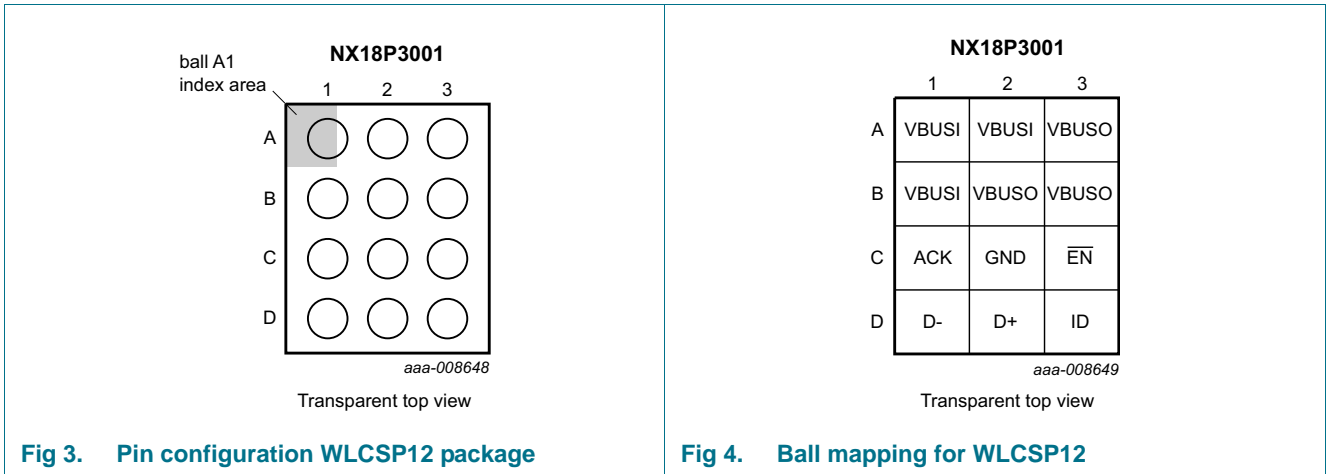


Fig 3. Pin configuration WLCSP12 package

Fig 4. Ball mapping for WLCSP12

7.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|--------|------------|---|
| VBUSO | A3, B2, B3 | VBUSO (output/input supply) |
| VBUSI | A1, A2, B1 | VBUSI (input supply/output) |
| ACK | C1 | acknowledge condition indicator (open-drain output) |
| GND | C2 | ground (0 V) |
| EN | C3 | enable input (active LOW) |
| D- | D1 | ESD-protection I/O |
| D+ | D2 | ESD-protection I/O |
| ID | D3 | ESD-protection I/O |

8. Functional description

Table 4. Function table^[1]

| $\overline{\text{EN}}$ | VBUSI | VBUSO | ACK | Operation mode |
|------------------------|------------------------|---------|-----|---|
| L | < 3.2 V | < 3.2 V | Z | undervoltage lockout; switch open |
| L | 3.2 V < VBUSI < 17.5 V | < 3.2 V | Z | enabled; switch closed; charging mode |
| L | < 3.2 V | > 3.2 V | Z | enabled; switch closed; OTG mode |
| L | X | X | 0 | overtemperature protection; switch open |
| L | > 17.5 V | X | 0 | overvoltage lockout; switch open |
| H | X | X | Z | disabled; switch open |

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

8.1 $\overline{\text{EN}}$ -input

A HIGH on $\overline{\text{EN}}$ disables the N-channel MOSFET and all protection circuits putting the device into a low-power mode. A LOW on $\overline{\text{EN}}$ enables the protection circuits and then the N-channel MOSFET.

8.2 Undervoltage lockout

When $\overline{\text{EN}}$ is LOW and VBUSI and VBUSO < 3.2 V, the UnderVoltage LockOut (UVLO) circuits disable the N-channel MOSFET. Once VBUSI or VBUSO > 3.3 V and no other protection circuits are active, the state of the N-channel MOSFET is controlled by the $\overline{\text{EN}}$ pin.

8.3 Overvoltage lockout

When $\overline{\text{EN}}$ is LOW and VBUSI > 17.5 V, the OverVoltage LockOut (OVLO) circuit disables the N-channel MOSFET and set the ACK output LOW. Once VBUSI < 17.35 V and no other protection circuits are active, ACK is set high impedance and the state of the N-channel MOSFET is controlled by the $\overline{\text{EN}}$ pin.

8.4 Overtemperature protection

When $\overline{\text{EN}}$ is LOW and the device temperature exceeds 125 °C the OverTemperature Protection (OTP) circuit disables the N-channel MOSFET and sets the ACK output LOW. Once the device temperature decreases to below 115 °C and no other protection circuits are active, ACK is set high impedance and the state of the N-channel MOSFET is controlled by the $\overline{\text{EN}}$ pin.

8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. If OVLO or OTP circuits are activated the ACK output is set LOW to indicate that a fault has occurred. The ACK output returns to high impedance state automatically once the fault condition is removed or $\overline{\text{EN}}$ is HIGH.

9. Application diagram

The NX18P3001 typically connects a USB port in a portable, battery operated device. The ACK signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level it is connected to.

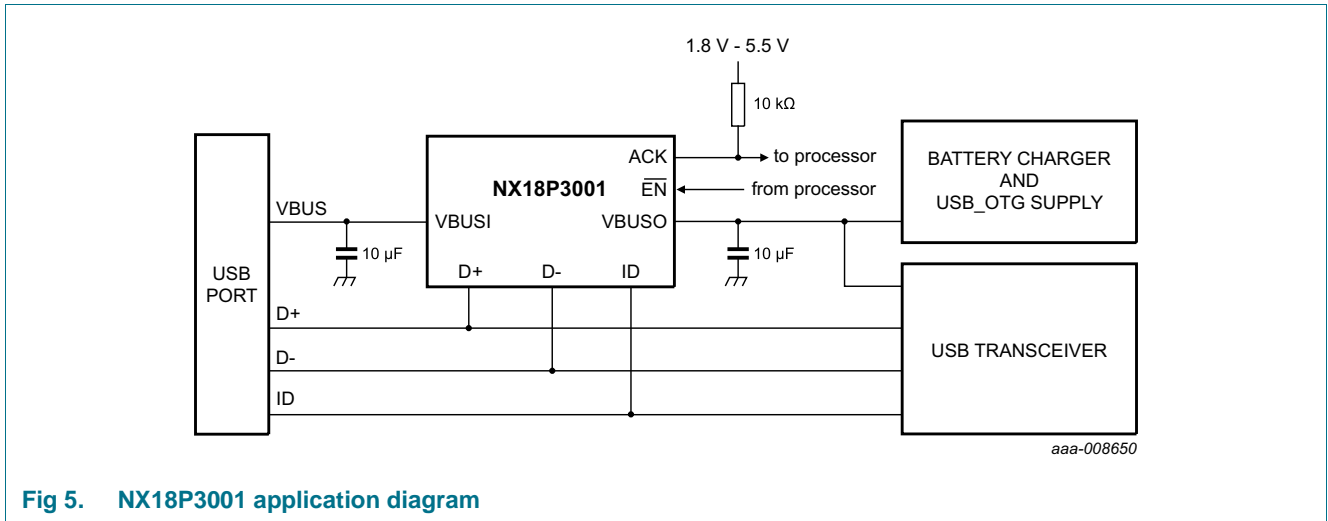


Fig 5. NX18P3001 application diagram

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|------------------------------|---------------------------------------|----------|-------|------|
| V _I | input voltage | VBUSI | [1] -0.5 | +32 | V |
| | | VBUSO | [1] -0.5 | +6.75 | V |
| | | EN | [2] -0.5 | +6.0 | V |
| | | D-, D+, ID | [1] -0.5 | +6.0 | V |
| V _O | output voltage | ACK | -0.5 | +6.0 | V |
| I _{IK} | input clamping current | EN: V _I < -0.5 V | -50 | - | mA |
| I _{SK} | switch clamping current | VBUSI; VBUSO; V _I < -0.5 V | -50 | - | mA |
| I _{SW} | switch current | T _{amb} = 85 °C | - | 3 | A |
| T _{j(max)} | maximum junction temperature | | -40 | +125 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |

Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-------------------------------------|-----|------|------|
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | | | |
| | | WLCSP12 package | [3] | 1.44 | W |

- [1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
 [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
 [3] For WLCSP12 package: P_{tot} derates linearly with 13.7 mW/K above 20 °C.

11. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|----------------------|------------------------|-----|-----|------|
| V _I | input voltage | VBUSI | 3.0 | 30 | V |
| | | VBUSO | 3.0 | 5.5 | V |
| | | $\overline{\text{EN}}$ | 0 | 5.5 | V |
| V _{I/O} | input/output voltage | D-, D+, ID | 0 | 5.5 | V |
| T _{amb} | ambient temperature | | -40 | +85 | °C |

12. Thermal characteristics

Table 7. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|------------|-----------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | | [1][2] 73 | K/W |

- [1] The overall R_{th(j-a)} can vary depending on the board layout. To minimize the effective R_{th(j-a)}, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.
 [2] Please rely on the measurement data given for a rough estimation of the R_{th(j-a)} in your application. The actual R_{th(j-a)} value may vary in applications using different layer stacks and layouts

13. Static characteristics

Table 8. Static characteristics

V_{I(VBUSI)} = 4.0 V to 16.0 V or V_{I(VBUSO)} = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | Unit |
|-----------------|--------------------------|----------------------------|--------------------------|--------------------|-----|-------------------------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | $\overline{\text{EN}}$ | 1.2 | - | - | 1.2 | - | V |
| V _{IL} | LOW-level input voltage | $\overline{\text{EN}}$ | - | - | 0.4 | - | 0.4 | V |
| V _{OL} | LOW-level output voltage | ACK; I _O = 8 mA | - | - | 0.5 | - | 0.5 | V |
| R _{pu} | pull-up resistance | ACK | 10 | - | 200 | 10 | 200 | kΩ |
| V _{pu} | pull-up voltage | ACK | 1.65 | - | 5.5 | 1.65 | 5.5 | V |

Bidirectional power switch for charger and USB-OTG combinations

Table 8. Static characteristics ...continued

$V_{I(VBUSI)} = 4.0\text{ V to }16.0\text{ V}$ or $V_{I(VBUSO)} = 4.0\text{ V to }5.5\text{ V}$; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | Unit |
|------------------------|---|--|--------------------------|--------------------|------|-------------------------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| I _{GND} | ground current | $\overline{\text{EN}} = \text{LOW}$; I _O = 0 A; see Figure 6 to Figure 13 | - | 280 | - | - | 450 | μA |
| | | $\overline{\text{EN}} = \text{HIGH}$; V _{I(VBUSx)} = 5.5 V; ^[2] I _O = 0 A; see Figure 6 to Figure 13 | - | 8 | - | - | 16 | μA |
| | | $\overline{\text{EN}} = \text{HIGH}$; V _{I(VBUSI)} = 16 V; I _O = 0 A; see Figure 6 to Figure 13 | - | 20 | - | - | 33 | μA |
| I _{S(OFF)} | OFF-state leakage current | V _{I(VBUSI)} = 30 V; ^[3] V _{I(VBUSO)} = 0 V to 5 V; see Figure 14 | - | 0.1 | - | - | 6.5 | μA |
| | | V _{I(VBUSO)} = 5.5 V; ^[4] V _{I(VBUSI)} = 0 V to 5 V; see Figure 15 | - | 0.1 | - | - | 8.5 | μA |
| V _{UVLO} | undervoltage lockout voltage | VBUSI; VBUSO; $\overline{\text{EN}} = \text{LOW}$ | 3.0 | 3.2 | 3.4 | 3.0 | 3.4 | V |
| V _{hys(UVLO)} | undervoltage lockout hysteresis voltage | VBUSI; VBUSO; $\overline{\text{EN}} = \text{LOW}$ | - | 100 | - | - | - | mV |
| V _{OVLO} | overvoltage lockout voltage | VBUSI; $\overline{\text{EN}} = \text{LOW}$ | 16.5 | 17.5 | 18.5 | 16.5 | 18.5 | V |
| V _{hys(OVLO)} | overvoltage lockout hysteresis voltage | VBUSI; $\overline{\text{EN}} = \text{LOW}$ | - | 105 | - | - | - | mV |
| C _{I/O} | input/output capacitance | D-; D+; ID; V _{I(VBUSx)} = 5.5 V ^[2] | - | 3 | - | - | - | pF |
| C _I | input capacitance | $\overline{\text{EN}}$ | - | 3 | - | - | - | pF |
| C _{S(ON)} | ON-state capacitance | VBUSI; VBUSO | - | - | 0.5 | - | 0.5 | nF |

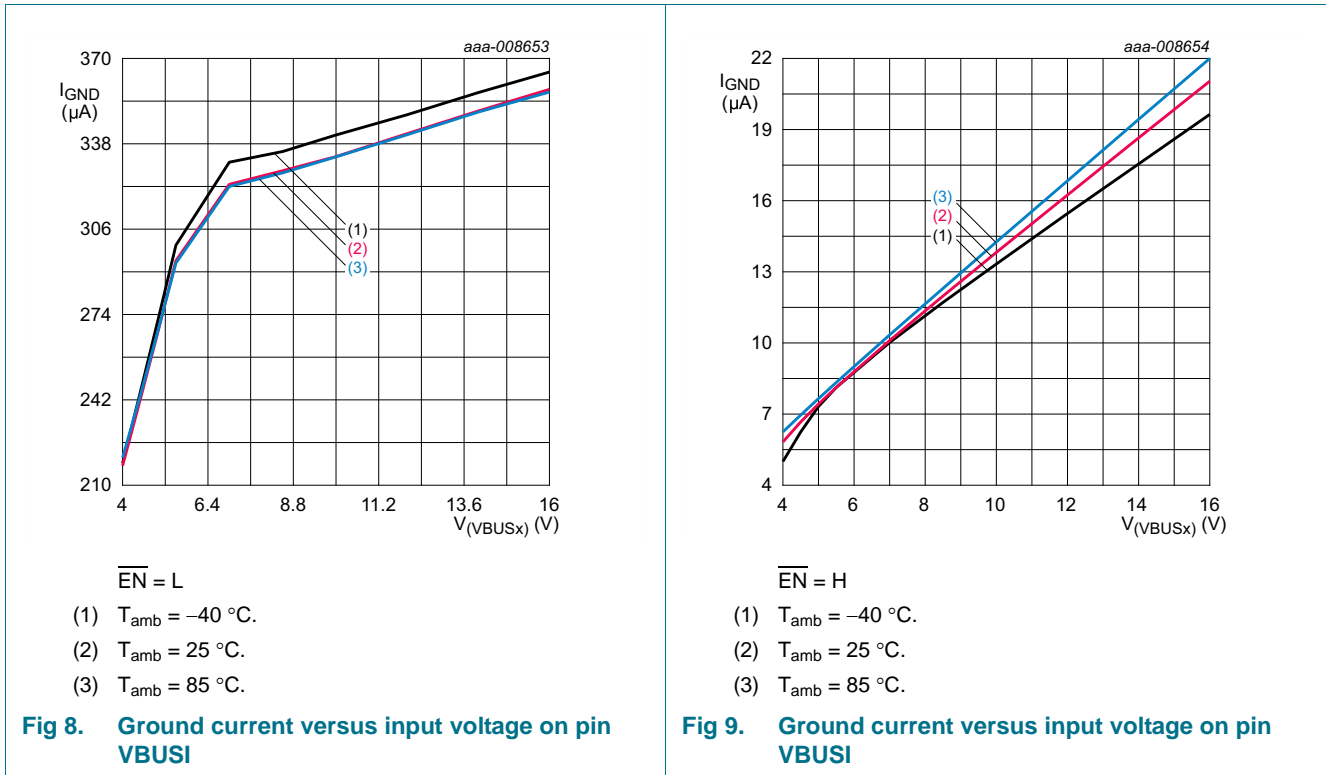
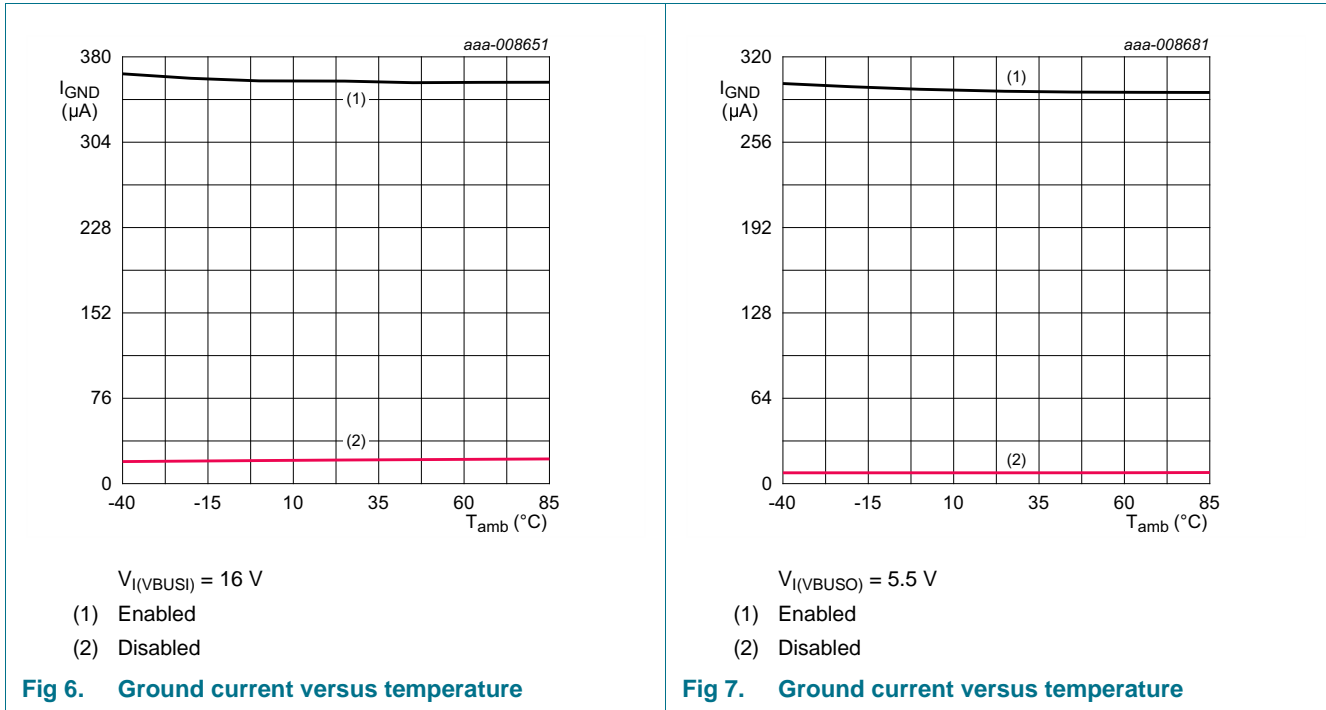
[1] All typical values are measured at V_{I(VBUSx)} = 5.0 V unless otherwise specified.

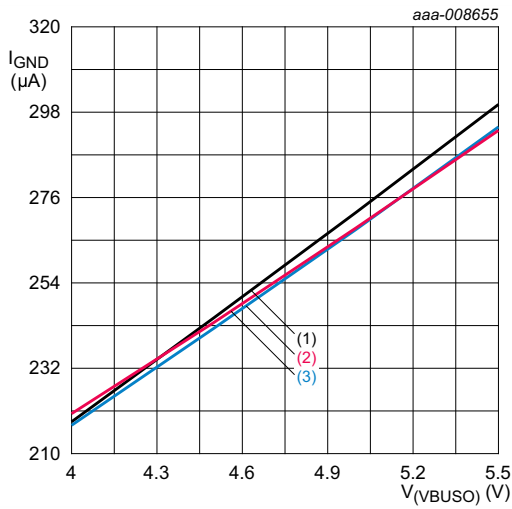
[2] VBUSx is the supply voltage associated with the input, either VBUSI or VBUSO.

[3] Typical value is measured at V_{I(VBUSO)} = 0 V.

[4] Typical value is measured at V_{I(VBUSI)} = 0 V.

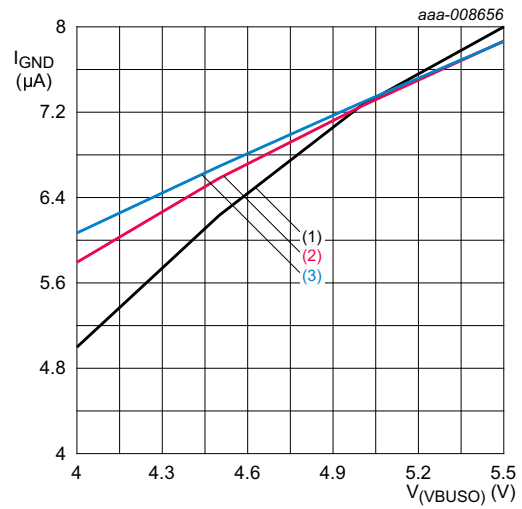
13.1 Graphs





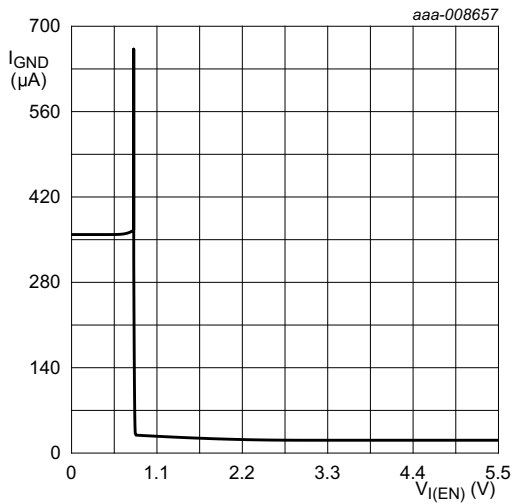
- $\overline{EN} = L$
- (1) $T_{amb} = -40\text{ }^{\circ}\text{C.}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C.}$
 - (3) $T_{amb} = 85\text{ }^{\circ}\text{C.}$

Fig 10. Ground current versus input voltage on pin VBUSO



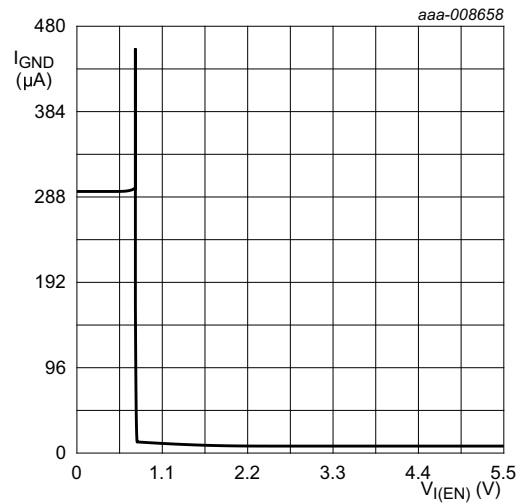
- $\overline{EN} = H$
- (1) $T_{amb} = -40\text{ }^{\circ}\text{C.}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C.}$
 - (3) $T_{amb} = 85\text{ }^{\circ}\text{C.}$

Fig 11. Ground current versus input voltage on pin VBUSO



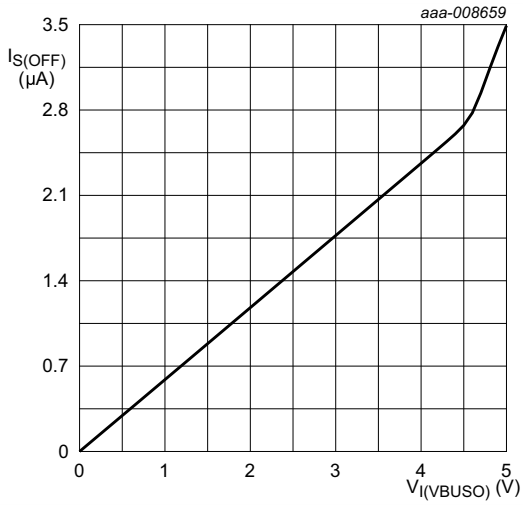
$V_{I(VBUS)} = 16\text{ V}$

Fig 12. Ground current versus input voltage on pin \overline{EN}



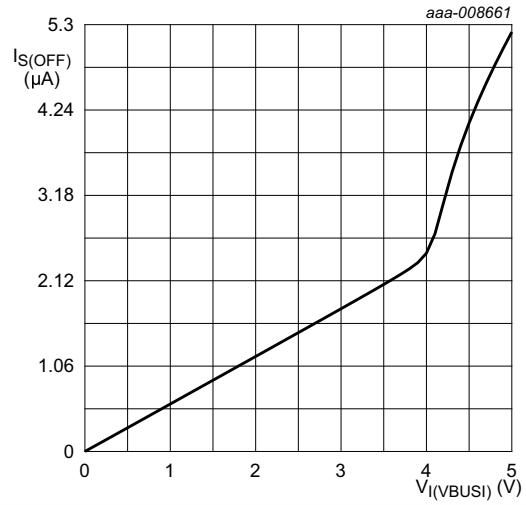
$V_{I(VBUS)} = 5.5\text{ V}$

Fig 13. Ground current versus input voltage on pin \overline{EN}



$V_{I(VBUSI)} = 16\text{ V}$

Fig 14. OFF-state leakage current versus input voltage on pin VBUSO



$V_{I(VBUSO)} = 5.5\text{ V}$

Fig 15. OFF-state leakage current versus input voltage on pin VBUSI

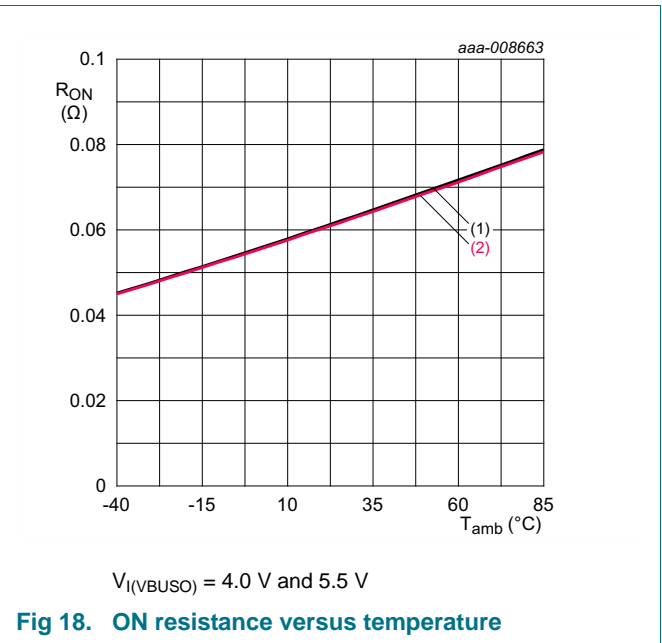
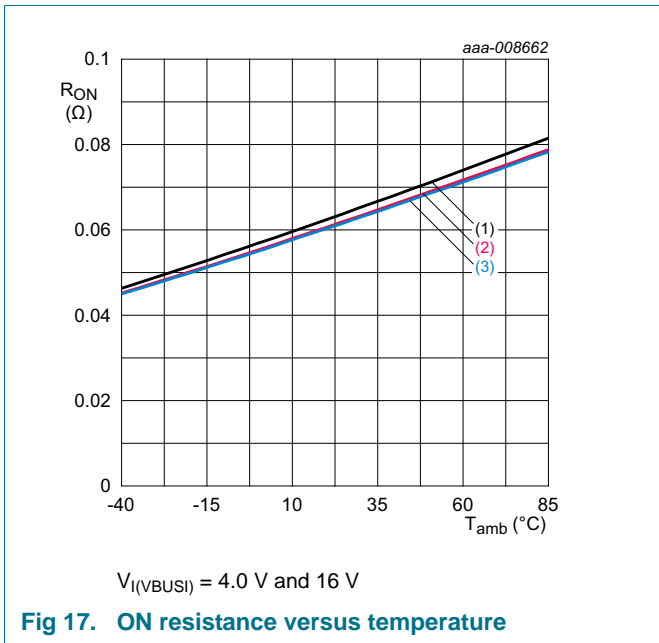
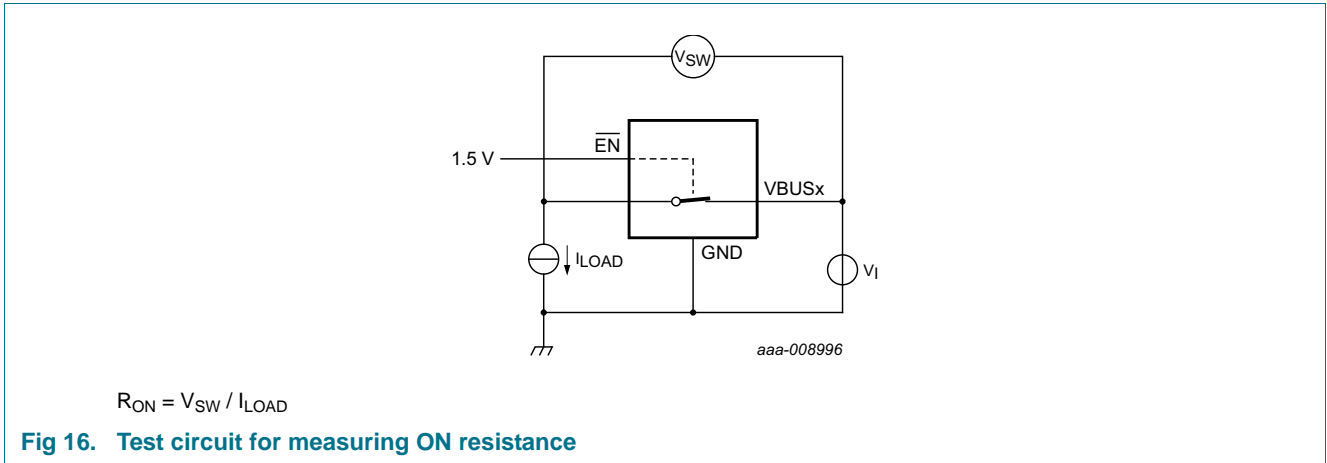
13.2 ON resistance

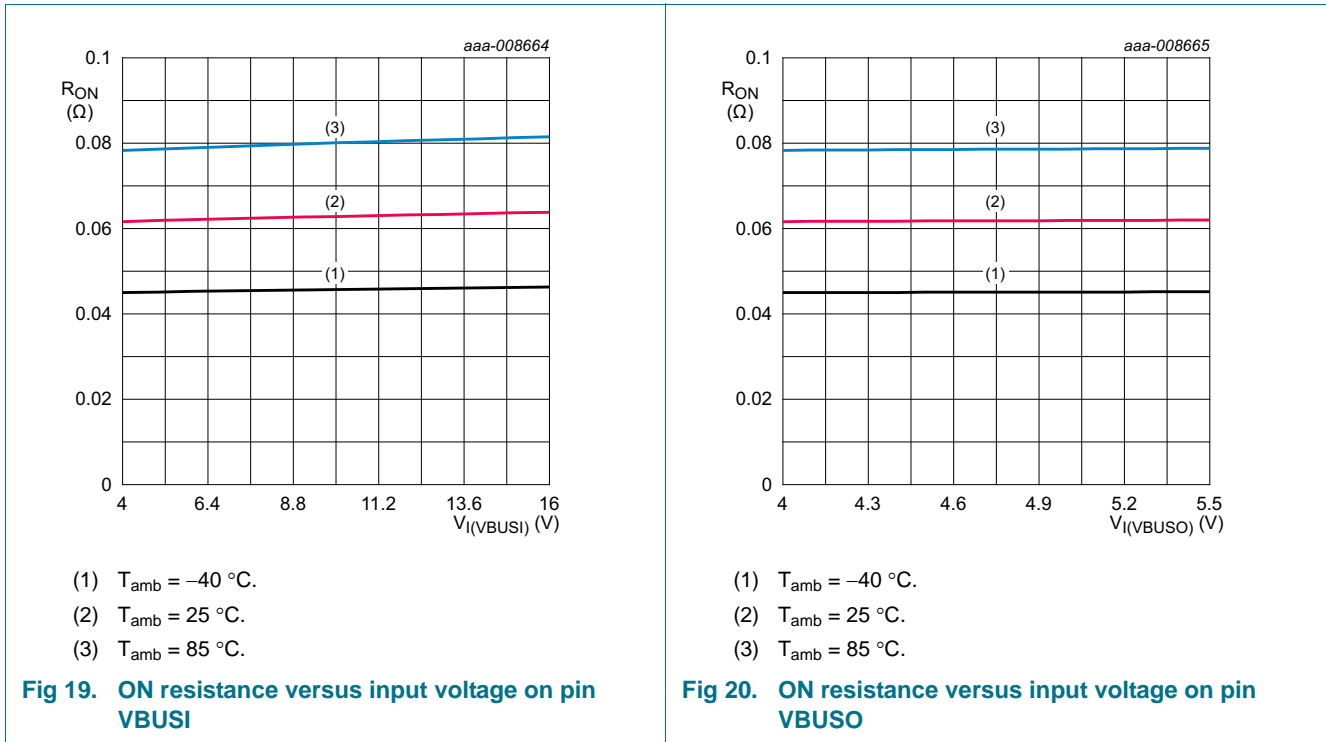
Table 9. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | $T_{amb} = 25\text{ °C}$ | | | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ | | Unit | |
|----------|---------------|--|----------------------------|-----|-----|--|-----|------|-----------|
| | | | Min | Typ | Max | Min | Max | | |
| R_{ON} | ON resistance | $V_{I(VBUSI)} = 4.0\text{ V to }16\text{ V};$ see Figure 16 to Figure 20 | $I_{LOAD} = 200\text{ mA}$ | - | 62 | - | 40 | 100 | $m\Omega$ |
| | | | $I_{LOAD} = 1.5\text{ A}$ | - | 62 | - | 40 | 100 | $m\Omega$ |
| | | $V_{I(VBUSO)} = 4.0\text{ V to }5.5\text{ V};$ see Figure 16 to Figure 20 | $I_{LOAD} = 200\text{ mA}$ | - | 62 | - | 40 | 100 | $m\Omega$ |
| | | | $I_{LOAD} = 1.5\text{ A}$ | - | 62 | - | 40 | 100 | $m\Omega$ |

13.3 ON resistance test circuit and graphs





14. Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 22](#).

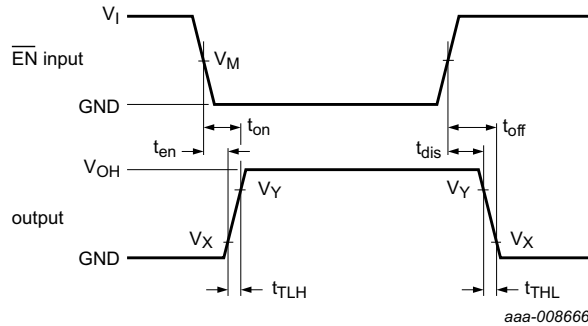
| Symbol | Parameter | Conditions | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | | | $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ | | Unit |
|-----------|--------------|--|--|-----|-----|---|-----|---------------|
| | | | Min | Typ | Max | Min | Max | |
| t_{en} | enable time | \overline{EN} to VBUSO; see Figure 21 and Figure 23 to Figure 26 | | | | | | |
| | | $V_{I(VBUSI)} = 4.0\text{ V}$ | - | 500 | - | 210 | - | μs |
| | | $V_{I(VBUSI)} = 16\text{ V}$ | - | 500 | - | 250 | - | μs |
| | | \overline{EN} to VBUSI; see Figure 21 and Figure 23 to Figure 26 | | | | | | |
| | | $V_{I(VBUSO)} = 4.0\text{ V}$ | - | 500 | - | 310 | - | μs |
| | | $V_{I(VBUSO)} = 5.5\text{ V}$ | - | 500 | - | 290 | - | μs |
| t_{dis} | disable time | \overline{EN} to VBUSO; see Figure 21 and Figure 27 to Figure 30 | | | | | | |
| | | $V_{I(VBUSI)} = 4.0\text{ V}$ | - | 1.6 | - | - | - | ms |
| | | $V_{I(VBUSI)} = 16\text{ V}$ | - | 1.6 | - | - | - | ms |
| | | \overline{EN} to VBUSI; see Figure 21 and Figure 27 to Figure 30 | | | | | | |
| | | $V_{I(VBUSO)} = 4.0\text{ V}$ | - | 1.6 | - | - | - | ms |
| | | $V_{I(VBUSO)} = 5.5\text{ V}$ | - | 1.6 | - | - | - | ms |

Bidirectional power switch for charger and USB-OTG combinations

Table 10. Dynamic characteristics ...continuedAt recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 22](#).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | Unit |
|------------------|------------------------------------|---|--------------------------|------|-----|-------------------------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{on} | turn-on time | \overline{EN} to VBUS0; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 1500 | - | 880 | - | μs |
| | | V _{I(VBUS0)} = 16 V | - | 2000 | - | 1130 | - | μs |
| | | \overline{EN} to VBUS1; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 1500 | - | 820 | - | μs |
| t _{off} | turn-off time | \overline{EN} to VBUS0; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 34.6 | - | - | - | ms |
| | | V _{I(VBUS0)} = 16 V | - | 34.6 | - | - | - | ms |
| | | \overline{EN} to VBUS1; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 34.6 | - | - | - | ms |
| t _{TLH} | LOW to HIGH output transition time | VBUS0; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 1000 | - | 670 | - | μs |
| | | V _{I(VBUS0)} = 16 V | - | 1500 | - | 880 | - | μs |
| | | VBUS1; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 1000 | - | 510 | - | μs |
| t _{THL} | HIGH to LOW output transition time | VBUS0; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 33.0 | - | - | - | ms |
| | | V _{I(VBUS0)} = 16 V | - | 33.0 | - | - | - | ms |
| | | VBUS1; see Figure 21 | | | | | | |
| | | V _{I(VBUS0)} = 4.0 V | - | 33.0 | - | - | - | ms |
| | | V _{I(VBUS0)} = 5.5 V | - | 33.0 | - | - | - | ms |

14.1 Waveforms and test circuit

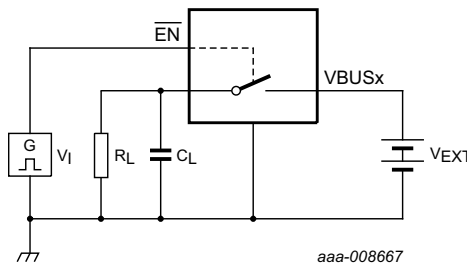


Measurement points are given in [Table 11](#).
 Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 21. Switching times

Table 11. Measurement points

| Supply voltage V_I | | EN Input | Output | |
|----------------------|----------------|------------------------|---------------------|---------------------|
| VBUSI | VBUSO | V_M | V_X | V_Y |
| 4.0 V to 16 V | 4.0 V to 5.5 V | $0.5 \times V_{I(EN)}$ | $0.1 \times V_{OH}$ | $0.9 \times V_{OH}$ |

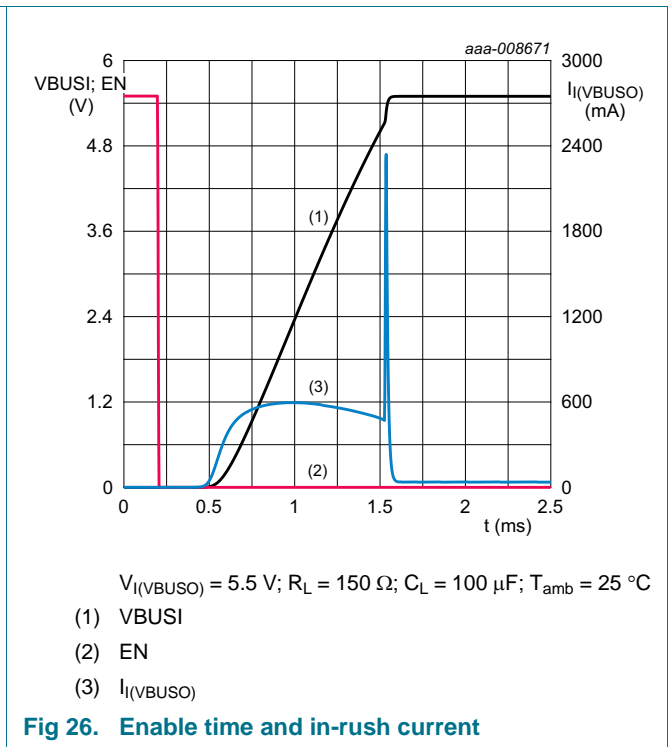
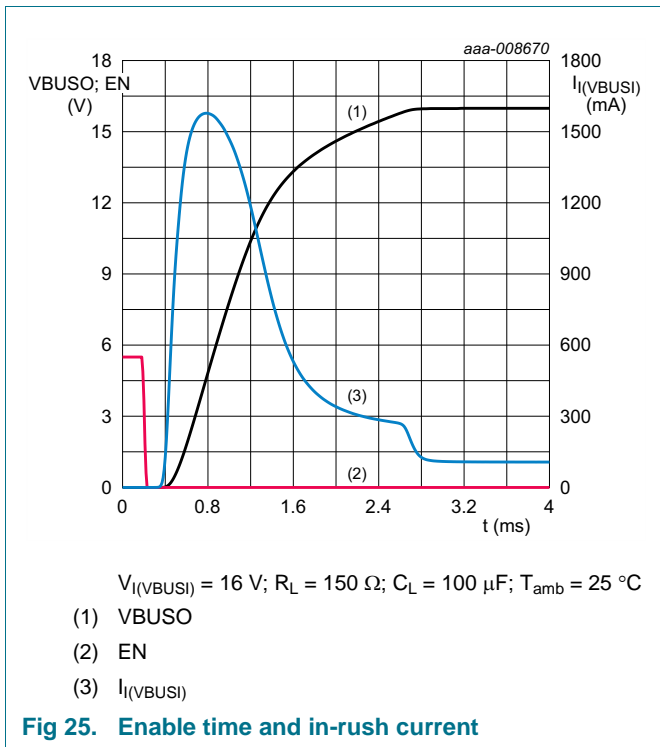
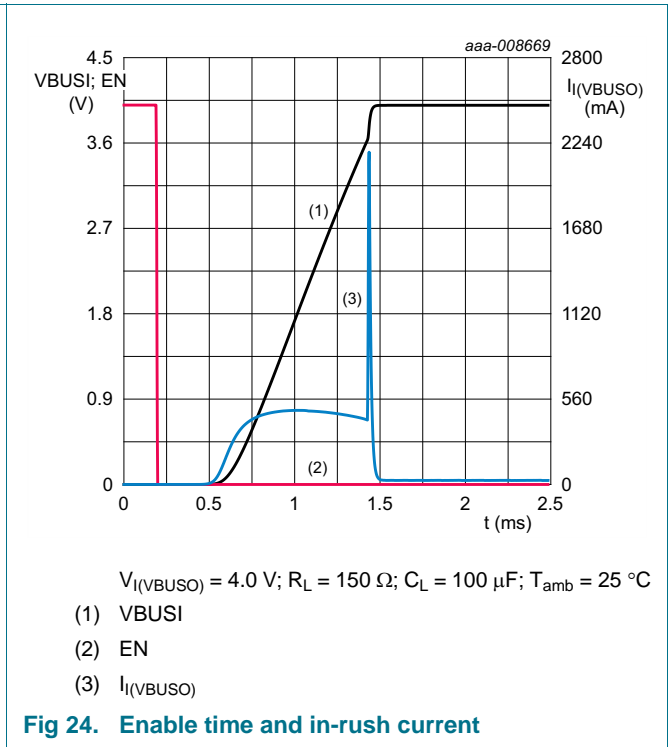
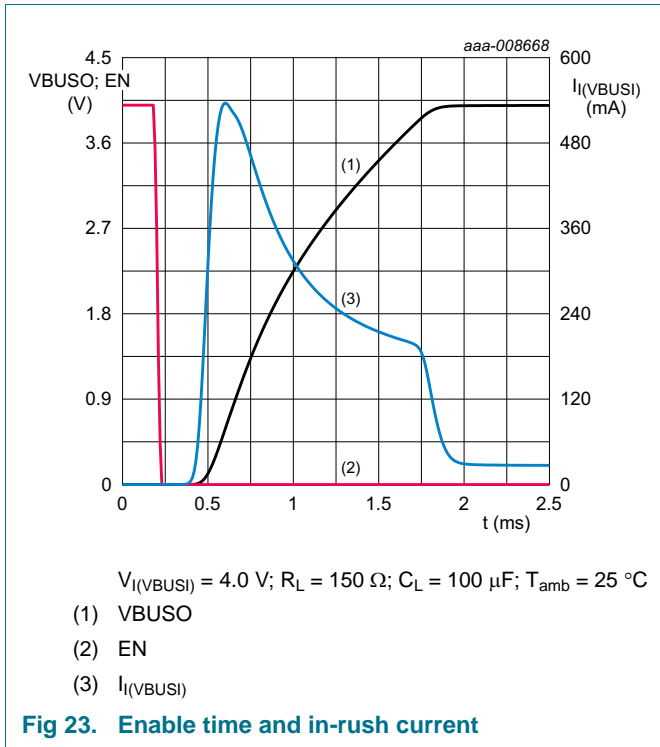


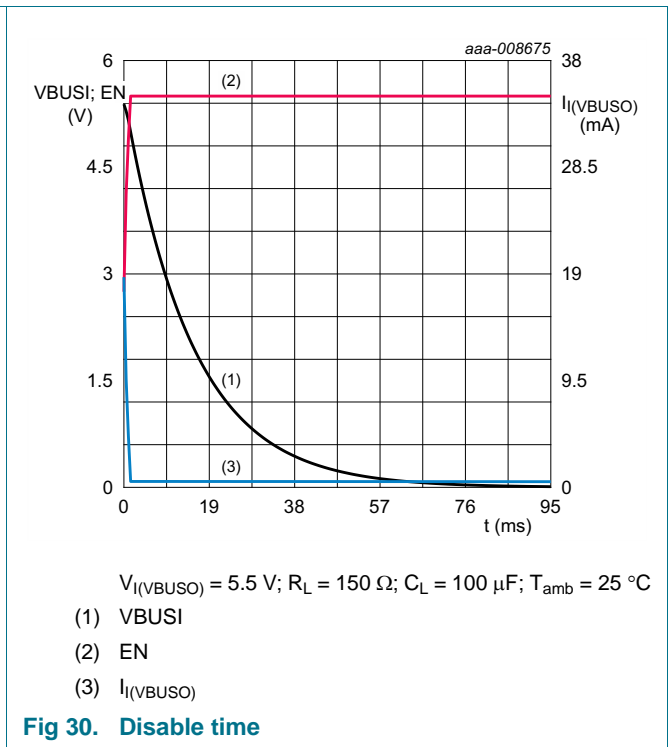
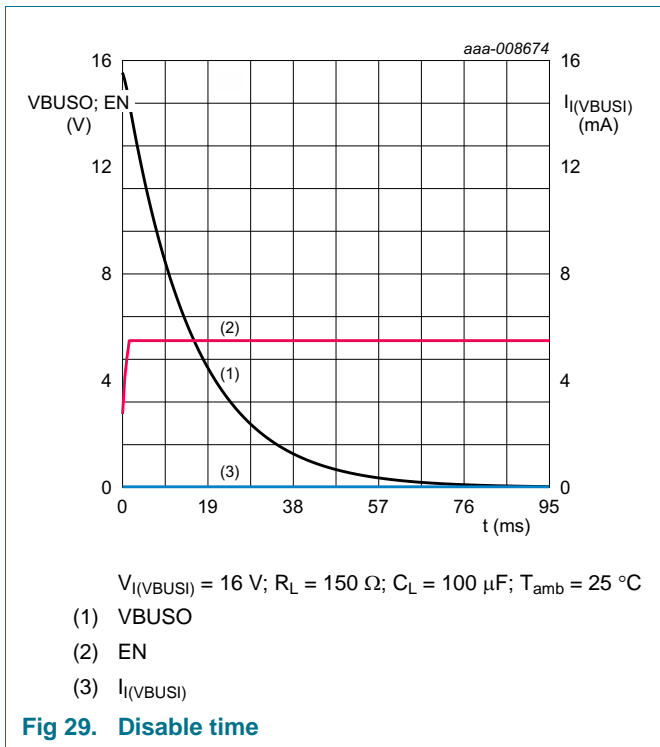
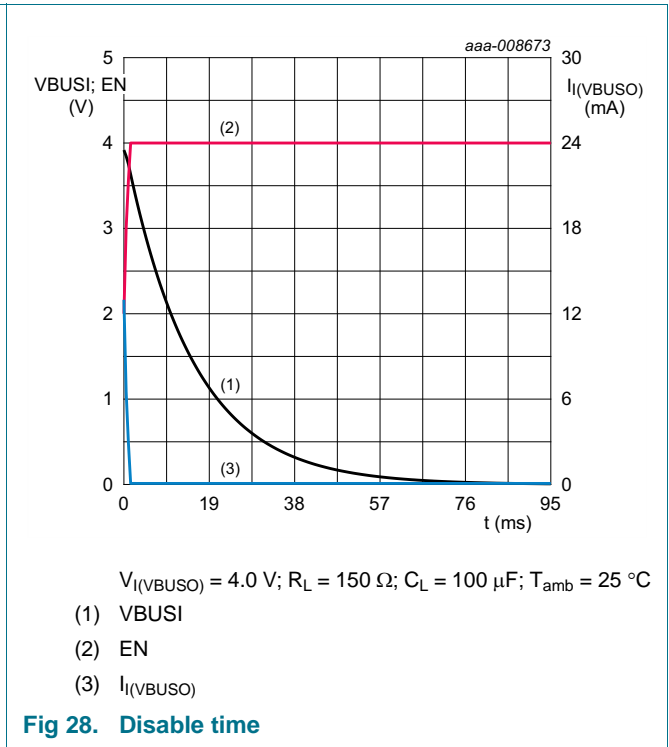
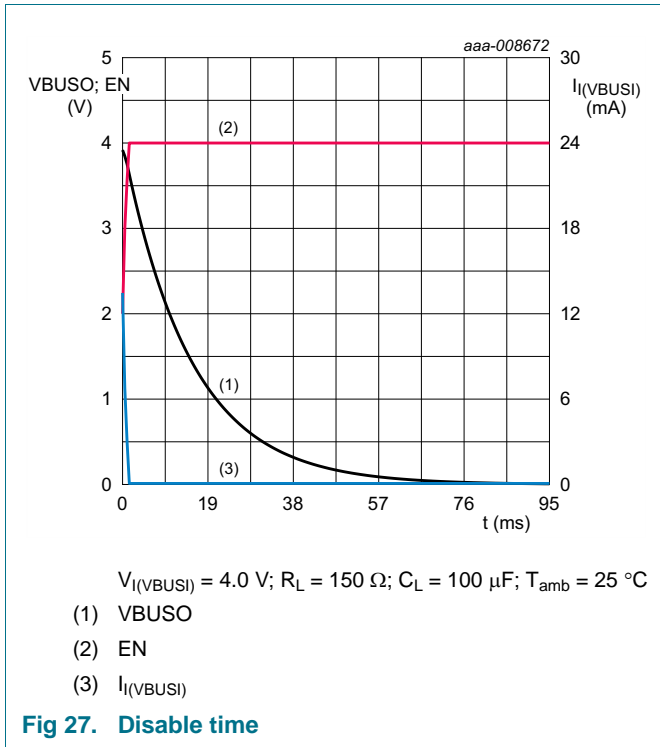
Test data is given in [Table 12](#).
 Definitions test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 V_{EXT} = External voltage for measuring switching times.

Fig 22. Test circuit for measuring switching times

Table 12. Test data

| Supply voltage V_{EXT} | | Input | Load | |
|--------------------------|----------------|-------|-------------|--------------|
| VBUSI | VBUSO | V_I | C_L | R_L |
| 4.0 V to 16 V | 4.0 V to 5.5 V | 1.5 V | 100 μF | 150 Ω |





15. Package outline

WLCSP12: wafer level chip-scale package;
12 bumps; 1.36 x 1.66 x 0.51 mm, 0.4 mm pitch (Backside coating included)

NX18P3001

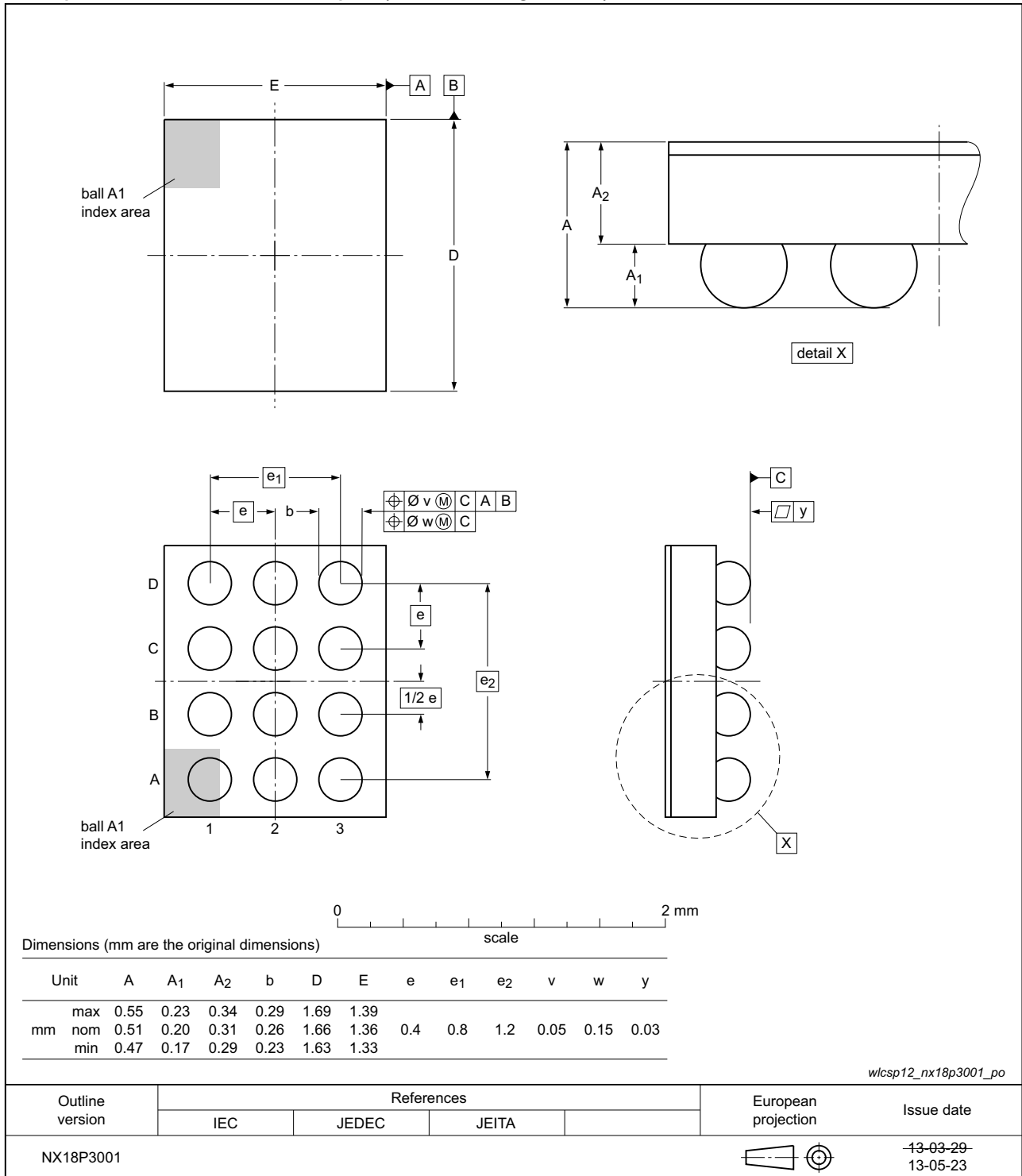


Fig 31. Package outline WLCSP12 package

16. Abbreviations

Table 13. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MOSFET | Metal-Oxide Semiconductor Field Effect Transistor |
| OTP | OverTemperature Protection |
| USB-OTG | Universal Serial Bus On-The-Go |
| UVLO | UnderVoltage LockOut |
| OVLO | OverVoltage LockOut |

17. Revision history

Table 14. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| NX18P3001 v.1 | 20130924 | Product data sheet | - | - |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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