

NTD5807N, NVD5807N

Power MOSFET

40 V, 23 A, Single N-Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable – NVD5807N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- CCFL Backlight
- DC Motor Control
- Class D Amplifier
- Power Supply Secondary Side Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DS}	40	V		
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V		
Gate-to-Source Voltage – Non-Repetitive ($t_p < 10 \mu\text{s}$)	V_{GS}	± 30	V		
Continuous Drain Current ($R_{\theta JC}$) (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D	23	A
		$T_C = 100^\circ\text{C}$		16	
Power Dissipation ($R_{\theta JC}$) (Note 1)		$T_C = 25^\circ\text{C}$	P_D	33	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	45	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$	
Source Current (Body Diode)	I_S	23	A		
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega, I_{L(pk)} = 14 \text{ A}, L = 0.3 \text{ mH}, V_{DS} = 40 \text{ V}$)	E_{AS}	29.4	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	107	

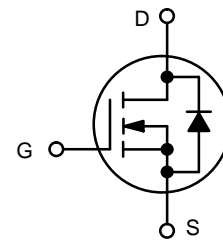
1. Surface-mounted on FR4 board using the minimum recommended pad size.



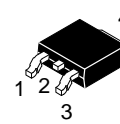
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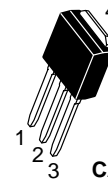
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	37 m Ω @ 4.5 V	16 A
	31 m Ω @ 10 V	23 A



N-CHANNEL MOSFET

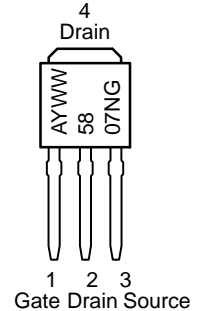
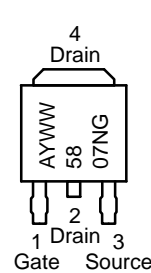


DPAK
CASE 369AA
(Surface Mount)
STYLE 2



IPAK
CASE 369D
(Straight Lead
DPAK)

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5807N = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			38		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		1.0	μA
			T _J = 150°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.4		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-5.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 5.0 A		20	31	mΩ
		V _{GS} = 4.5 V, I _D = 4.0 A		29	37	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 15 A		8.1		S

CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		603		pF
Output Capacitance	C _{oss}			96		
Reverse Transfer Capacitance	C _{riss}			73		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 20 V, I _D = 5.0 A		12.6	20	nC
Threshold Gate Charge	Q _{G(TH)}			0.76		
Gate-to-Source Charge	Q _{GS}			2.2		
Gate-to-Drain Charge	Q _{GD}			3.1		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DD} = 20 V, I _D = 30 A, R _G = 2.5 Ω		11.2		ns
Rise Time	t _r			111		
Turn-Off Delay Time	t _{d(off)}			11.2		
Fall Time	t _f			3.2		
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 20 V, I _D = 30 A, R _G = 2.5 Ω		6.7		ns
Rise Time	t _r			20.4		
Turn-Off Delay Time	t _{d(off)}			15.6		
Fall Time	t _f			2.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		0.91	1.2	V
			T _J = 150°C		0.76		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		15.7		ns	
Charge Time	t _a			10.75			
Discharge Time	t _b			5.0			
Reverse Recovery Charge	Q _{RR}			6.1			

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CHARACTERISTICS

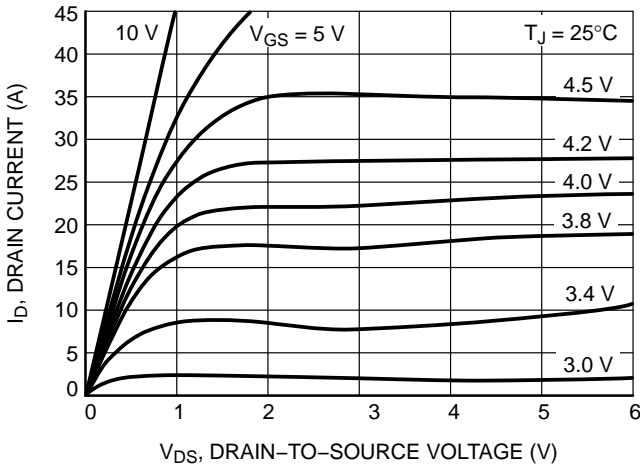


Figure 1. On-Region Characteristics

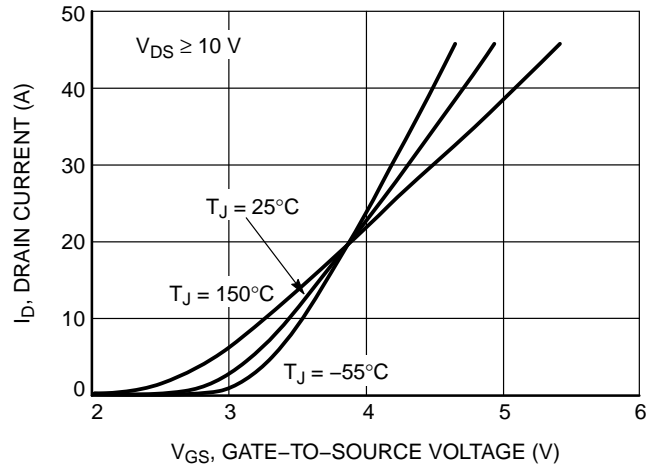


Figure 2. Transfer Characteristics

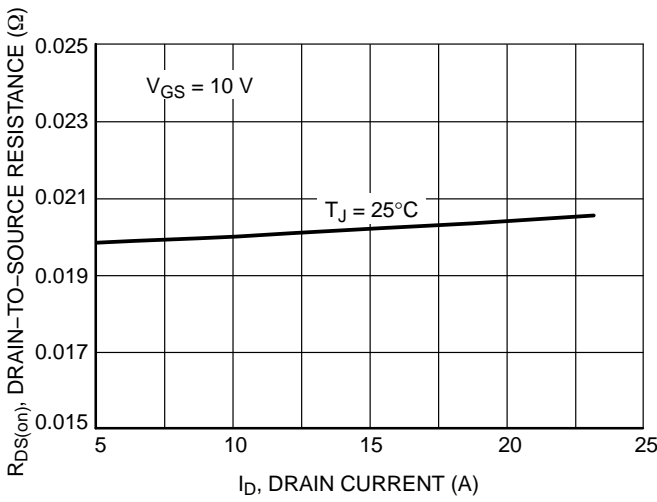


Figure 3. On-Resistance vs. Drain Current

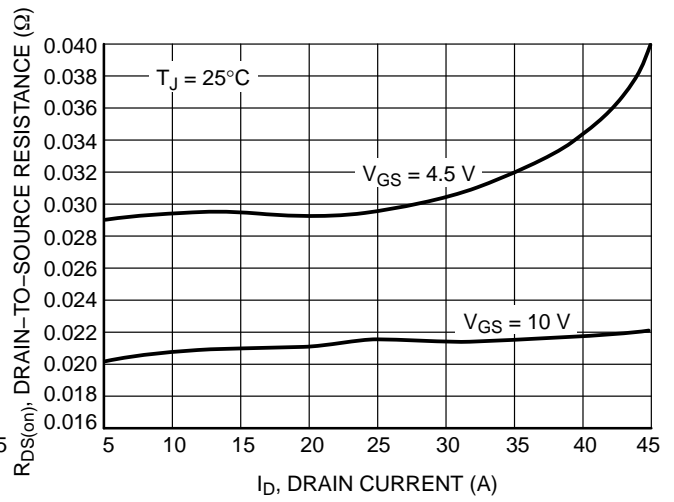


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

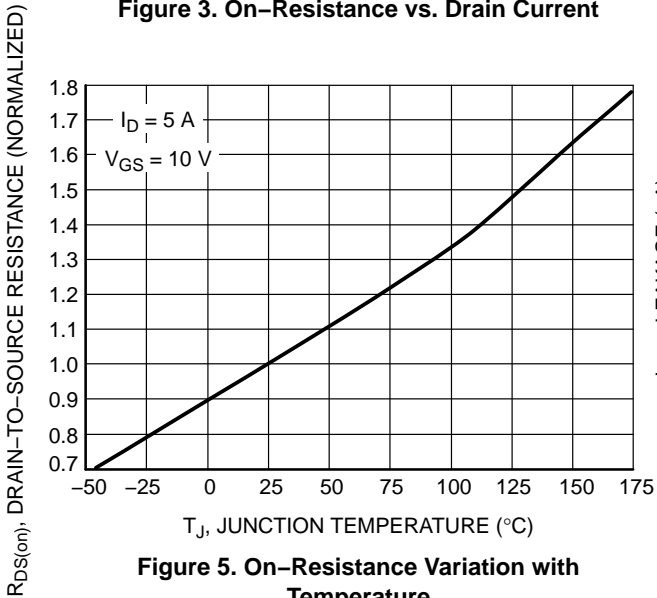


Figure 5. On-Resistance Variation with Temperature

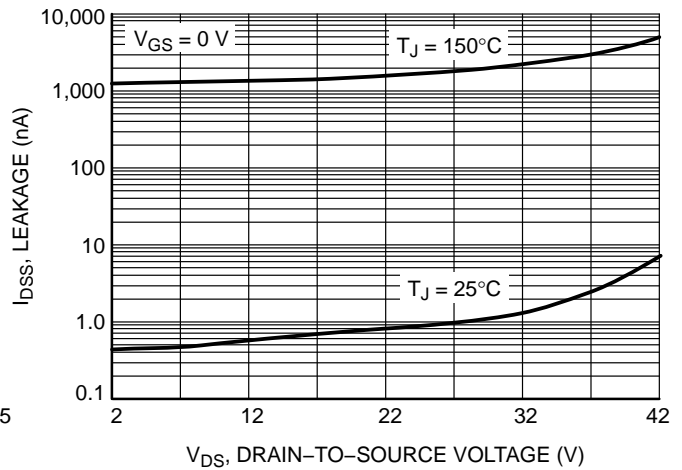


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS

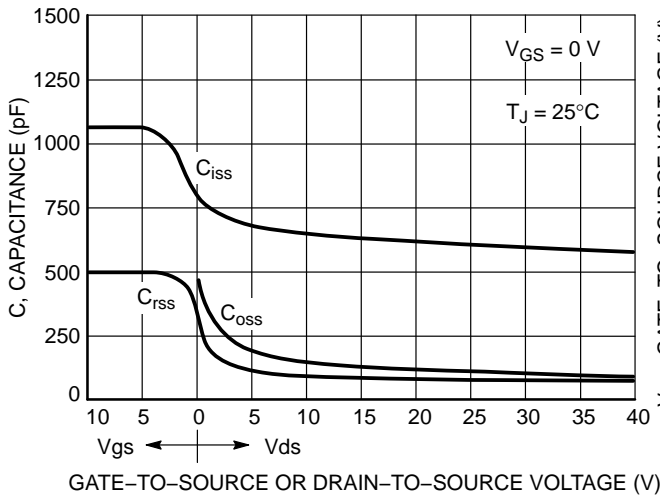


Figure 7. Capacitance Variation

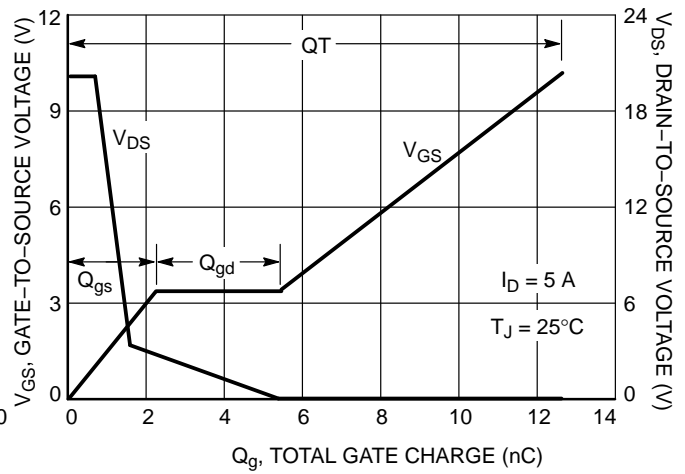


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

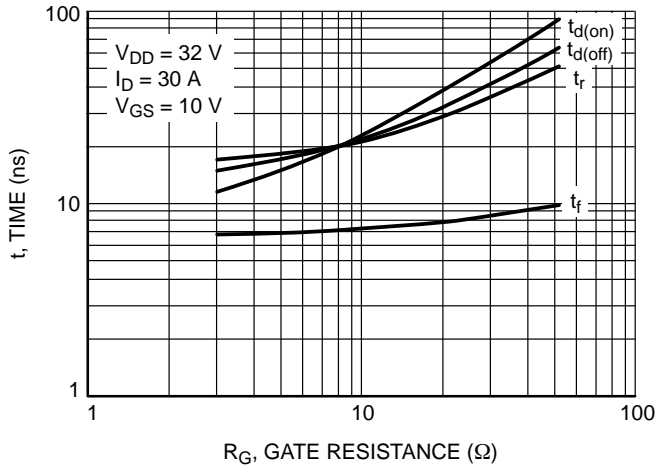


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

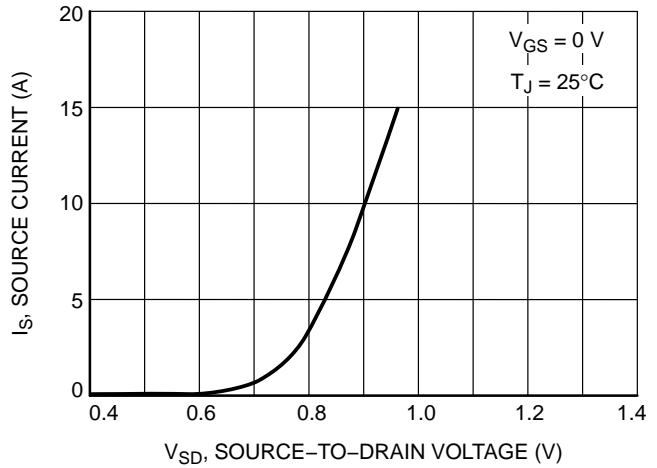


Figure 10. Diode Forward Voltage vs. Current

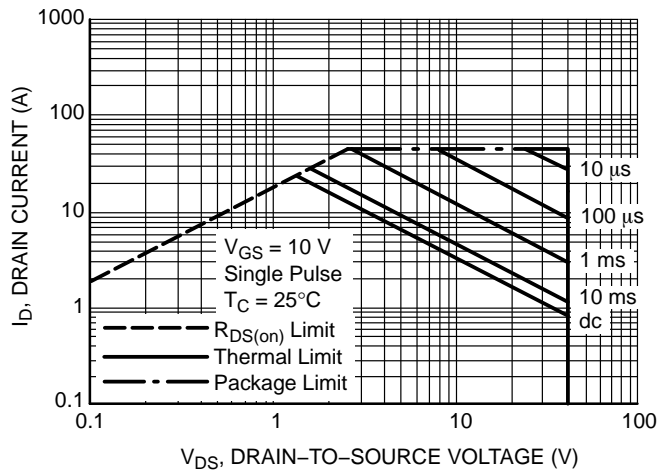


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL PERFORMANCE CHARACTERISTICS

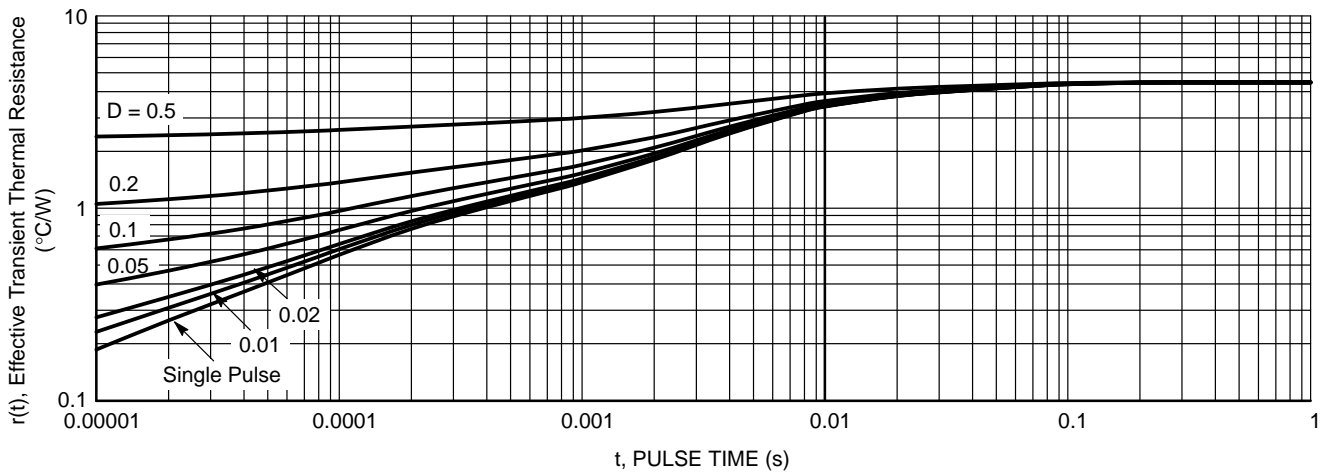


Figure 12. Thermal Response

ORDERING INFORMATION

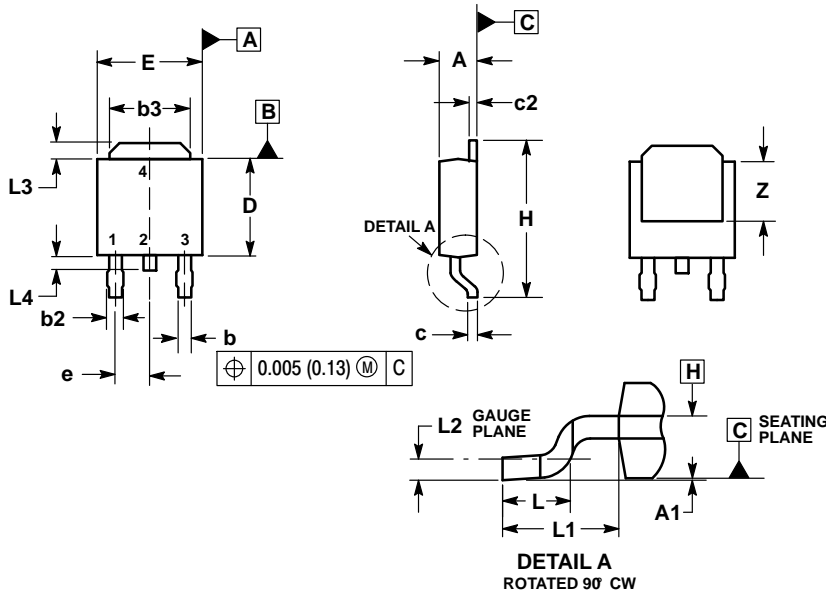
Order Number	Package	Shipping†
NTD5807NG	IPAK (Straight Lead DPAK) (Pb-Free)	75 Units / Rail
NTD5807NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5807NT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD5807N, NVD5807N

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369AA-01 ISSUE B

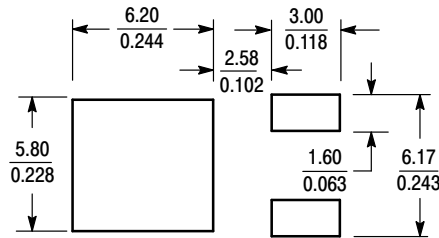


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 ($\frac{\text{mm}}{\text{inches}}$)

STYLE 2:

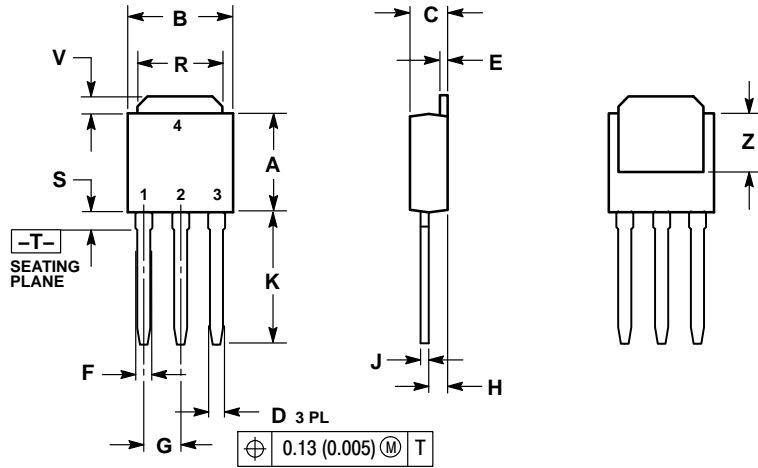
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

IPAK CASE 369D-01 ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	—	3.93	—

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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