

2.5V Drive Nch+SBD MOS FET

QS5U12

●Structure

Silicon N-channel MOSFET
Schottky Barrier DIODE

●Features

- 1) The QS5U12 combines Nch MOSFET with a Schottky barrier diode in a single TSMT5 package.
- 2) Low on-state resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) The Independently connected Schottky barrier diode has low forward voltage.

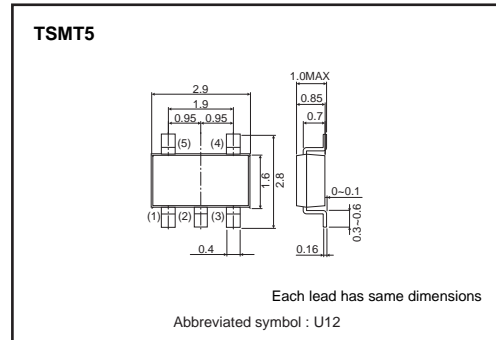
●Applications

Load switch, DC / DC conversion

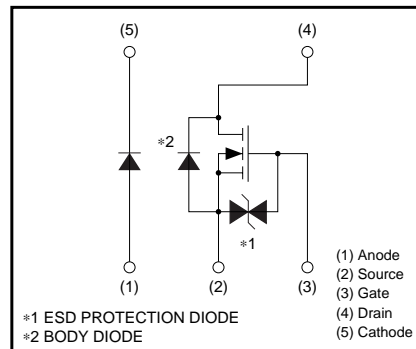
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS5U12		○

●External dimensions (Unit : mm)



●Equivalent circuit



Transistors

●Absolute maximum ratings (Ta=25°C)

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Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	30	V	
Gate-source voltage	V _{GSS}	12	V	
Drain current	Continuous	I _D	±2.0	A
	Pulsed	I _{DP} *1	±8.0	A
Source current (Body diode)	Continuous	I _S	0.8	A
	Pulsed	I _{SP} *1	3.2	A
Channel temperature	T _{ch}	150	°C	
Power dissipation	P _D *3	0.9	W/ELEMENT	

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Repetitive peak reverse voltage	V _{RM}	25	V
Reverse voltage	V _R	20	V
Forward current	I _F	1.0	A
Forward current surge peak	I _{FSM} *2	3.0	A
Junction temperature	T _j	150	°C
Power dissipation	P _D *3	0.7	W/ELEMENT

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Total power dissipation	P _D *3	1.25	W / TOTAL
Range of Storage temperature	T _{stg}	-55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1% *2 60Hz·1cyc. *3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	10	μA	V _{GS} =12V / V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	30	–	–	V	I _D =1mA, / V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	1	μA	V _{DS} =30V / V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	0.5	–	1.5	V	V _{DS} =10V / I _D =1mA
Static drain-source on-state resistance	R _{DS(on)} *	–	71	100	mΩ	I _D =2.0A, V _{GS} =4.5V
		–	76	107	mΩ	I _D =2.0A, V _{GS} =4V
		–	110	154	mΩ	I _D =2.0A, V _{GS} =2.5V
Forward transfer admittance	Y _{fs} *	1.5	–	–	S	V _{DS} =10V, I _D =2.0A
Input capacitance	C _{iss}	–	175	–	pF	V _{DS} =10V
Output capacitance	C _{oss}	–	50	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{riss}	–	25	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	–	8	–	ns	I _D =1.0A
Rise time	t _r *	–	10	–	ns	V _{DD} ≐15V
Turn-off delay time	t _{d(off)} *	–	21	–	ns	V _{GS} =4.5V
Fall time	t _f *	–	8	–	ns	R _L =15Ω
Total gate charge	Q _g *	–	2.8	3.9	nC	R _G =10Ω
Gate-source charge	Q _{gs} *	–	0.6	–	nC	V _{DD} ≐15V
Gate-drain charge	Q _{gd} *	–	0.8	–	nC	V _{GS} =4.5V
						I _D =2.0A

*Pulsed

<Body diode (source-drain)>

Forward voltage	V _{SD} *	–	–	1.2	V	I _S =3.2A / V _{GS} =0V
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* Pulsed

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Forward voltage	V _F	–	–	0.45	V	I _F =1.0A
Reverse current	I _R	–	–	200	μA	V _R =20V

Transistors

●Electrical characteristic curves

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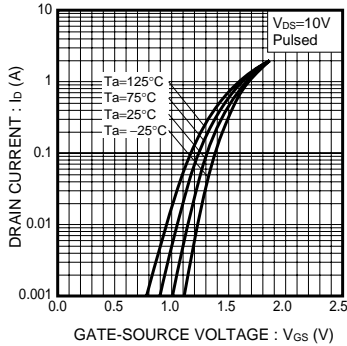


Fig.1 Typical Transfer Characteristics

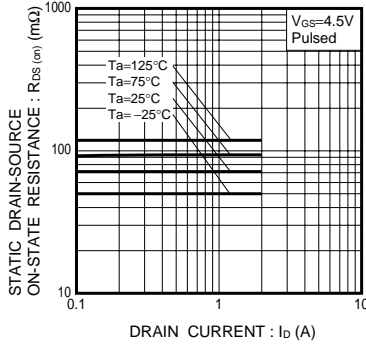


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

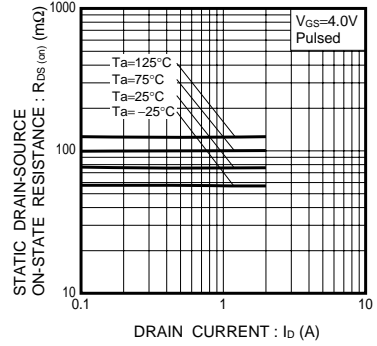


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

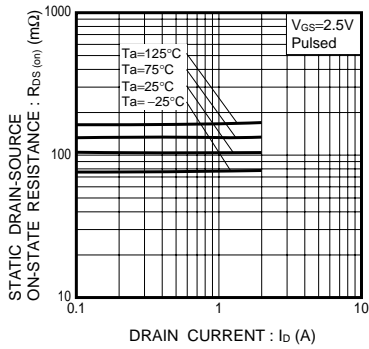


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

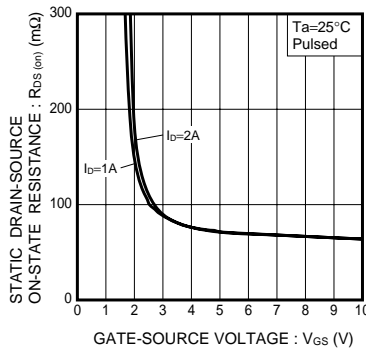


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

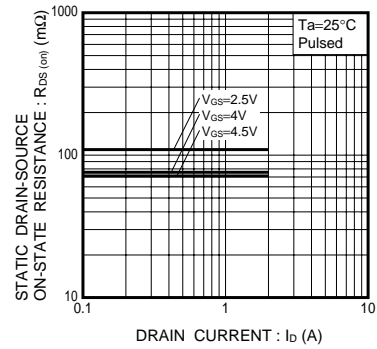


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

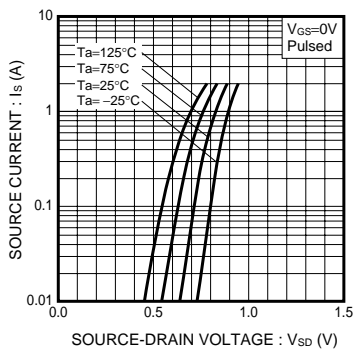


Fig.7 Reverse Drain Current vs. Source-Drain Current

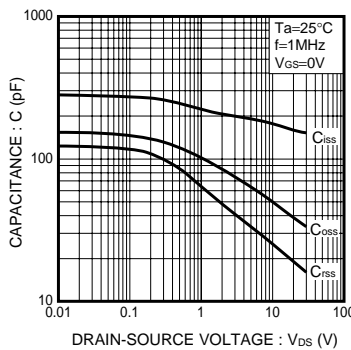


Fig.8 Typical Capacitance vs. Drain-Source Voltage

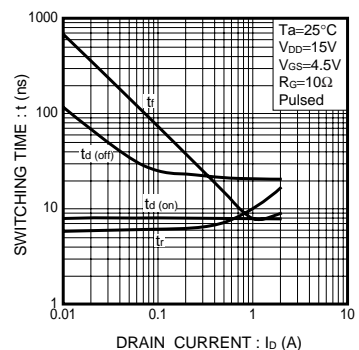


Fig.9 Switching Characteristics

Transistors

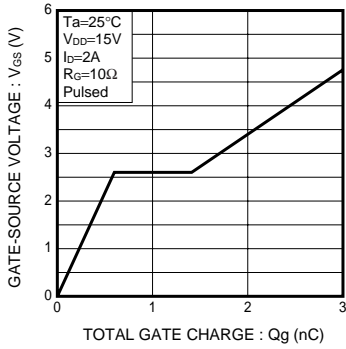


Fig.10 Dynamic Input Characteristics

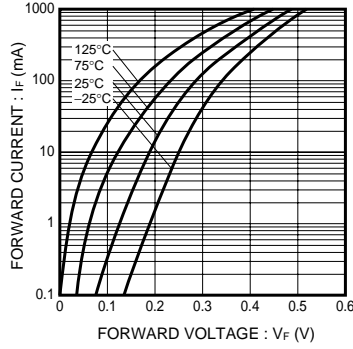


Fig.11 Forward Current vs. Forward Voltage

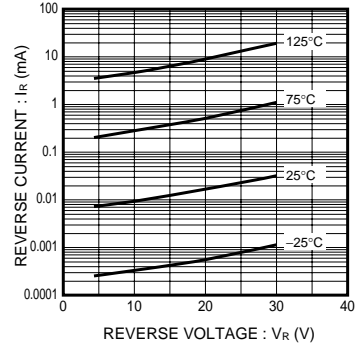


Fig.12 Reverse Current vs. Reverse Voltage

●Measurement circuits

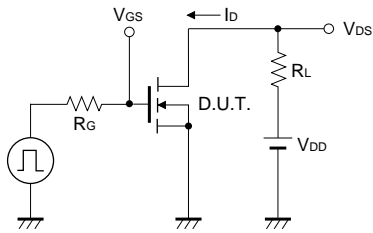


Fig.13 Switching Time Measurement Circuit

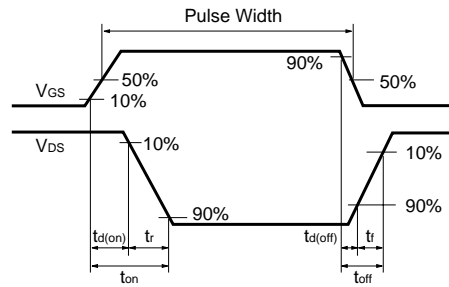


Fig.14 Switching Waveforms

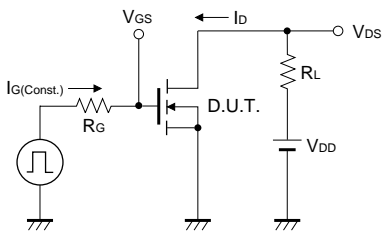


Fig.15 Gate Charge Measurement Circuit

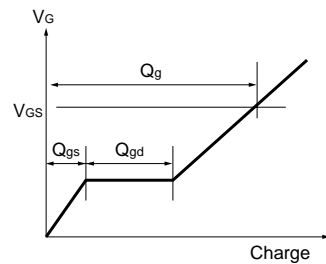


Fig.16 Gate Charge Waveform

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