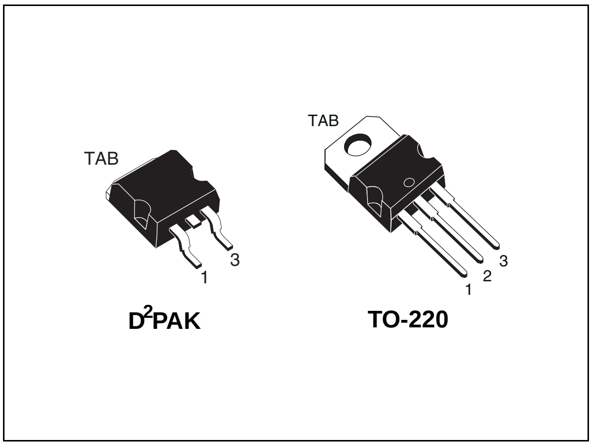
STB100NF04, STP100NF04

N-channel 40 V, 0.0043 Ω typ., 120 A STripFET™ II Power MOSFET in D^{2}PAK and TO-220 packages

Datasheet — production data



Features

Order codes	V_{DS}	$R_{DS(on)}$	I_D	Pw
STP100NF04	40 V	0.0046 Ω	120 A	300 W
STB100NF04	40 V	0.0046 Ω	120 A	300 W

- Standard threshold drive
- 100% avalanche tested

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and with low gate charge driving requirements.

Figure 1. Internal schematic diagram

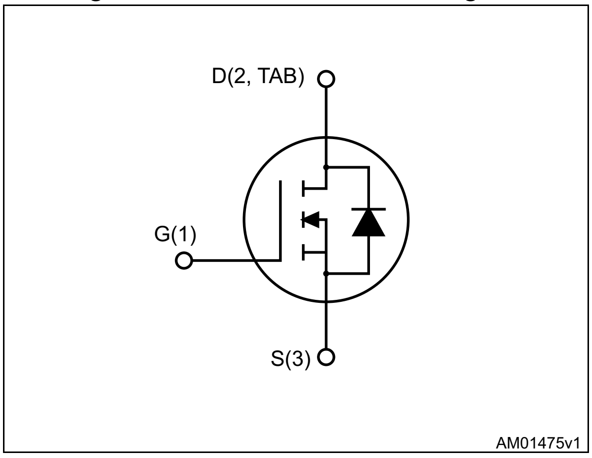


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB100NF04	B100NF04	D²PAK	Tape and reel
STP100NF04	P100NF04	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain-current (continuous) at Tc=25°C	120	A
I_D (1)	Drain-current (continuous) at Tc=100°C	120	A
I_{DM} (2)	Drain-current (pulsed)	480	A
P_{TOT}	Total dissipation at Tc=25°C	300	W
	Derating factor	2	W/°C
dv/dt(3)	Peak diode recovery voltage slope	6	V/ns
E_{AS} (4)	Single pulse avalanche energy	1.2	J
T_j	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Current limited by package
2. Pulse width limited by safe operating area.
3. I_{SD} ≤120A, di/dt ≤300A/µs, $V_{DD} \leq V_{(BR)DSS}$, Tj ≤ Tjmax
4. Starting Tj=25°C, I_D=60A, V_{DD}=30V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance Junction-case max	0.5	°C/W
$R_{thj-pcb}$	Thermal resistance Junction-pcb max	(see *Figure 14*)	°C/W
$R_{thj-amb}$	Thermal resistance Junction-ambient (Free Air) max	62.5	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D=250µA, V_{GS}=0	40			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS}=0)	V_{DS}=40 V V_{DS}=40 V, Tc=125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS}=0)	V_{GS}=±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=$V_{GS,}$ I_D=250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-Resistance	V_{GS}=10 V, I_D=50 A		0.0043	0.0046	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}=25 V, f=1 MHz,V_{GS}=0	-	5100		pF
C_{oss}	Output capacitance		-	1300		pF
C_{rss}	Reverse transfer capacitance		-	160		pF
Q_g	Total gate charge	V_{DD}=32 V, I_D=120 A V_{GS}=10 V	-	110	150	nC
Q_{gs}	Gate-source charge		-	35		nC
Q_{gd}	Gate-drain charge		-	70		nC
$t_{d(on)}$	Turn-on delay time	V_{DD}=20 V, I_D=60 A R_G=4.7 Ω, V_{GS}=10 V (see *Figure 22*)	-	35		ns
t_r	Rise time		-	220		ns
$t_{d(off)}$	Turn-off delay time		-	80		ns
t_f	Fall time		-	50		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM} (1)	Source-drain current (pulsed)		-		480	A
V_{SD} (2)	Forward on voltage	I_{SD}=120 A, V_{GS}=0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD}=120 A, V_{DD}=20 V, di/dt=100 A/µs, Tj=150 °C	-	75		ns
Q_{rr}	Reverse recovery charge		-	185		nC
I_{RRM}	Reverse recovery current		-	5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Power derating vs. temperature

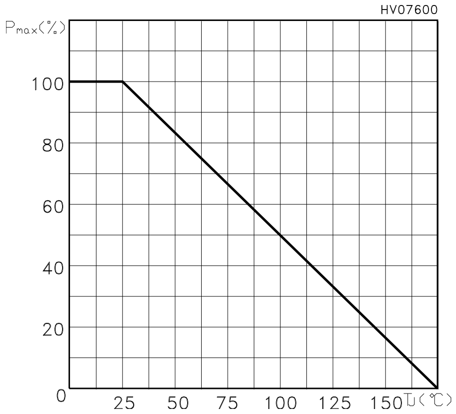


Figure 3. Max Id current vs. temperature

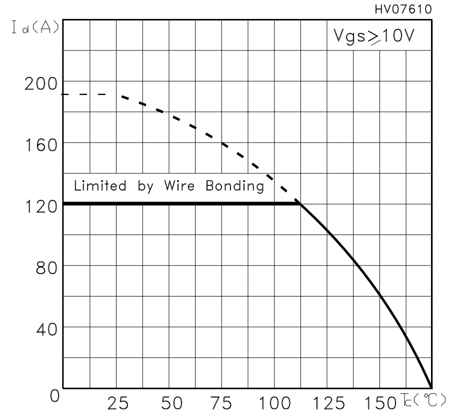


Figure 4. Output characteristics

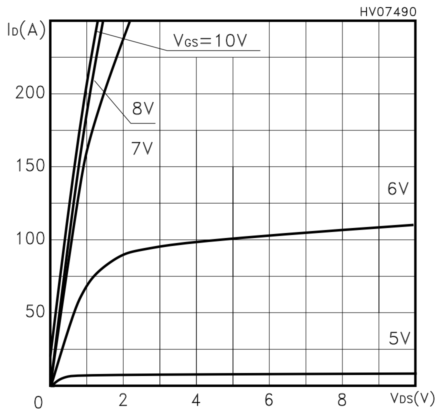


Figure 5. Transfer characteristics

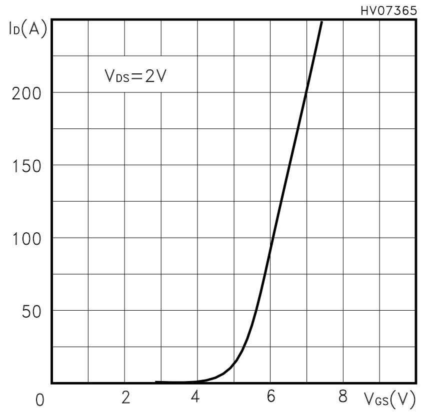


Figure 6. Transconductance

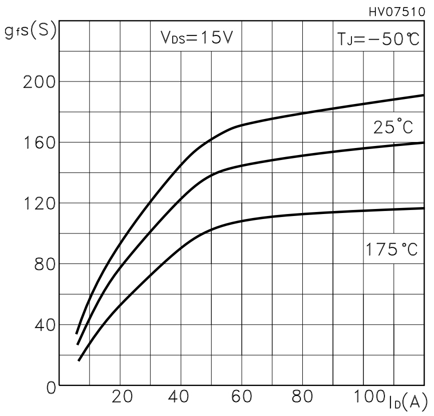


Figure 7. Static drain-source on-resistance

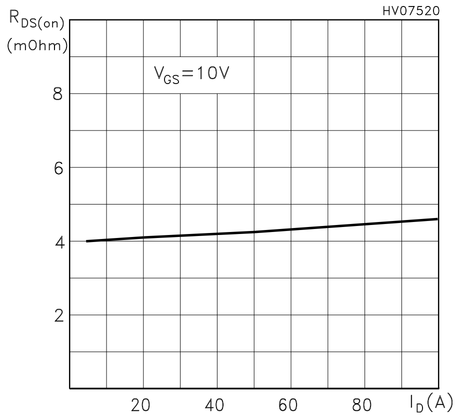


Figure 8. Gate charge vs. gate-source voltage

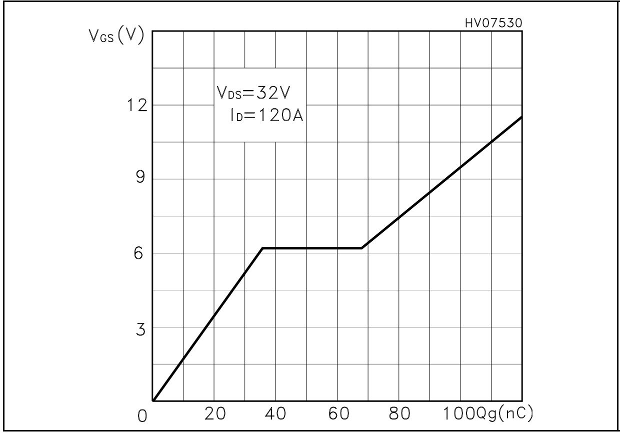


Figure 9. Capacitance variations

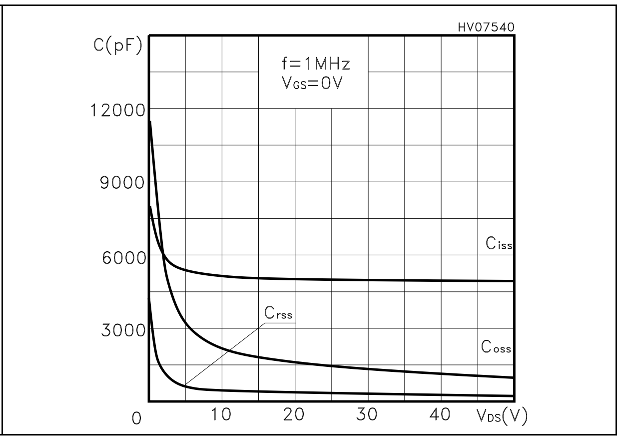


Figure 10. Normalized gate threshold voltage vs. temperature

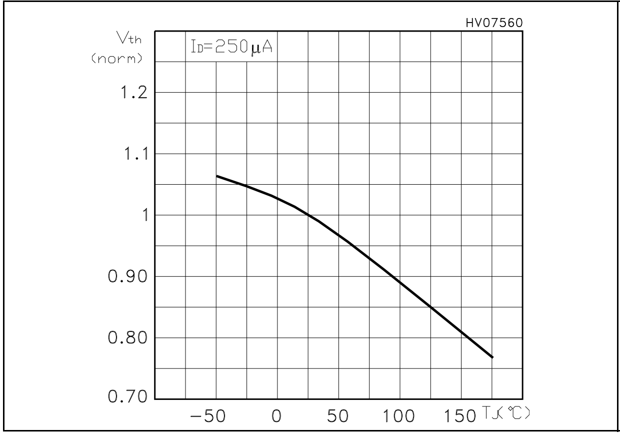


Figure 11. Normalized on-resistance vs. temperature

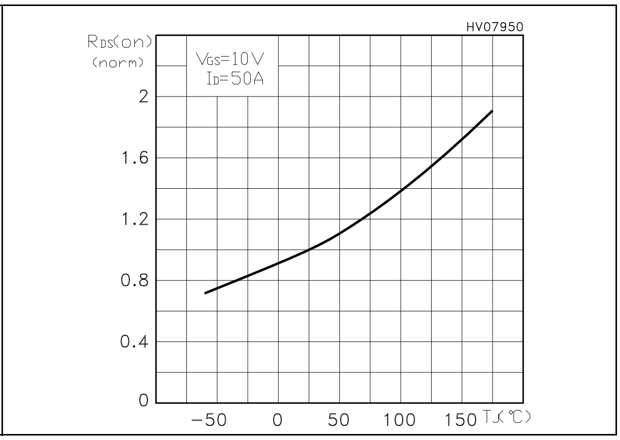


Figure 12. Source-drain diode forward characteristics

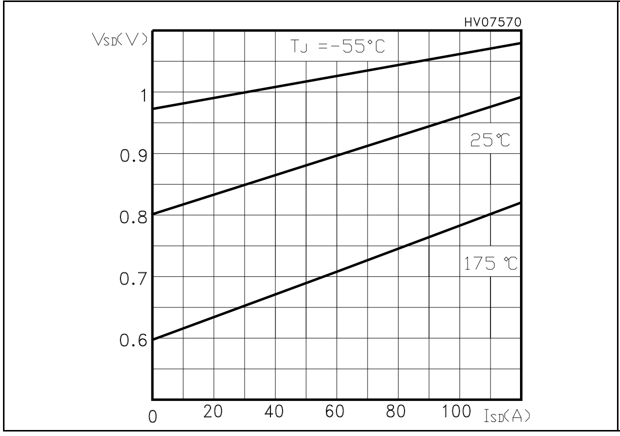


Figure 13. Normalized B_{VDSS} vs. temperature

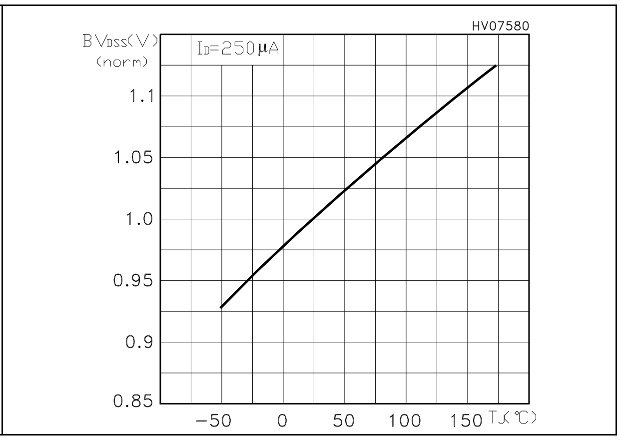


Figure 14. Thermal resistance $R_{thj-pcb}$ vs. PCB copper area

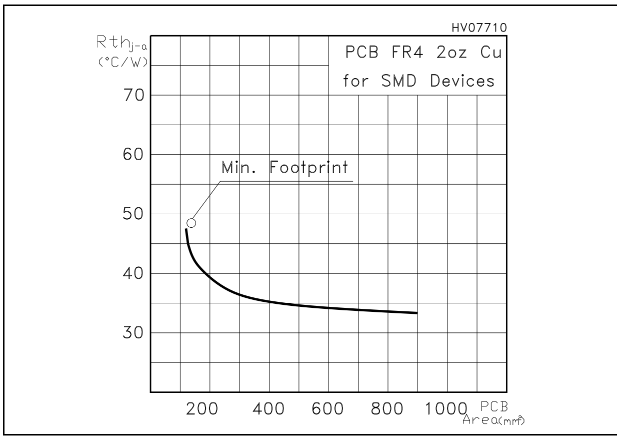


Figure 15. Thermal impedance

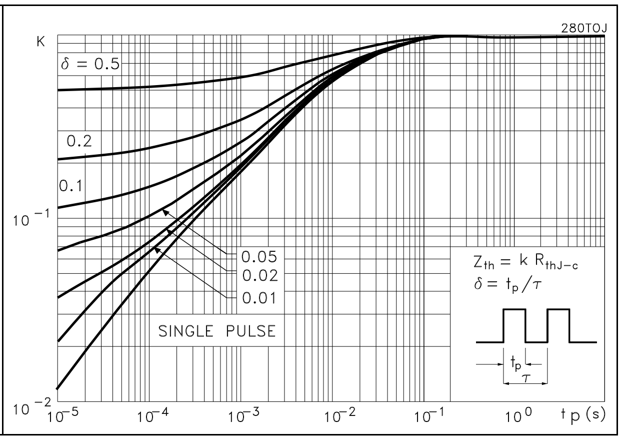


Figure 16. Max power dissipation vs. PCB copper area

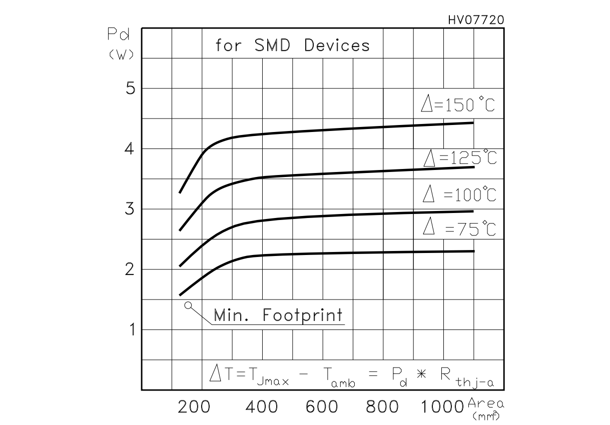


Figure 17. Safe operating area

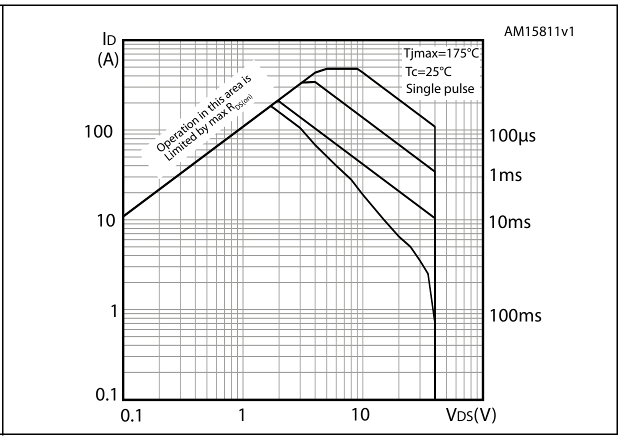
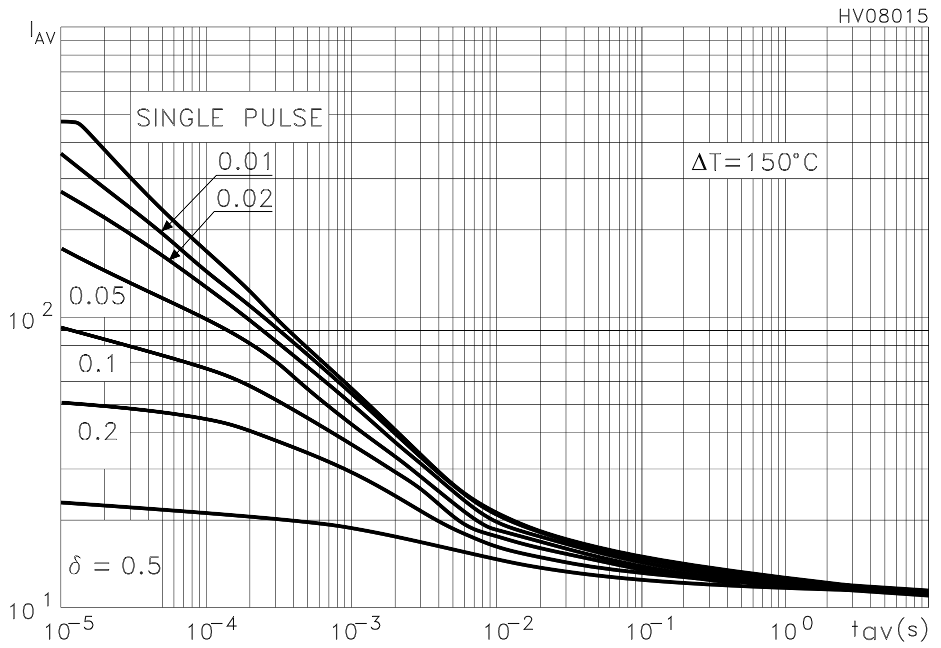


Figure 18. Allowable Iav vs. time in avalanche



The previous curve give the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*BV_{DSS}*I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

To de rate above 25°C, at fixed I_{AV}, the following equation must be applied:

$I_{AV}=2*(T_{jmax} - T_{CASE}) / (1.3*BV_{DSS} * Z_{th})$

Where:

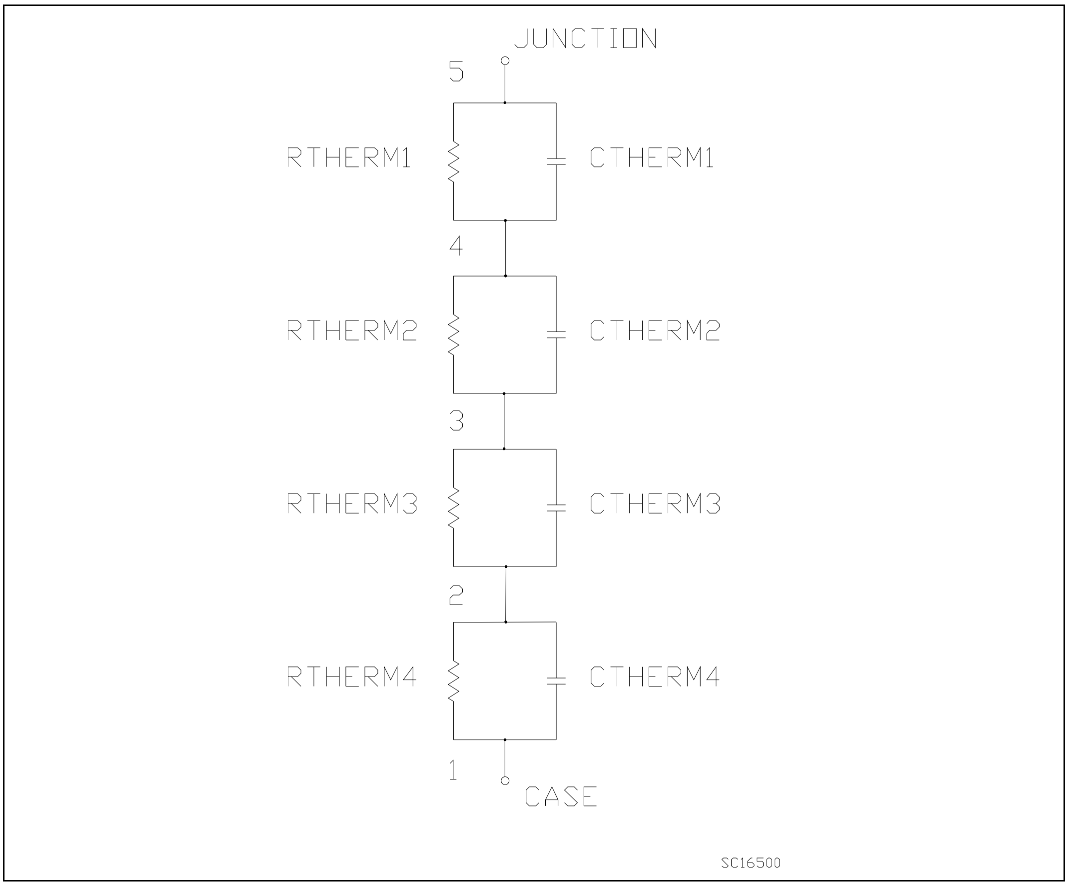
$Z_{th}= K*R_{th}$ is the value coming from normalized thermal response at fixed pulse width equal to T_{AV}

2.2 Spice thermal model

Table 7. Spice parameter

Parameter	Node	Value
CTHERM1	5 - 4	0.011
CTHERM1	4 - 3	0.0012
CTHERM3	3 - 2	0.05
CTHERM4	2 - 1	0.1
RTHERM1	5 - 4	0.09
RTHERM2	4 - 3	0.02
RTHERM3	3 - 2	0.11
RTHERM4	2 - 1	0.17

Figure 19. Spice model schematic



3 Test circuit

Figure 20. Unclamped inductive load test circuit

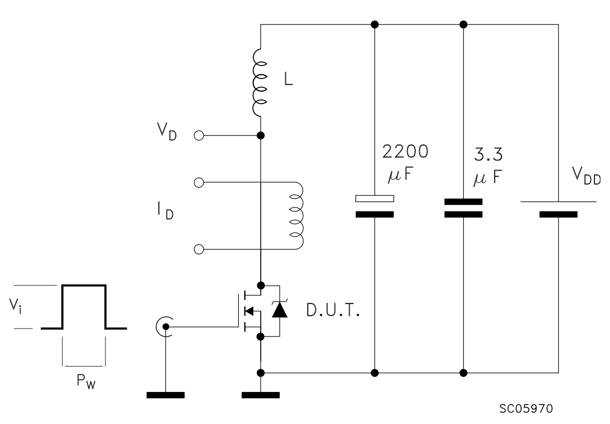


Figure 21. Unclamped inductive waveform

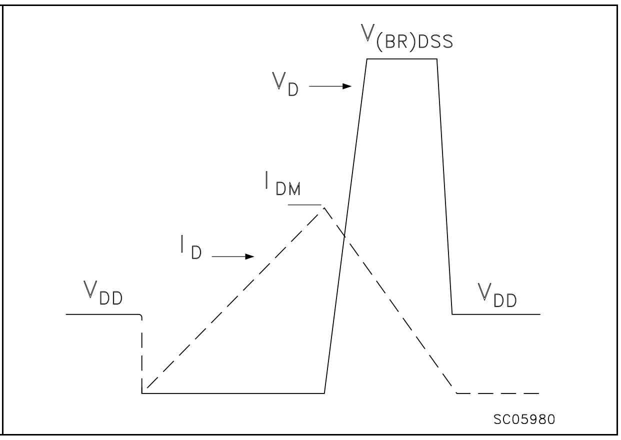


Figure 22. Switching times test circuit for resistive load

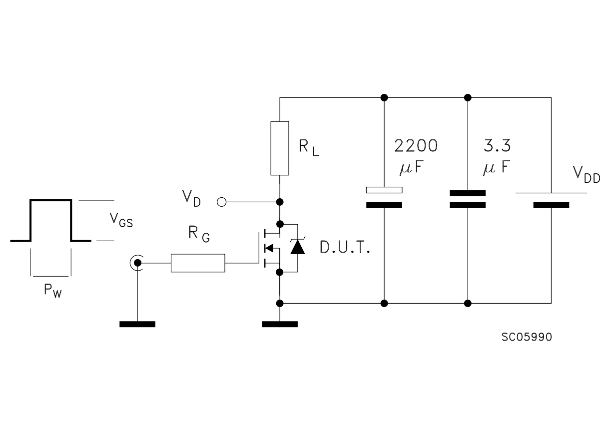


Figure 23. Gate charge test circuit

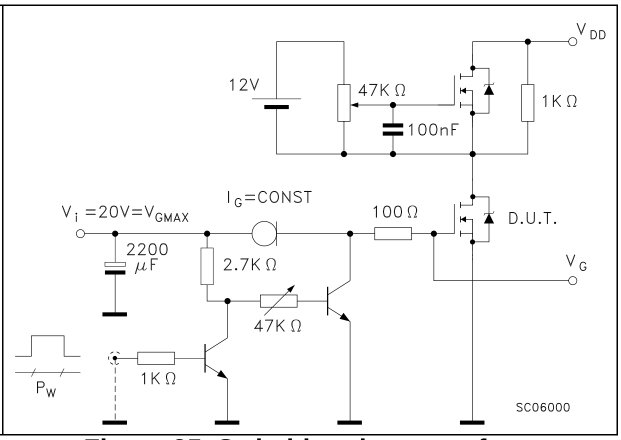


Figure 24. Test circuit for inductive load switching

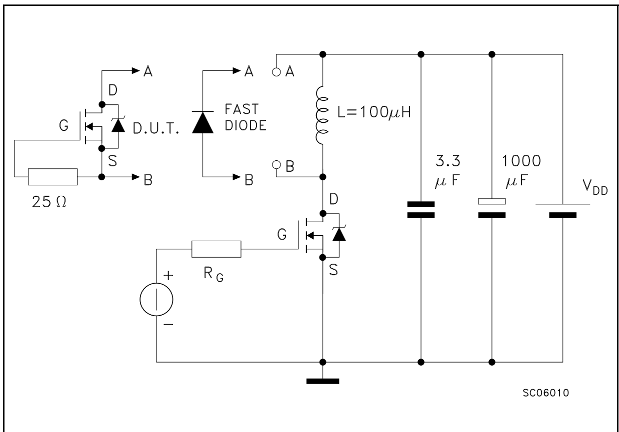
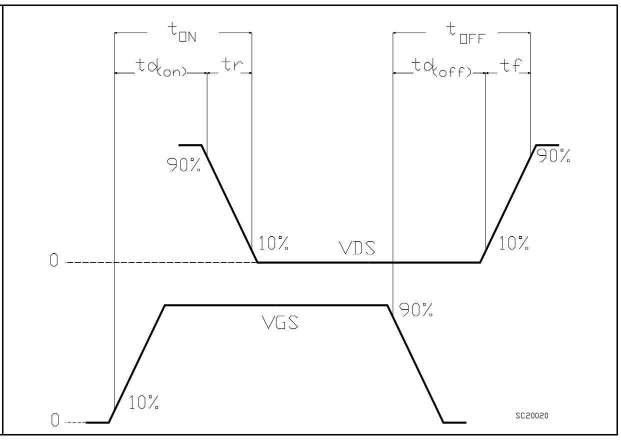


Figure 25. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. D^2PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 26. D²PAK (TO-263) drawing

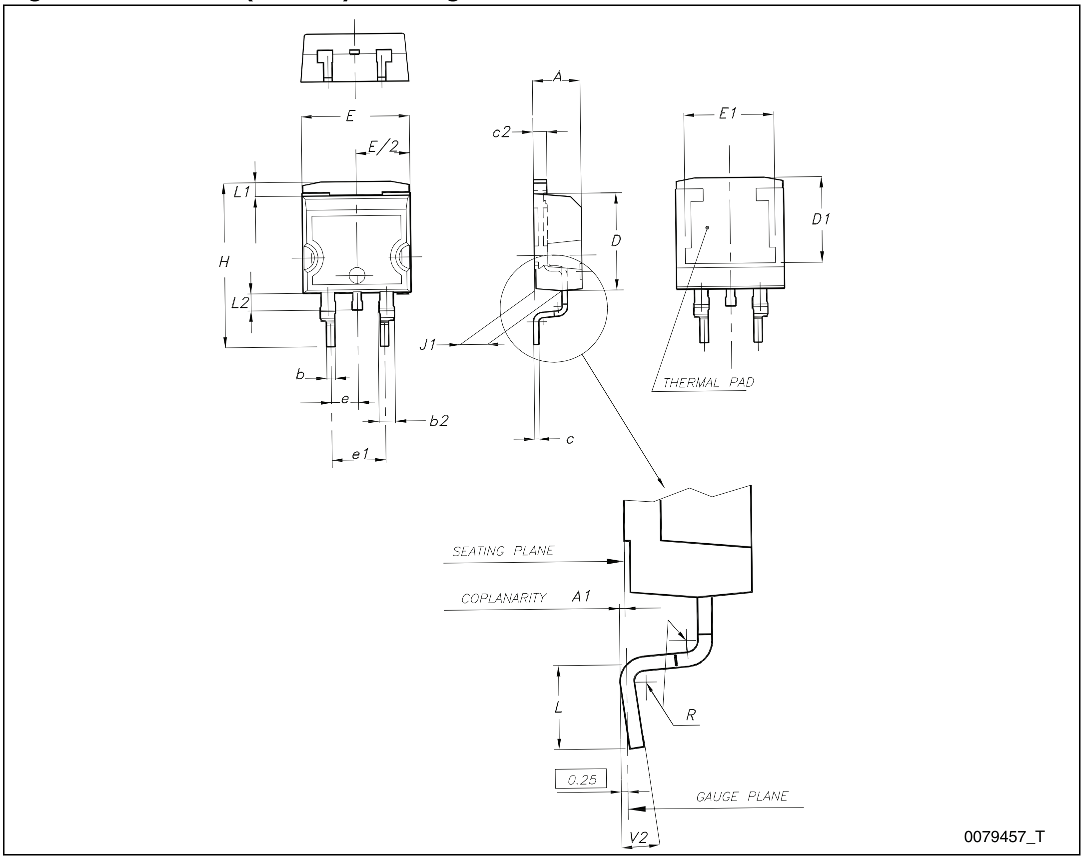
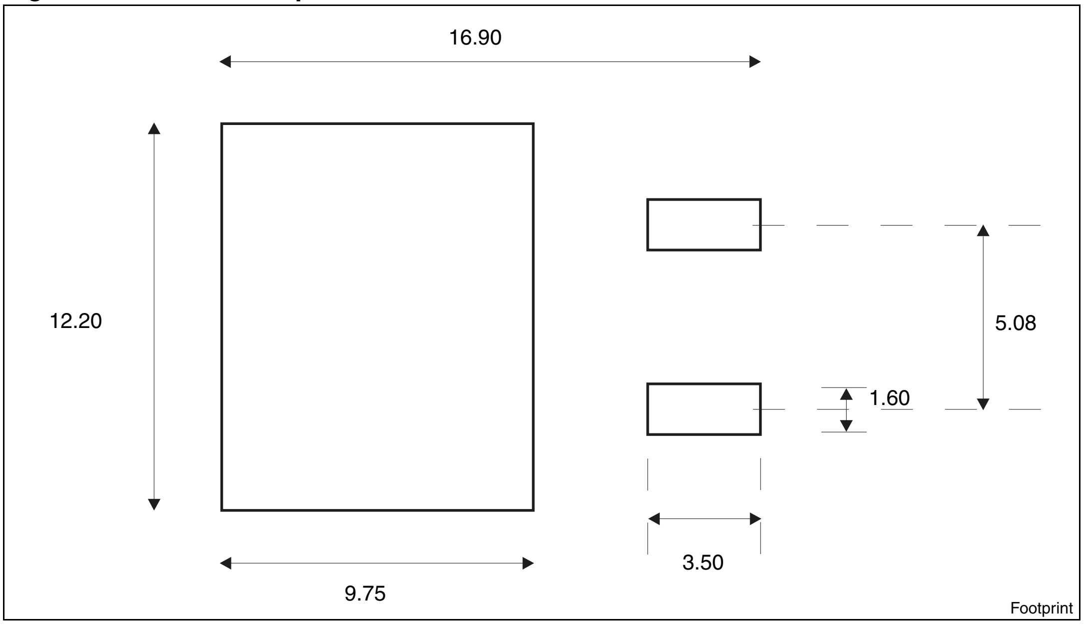


Figure 27. D²PAK footprint[a]

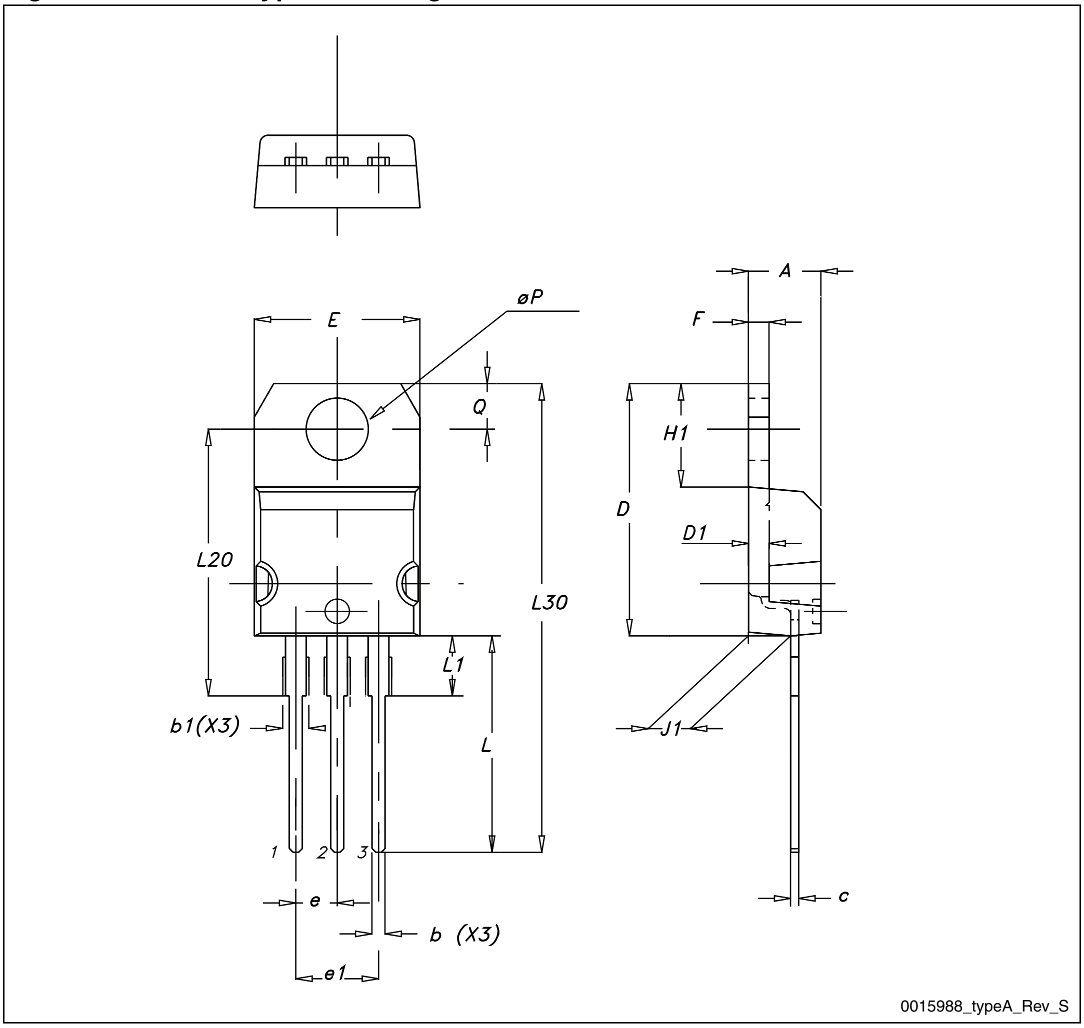


a. All dimension are in millimeters

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 28. TO-220 type A drawing



5 Packaging mechanical data

Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 29. Tape

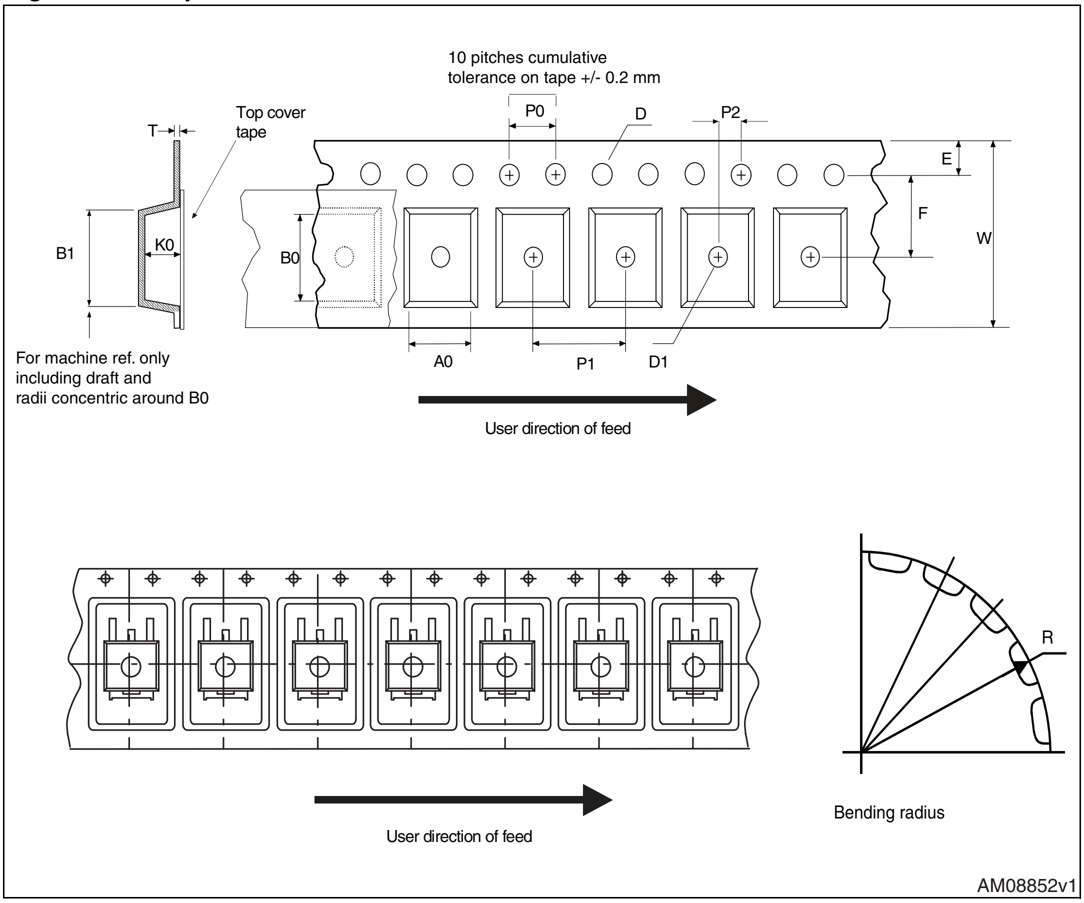
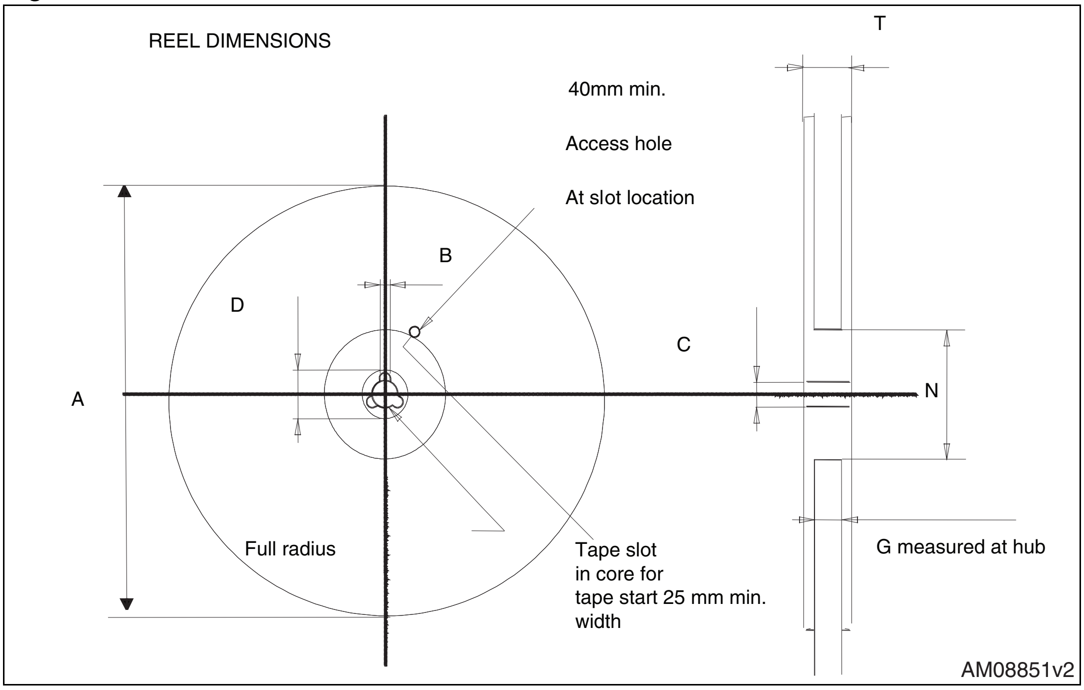


Figure 30. Reel



6 Revision history

Table 11. Revision history

Date	Revision	Changes
23-Mar-2005	2	New template
01-Mar-2006	3	Removed I^2PAK and inserted D^2PAK.
04-Sep-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1
16-May-2013	6	– Minor text changes – Modified: *Figure 17* – Updated: *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*