

N-channel 800 V, 0.95 Ω typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFETs in DPAK, TO-220 and IPAK packages

Datasheet - production data

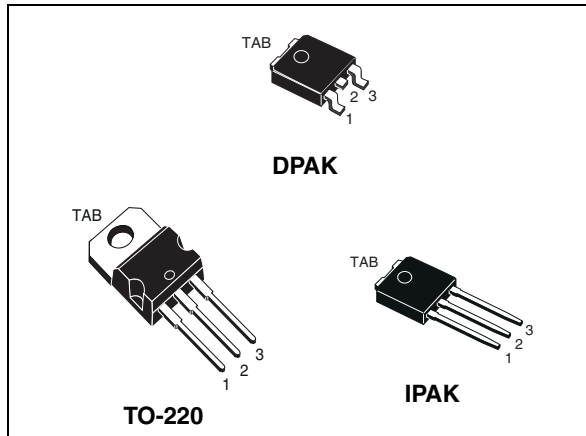
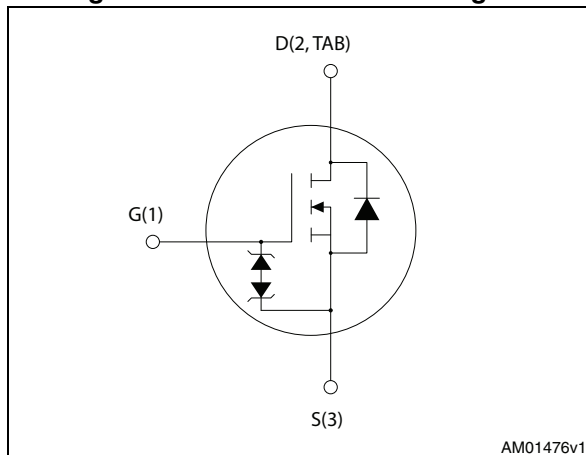


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STD7N80K5	800 V	1.2 Ω	6 A	110 W
STP7N80K5				
STU7N80K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD7N80K5	7N80K5	DPAK	Tape and reel
STP7N80K5		TO-220	Tube
STU7N80K5		IPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25 °C	6	A
I _D	Drain current (continuous) at T _C = 100 °C	3.8	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	24	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{jmax})	2	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AS} , V _{DD} = 50 V)	88	mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
T _J	Operating junction temperature	-55 to 150	°C
T _{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 6 A, di/dt ≤ 100 A/μs, V_{DS(peak)} ≤ V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
R _{thj-case}	Thermal resistance junction-case max	1.14			°C/W
R _{thj-amb}	Thermal resistance junction-amb max		62.5	100	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	50			°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 800\text{ V}$ $V_{DS} = 800\text{ V}, T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		0.95	1.2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	360	-	pF
C_{oss}	Output capacitance		-	30	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }640\text{ V}$	-	47	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	20	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	6	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}, I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 17)	-	13.4	-	nC
Q_{gs}	Gate-source charge		-	3.7	-	nC
Q_{gd}	Gate-drain charge		-	7.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19)	-	11.3	-	ns
t_r	Rise time			8.3		ns
$t_{d(off)}$	Turn-off delay time				23.7	ns
t_f	Fall time				20.2	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 18)	-	315		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	480		ns
Q_{rr}	Reverse recovery charge		-	3.8		μC
I_{RRM}	Reverse recovery current		-	16		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

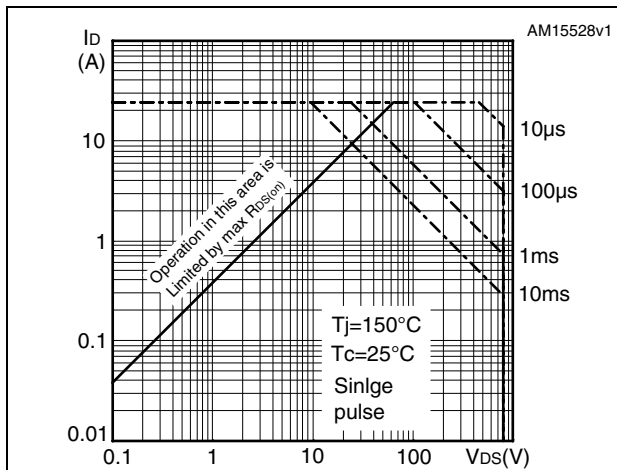


Figure 3. Thermal impedance for DPAK and IPAK

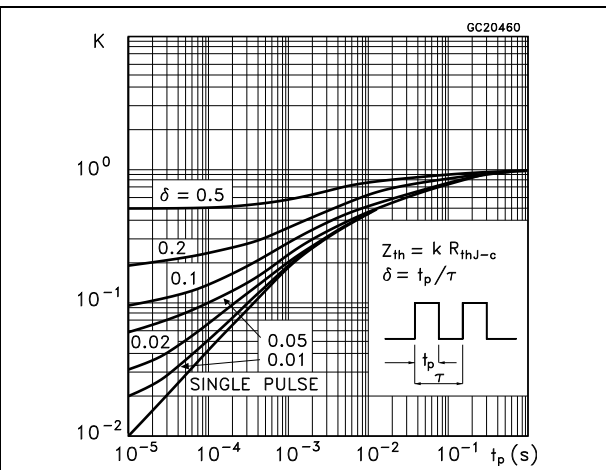


Figure 4. Safe operating area for TO-220

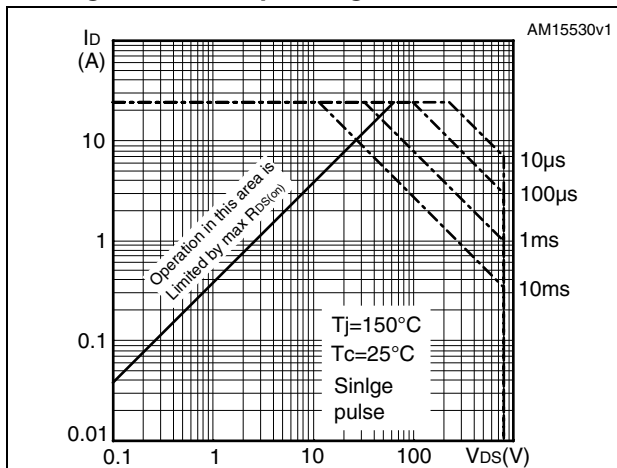


Figure 5. Thermal impedance for TO-220

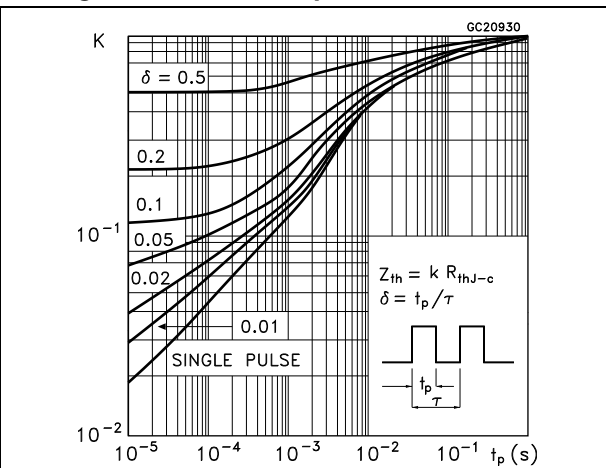


Figure 6. Output characteristics

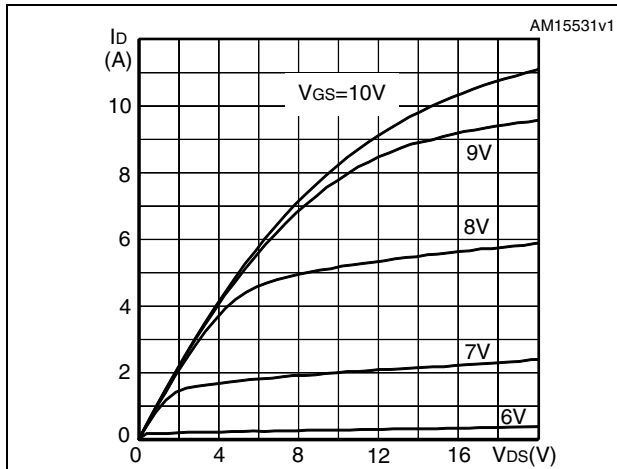


Figure 7. Transfer characteristics

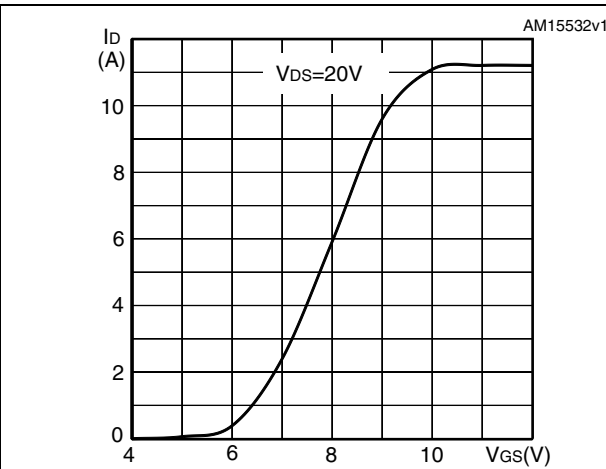


Figure 8. Gate charge vs gate-source voltage

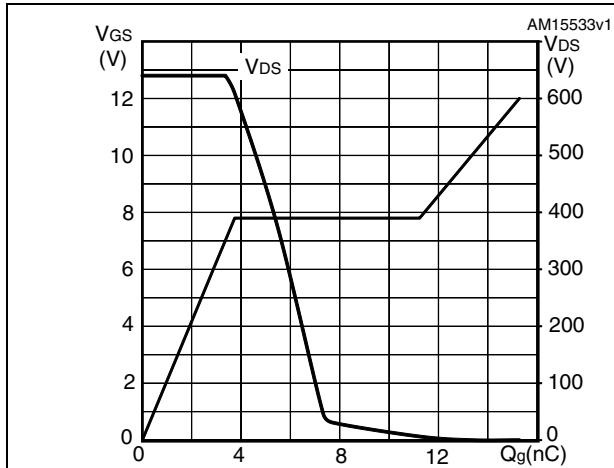


Figure 9. Static drain-source on-resistance

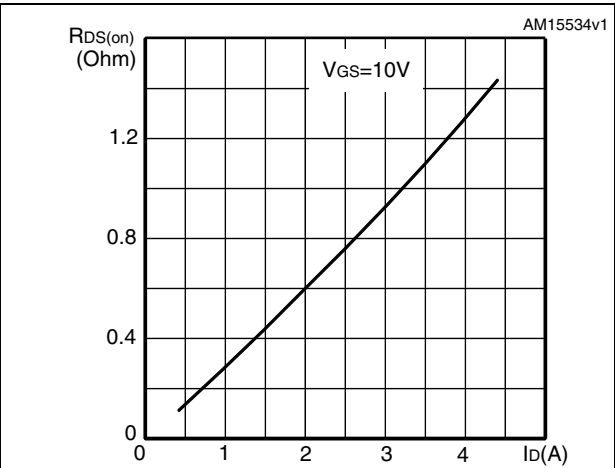


Figure 10. Capacitance variations

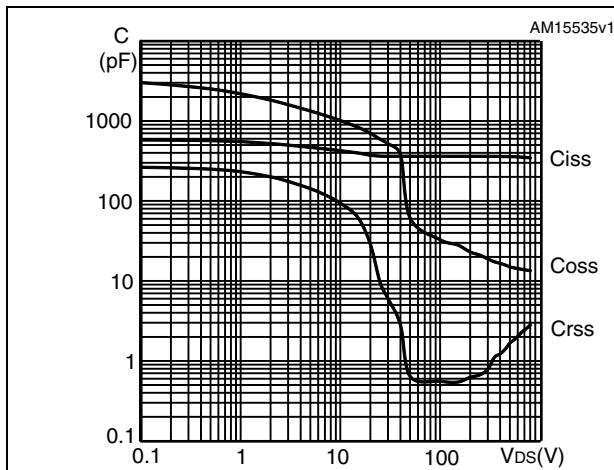


Figure 11. Source-drain diode forward characteristics

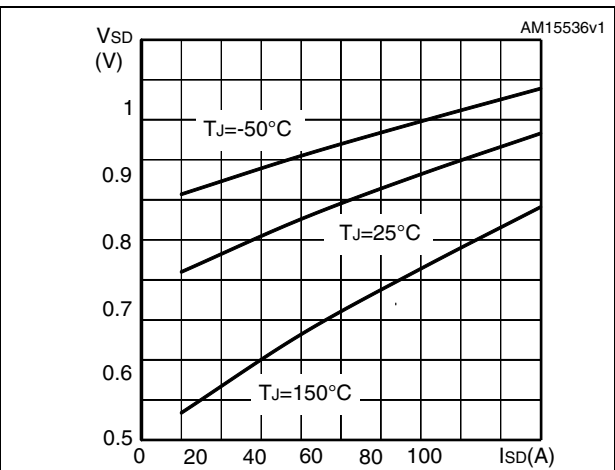


Figure 12. Normalized gate threshold voltage vs temperature

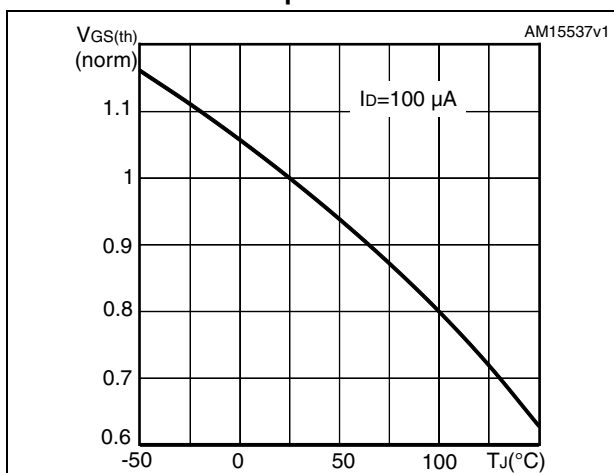


Figure 13. Normalized on-resistance vs temperature

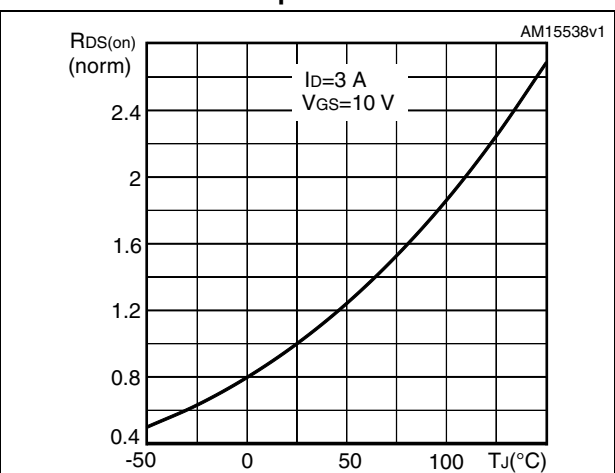


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

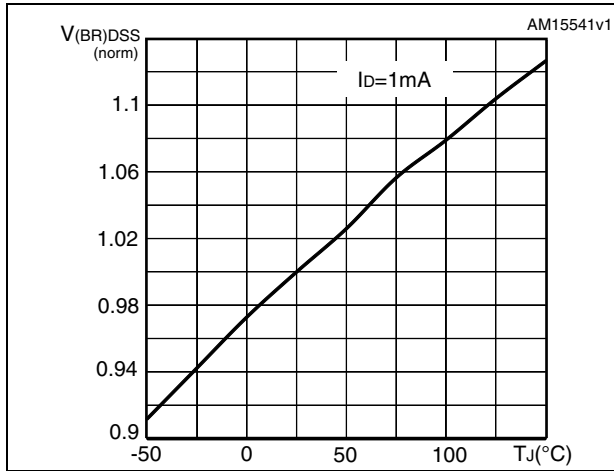
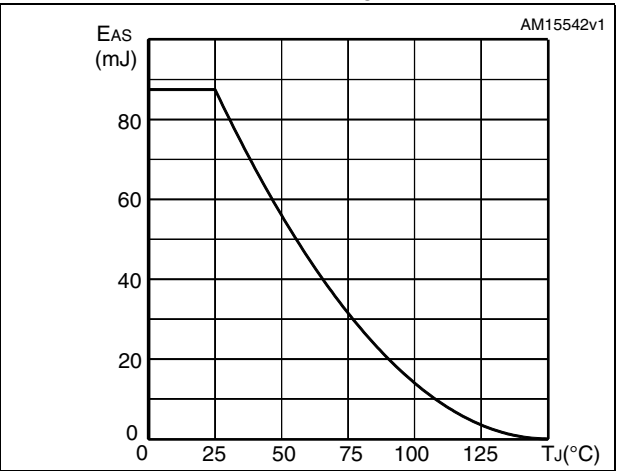


Figure 15. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 16. Switching times test circuit for resistive load



Figure 17. Gate charge test circuit

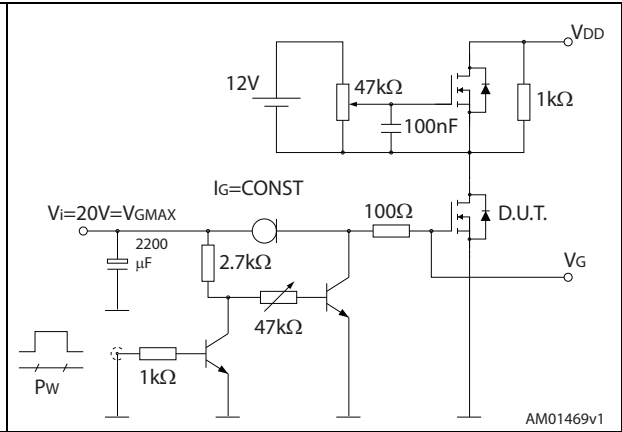


Figure 18. Test circuit for inductive load switching and diode recovery times



Figure 19. Unclamped inductive load test circuit

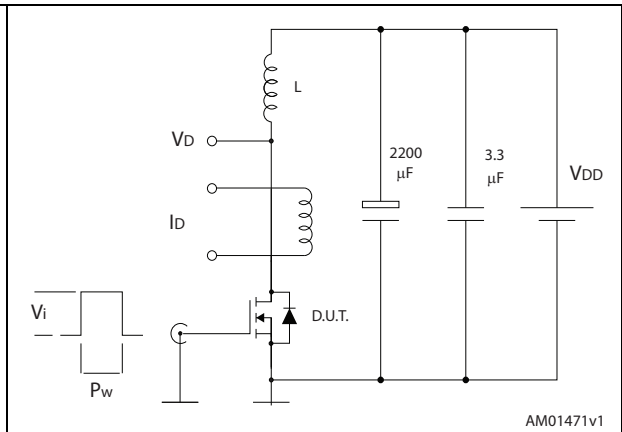


Figure 20. Unclamped inductive waveform

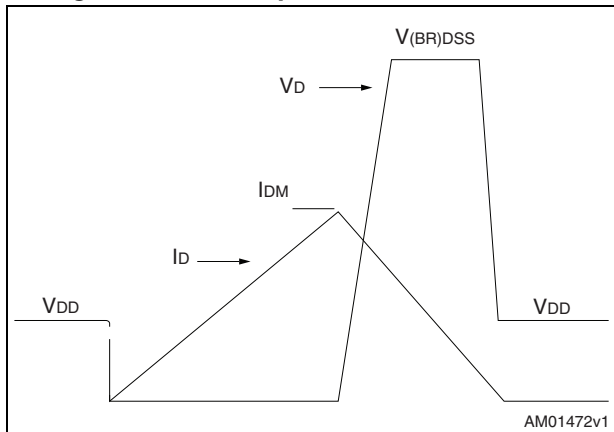
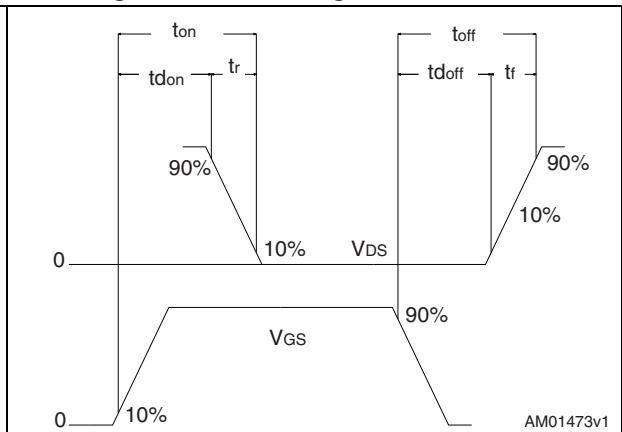


Figure 21. Switching time waveform



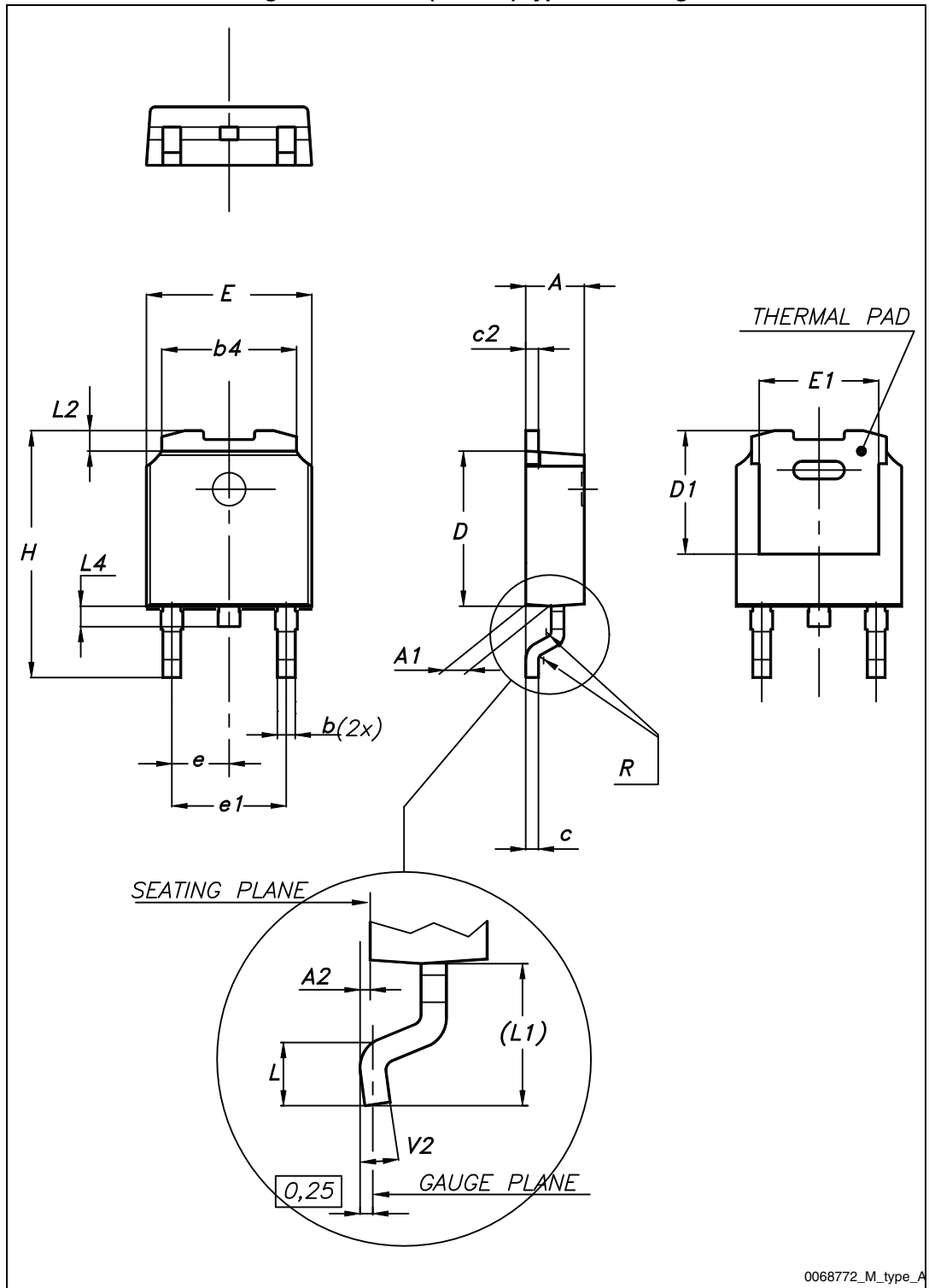
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. DPAK (TO-252) type A mechanical data

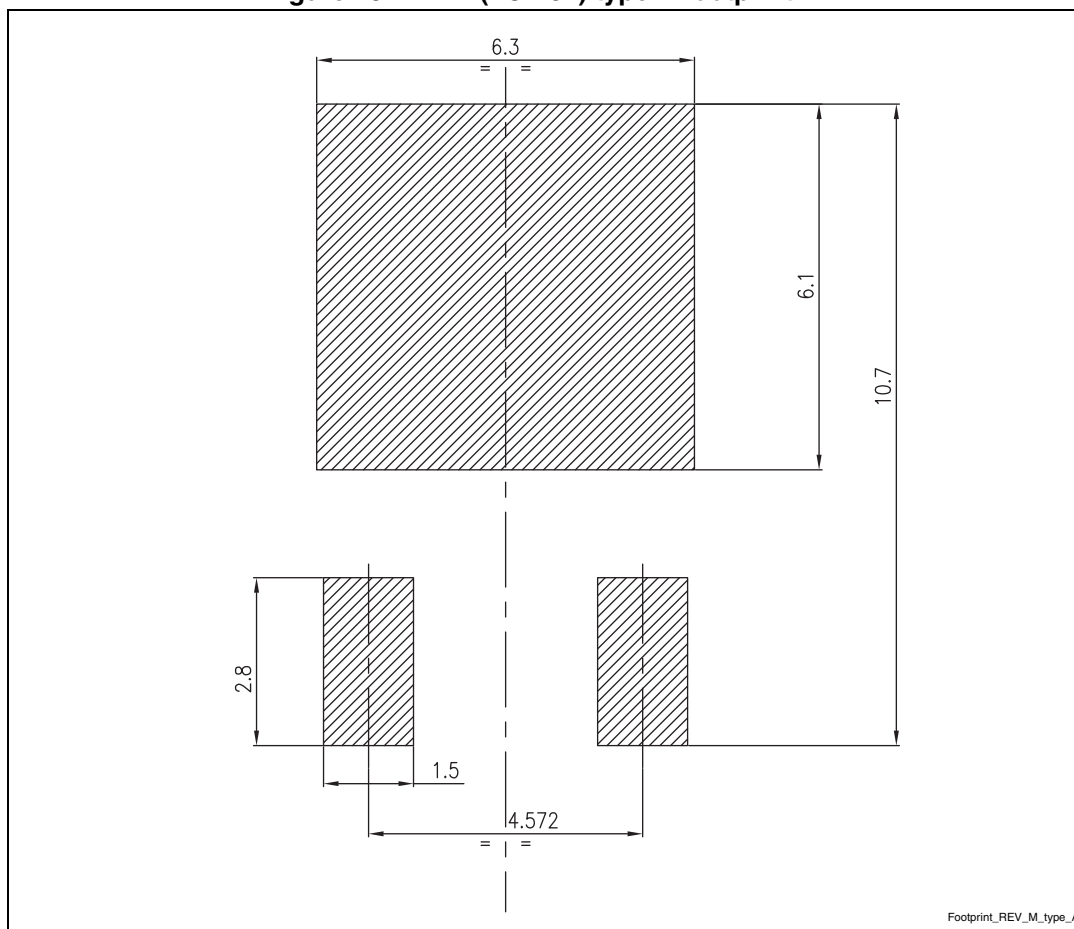
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 22. DPAK (TO-252) type A drawing



0068772_M_type_A

Figure 23. DPAK (TO-252) type A footprint (a)



a. All dimensions are in millimeters

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawing

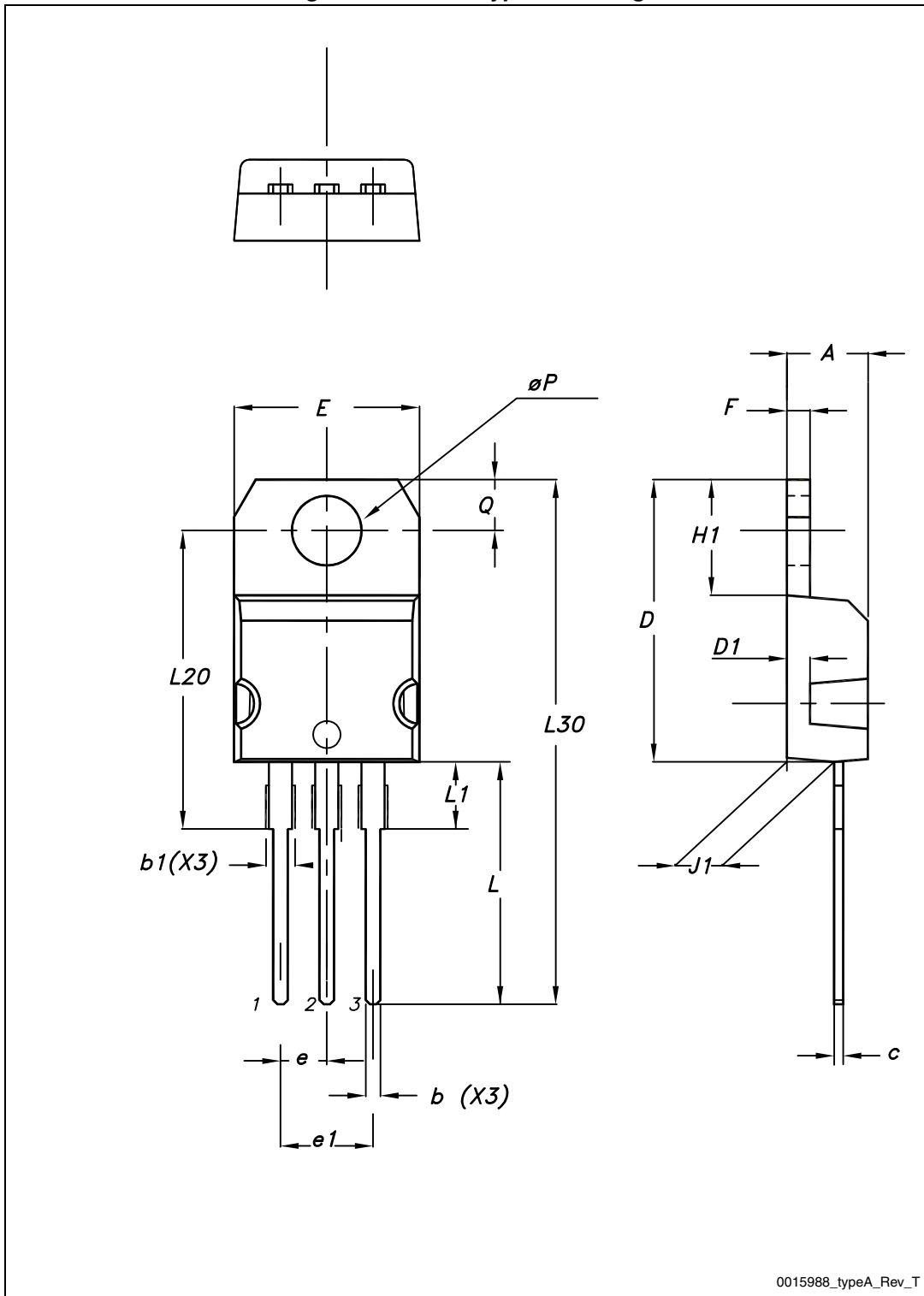
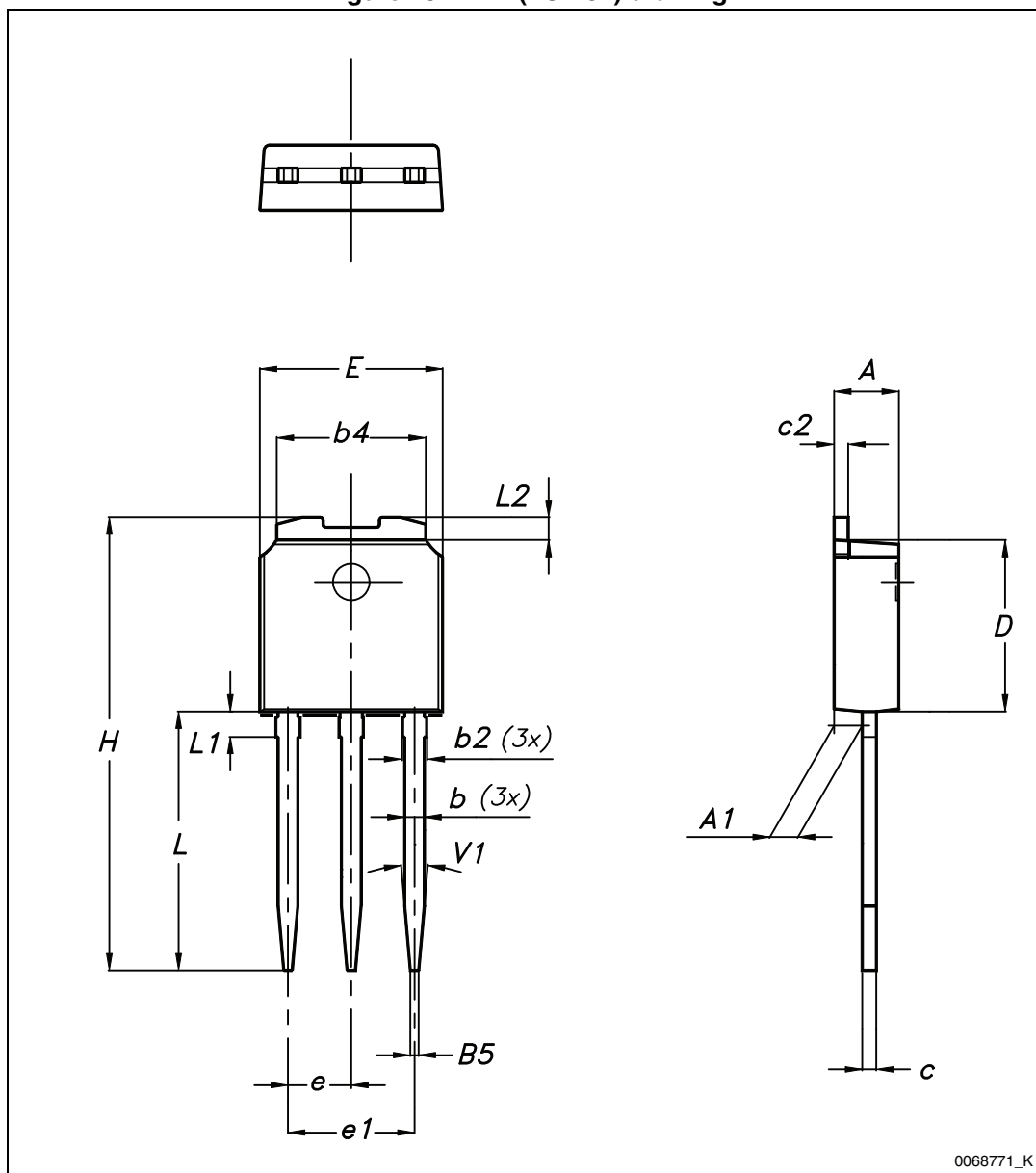


Table 11. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 25. IPAK (TO-251) drawing



0068771_K

5 Packaging mechanical data

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 26. Tape

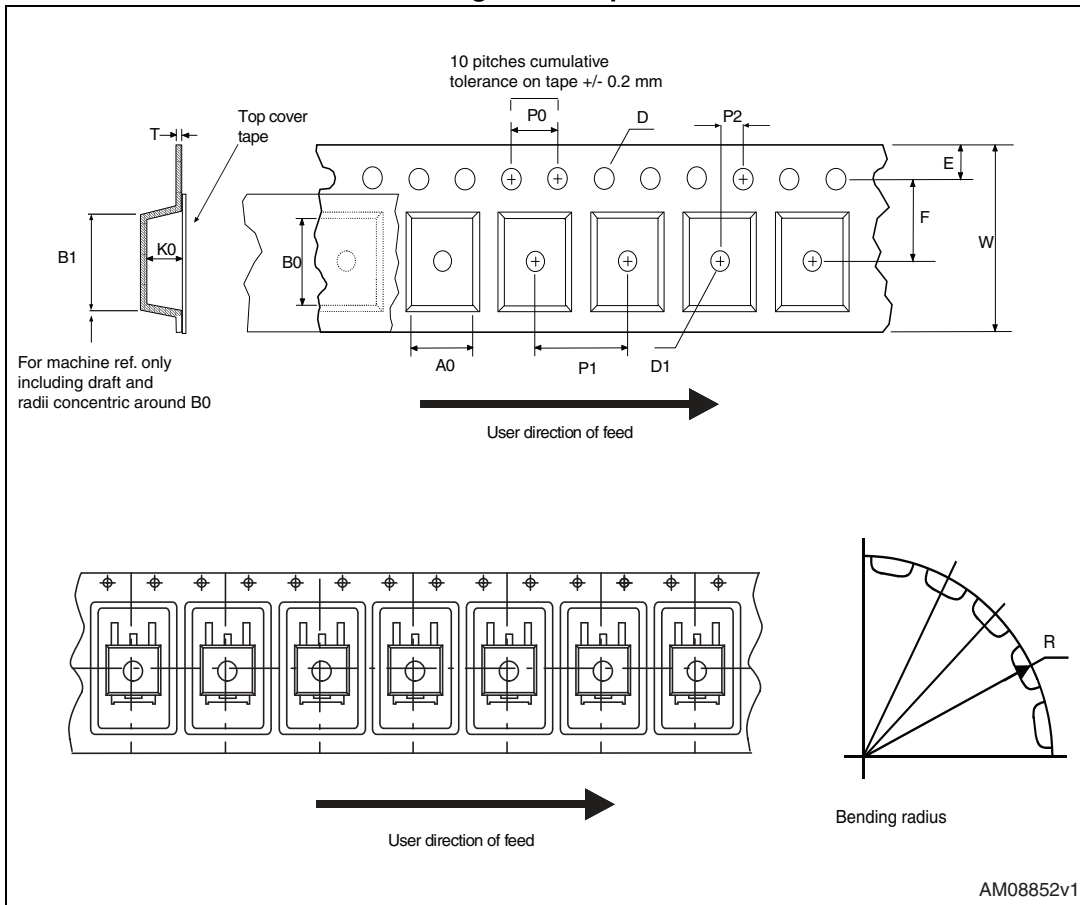
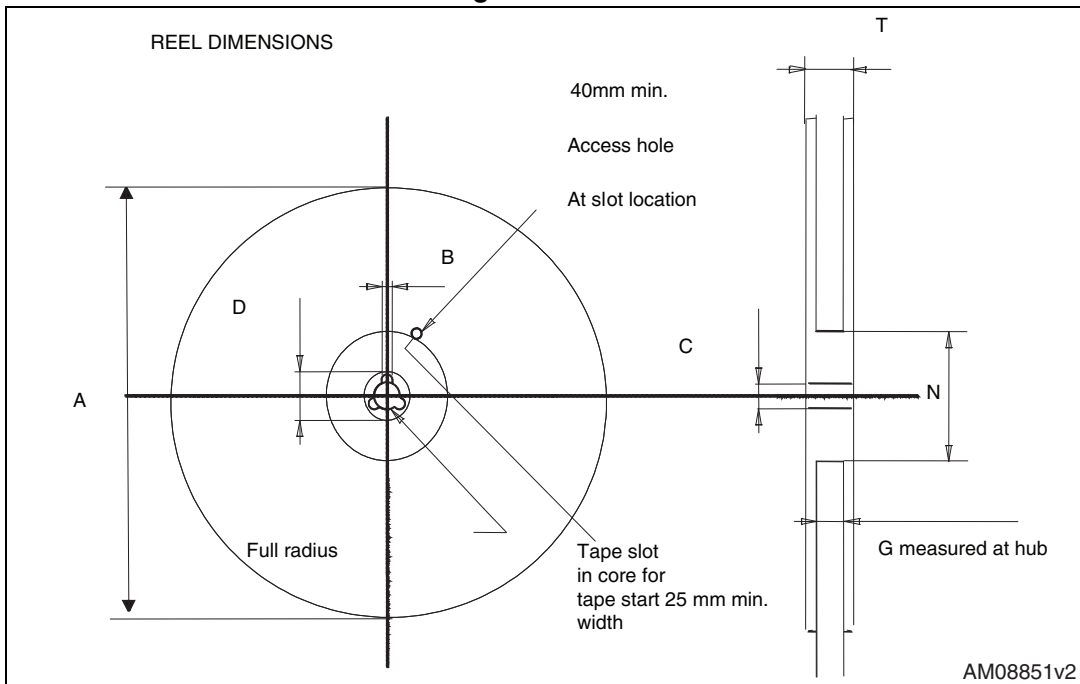


Figure 27. Reel



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
17-Jul-2012	1	First release.
17-Oct-2012	2	– Minor text changes in cover page – Modified: title and I_D value in cover page
19-Dec-2012	3	– Minor text changes – Added: IPAK package – Updated: Section 4: Package mechanical data for IPAK
18-Mar-2013	4	– Modified: I_{AR} value on Table 2 – Updated: Section 4: Package mechanical data only for DPAK package
09-Oct-2013	5	– The part number STF7N80K5 has been moved to a separate datasheet – Minor text changes

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