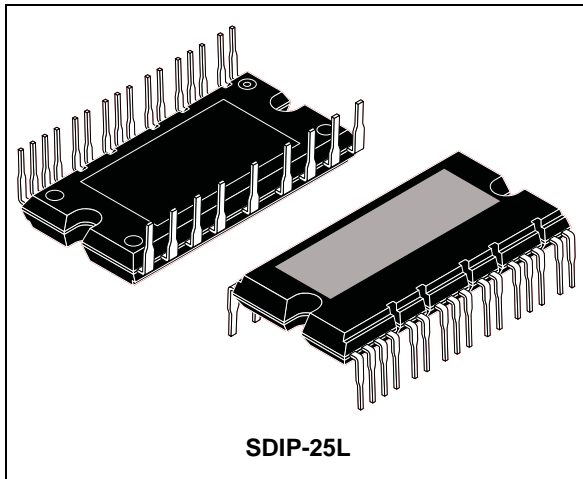


SLLIMM™ small low-loss intelligent molded module IPM, 3-phase inverter - 20 A, 600 V short-circuit rugged IGBT

Datasheet - production data



Applications

- 3-phase inverters for motor drives
- Air conditioners

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as motor drives and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Features

- IPM 20 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down / pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shutdown function
- 4.7 kΩ NTC for temperature control
- DBC leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- UL recognized: UL1557 file E81734

Table 1. Device summary

Order code	Marking	Package	Packing
STGIPS20C60T-H	GIPS20C60T-H	SDIP-25L	Tube

Contents

- 1 Internal block diagram and pin configuration 3**
- 2 Electrical ratings 5**
 - 2.1 Absolute maximum ratings 5
 - 2.2 Thermal data 6
- 3 Electrical characteristics 7**
 - 3.1 Control part 9
 - 3.1.1 NTC thermistor 11
 - 3.2 Waveform definitions 12
- 4 Application information 13**
 - 4.1 Recommendations 14
- 5 Package information 15**
 - 5.1 SDIP-25L package information 15
 - 5.2 Packing information 17
- 6 Revision history 18**

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

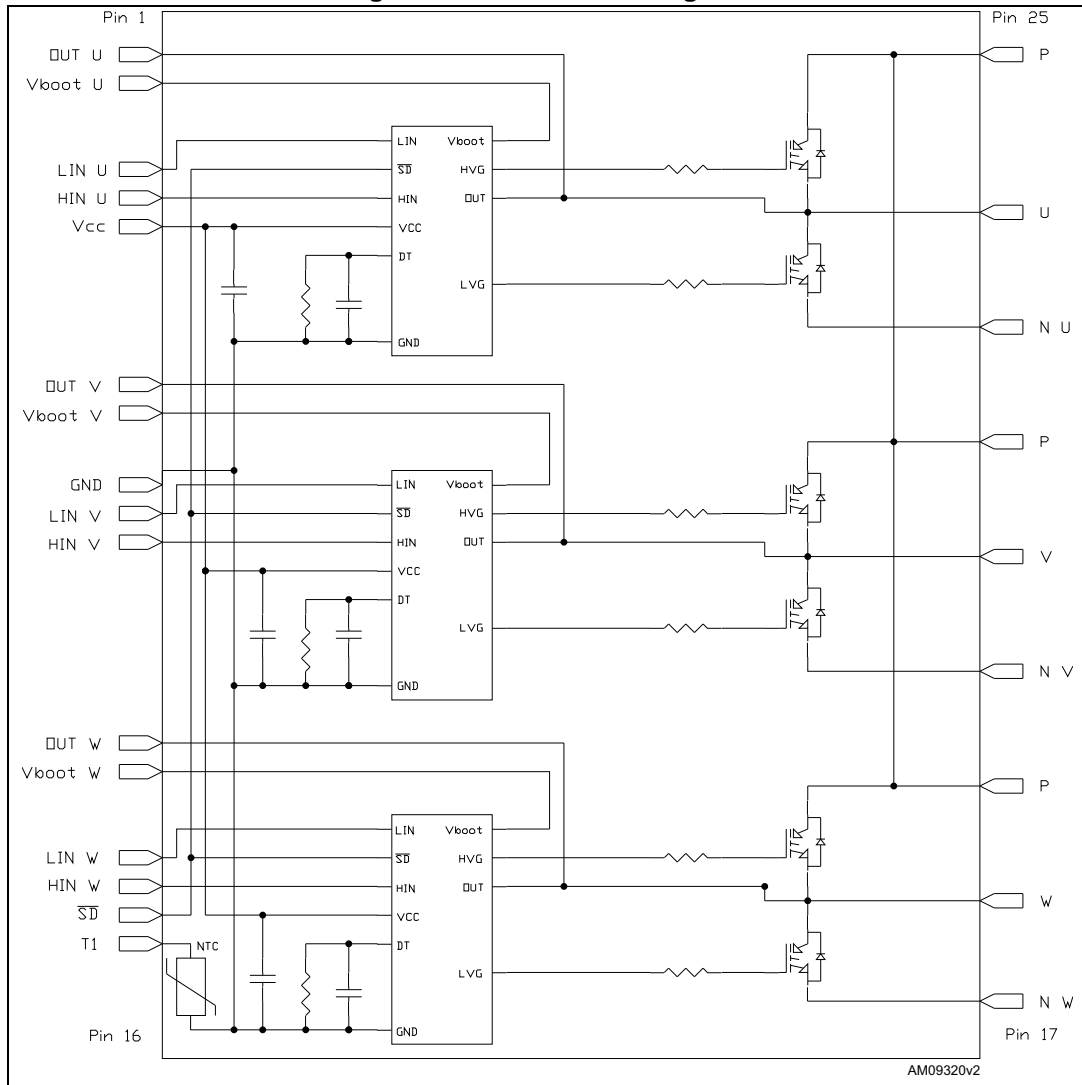
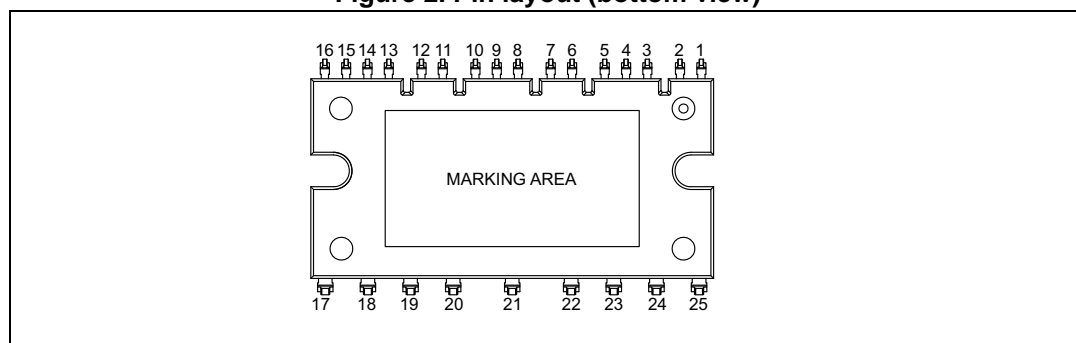


Table 2. Pin description

Pin n°	Symbol	Description
1	OUT _U	High-side reference output for U phase
2	V _{bootU}	Bootstrap voltage for U phase
3	LIN _U	Low-side logic input for U phase
4	HIN _U	High-side logic input for U phase
5	V _{CC}	Low voltage power supply
6	OUT _V	High-side reference output for V phase
7	V _{boot V}	Bootstrap voltage for V phase
8	GND	Ground
9	LIN _V	Low-side logic input for V phase
10	HIN _V	High-side logic input for V phase
11	OUT _W	High-side reference output for W phase
12	V _{boot W}	Bootstrap voltage for W phase
13	LIN _W	Low-side logic input for W phase
14	HIN _W	High-side logic input for W phase
15	\overline{SD}	Shutdown logic input (active low)
16	T1	NTC thermistor terminal
17	N _W	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N _V	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N _U	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U , N_V , N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - N_U , N_V , N_W	500	V
V_{CES}	Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$)	600	V
$\pm I_C$	Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$	20	A
$\pm I_{CP}^{(2)}$	Each IGBT pulsed collector current	40	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25^\circ\text{C}$	46	W
t_{scw}	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$	5	μs

1. Applied between HIN_i , LIN_i and GND for $i = U, V, W$
2. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U , OUT_V , OUT_W - GND	$V_{boot} - 21$ to $V_{boot} + 0.3$	V
V_{CC}	Low voltage power supply	- 0.3 to +21	V
V_{boot}	Bootstrap voltage applied between $V_{boot\ i} - OUT_i$ for $i = U, V, W$	- 0.3 to 620	V
V_{IN}	Logic input voltage applied between HIN , LIN and GND	- 0.3 to 15	V
$V_{SD/OD}$	Open drain voltage	- 0.3 to 15	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$)	2500	V
T_j	Power chips operating junction temperature	- 40 to 150	$^\circ\text{C}$
T_C	Module case operation temperature	- 40 to 125	$^\circ\text{C}$

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT	2.7	°C/W
	Thermal resistance junction-case single diode	5	°C/W

Figure 3. Maximum $I_{C(RMS)}$ current vs. switching frequency (1)

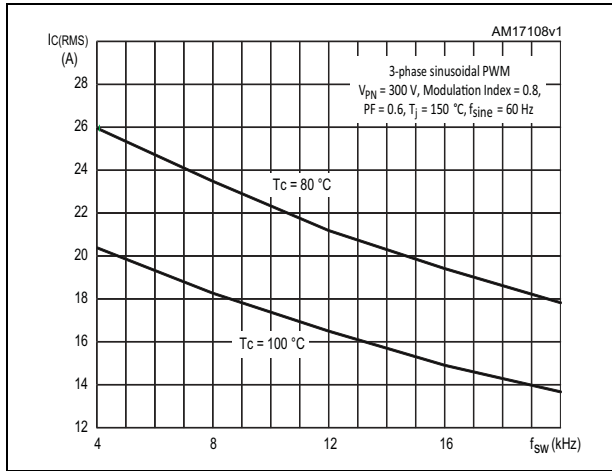
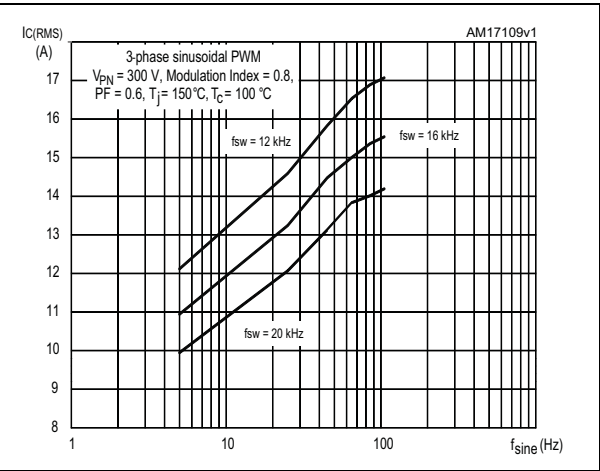


Figure 4. Maximum $I_{C(RMS)}$ current vs. f_{sine} (1)



1. Simulated curves refer to typical IGBT parameters and maximum R_{thj-c} .

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 20\text{ A}$	-	1.6	2	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 20\text{ A}$, $T_J = 125\text{ °C}$	-	1.7		
I_{CES}	Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$	-		100	μA
V_F	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 20\text{ A}$	-		2.2	V
Inductive load switching time and energy						
t_{on}	Turn-on time	$V_{PN} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 20\text{ A}$ (see Figure 5)	-	390	-	ns
$t_{c(on)}$	Crossover time (on)		-	170	-	
t_{off}	Turn-off time		-	970	-	
$t_{c(off)}$	Crossover time (off)		-	150	-	
t_{rr}	Reverse recovery time		-	284	-	μJ
E_{on}	Turn-on switching losses		-	520	-	
E_{off}	Turn-off switching losses		-	460	-	

1. Applied between HIN_i , LIN_i and GND for $i = U, V, W$.

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 5. Switching time test circuit



Figure 6. Switching time definition

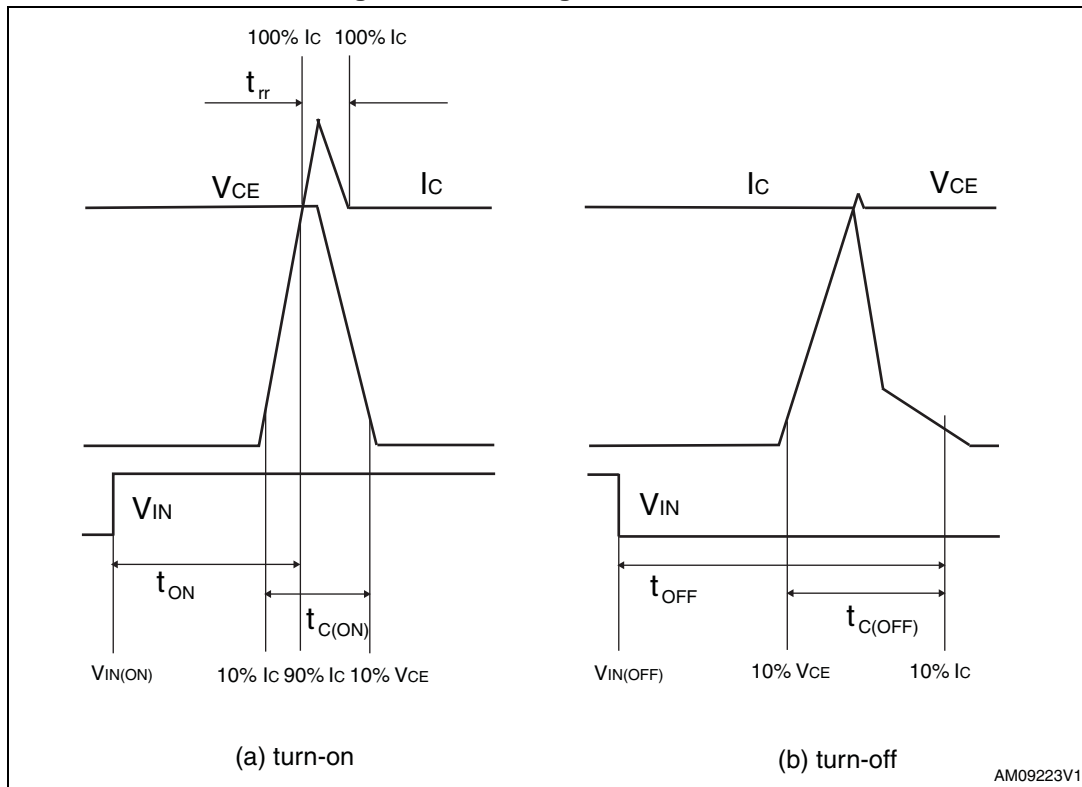


Figure 4 "Switching time definition" refers to HIN, LIN inputs (active high).

3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ $\overline{SD} = 5\text{ V}; \text{LIN} = \text{HIN} = 0$			450	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$ $\overline{SD} = 5\text{ V}; \text{LIN} = \text{HIN} = 0$			3.5	mA

Table 9. Bootstrapped voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	$V_{BS} < 9\text{ V}$ $\overline{SD} = 5\text{ V}; \text{LIN} = 0, \text{HIN} = 5\text{ V}$		70	110	μA
I_{QBS}	V_{BS} quiescent current	$V_{BS} = 15\text{ V}$ $\overline{SD} = 5\text{ V}; \text{LIN} = 0, \text{HIN} = 5\text{ V}$		200	300	μA
$R_{DS(on)}$	Bootstrap driver on resistance	$\text{LIN} = 5\text{ V}; \text{HIN} = 0\text{ V}$		120		Ω

Table 10. Logic inputs ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low level logic threshold voltage		0.8		1.1	V
V_{ih}	High level logic threshold voltage		1.9		2.25	V
I_{HINh}	HIN logic "1" input bias current	$\text{HIN} = 15\text{ V}$	20	40	100	μA
I_{HINI}	HIN logic "0" input bias current	$\text{HIN} = 0\text{ V}$			1	μA
I_{LINh}	LIN logic "1" input bias current	$\text{LIN} = 15\text{ V}$	20	40	100	μA
I_{LINI}	LIN logic "0" input bias current	$\text{LIN} = 0\text{ V}$			1	μA
I_{SDh}	\overline{SD} logic "0" input bias current	$\overline{SD} = 15\text{ V}$	30	120	300	μA
I_{SDI}	\overline{SD} logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	μA
Dt	Dead time	see Figure 7 and Table 14		1.2		μs

Table 11. Sense comparator characteristics ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current	$V_{CIN} = 1\text{ V}$	-		3	μA
V_{ol}	Open-drain low-level output voltage	$I_{od} = 3\text{ mA}$	-		0.5	V
t_{d_comp}	Comparator delay	\overline{SD}/OD pulled to 5 V through 100 k Ω resistor	-	90	130	ns
SR	Slew rate	$C_L = 180\text{ pF}$; $R_{pu} = 5\text{ k}\Omega$	-	60		V/ μsec
t_{sd}	Shut down to high / low side driver propagation delay	$V_{OUT} = 0$, $V_{boot} = V_{CC}$, $V_{IN} = 0$ to 3.3 V	50	125	200	ns

Table 12. Truth table

Condition	Logic input (V_i)			Output	
	\overline{SD}	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 "logic state" half-bridge tri-state	H	L	L	L	L
1 "logic state" low side direct driving	H	H	L	H	L
1 "logic state" high side direct driving	H	L	H	L	H

Note: X: don't care

3.1.1 NTC thermistor

Table 13. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R ₂₅	Resistance	T = 25°C		4.7		kΩ
R ₁₂₅	Resistance	T = 125°C		160		Ω
B	B-constant	T = 25°C to 85°C		3950		K
T	Operating temperature		-40		150	°C

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B \left(\frac{1}{T} - \frac{1}{298} \right)}$$

Where T are temperatures in Kelvins

Figure 7. NTC resistance vs. temperature

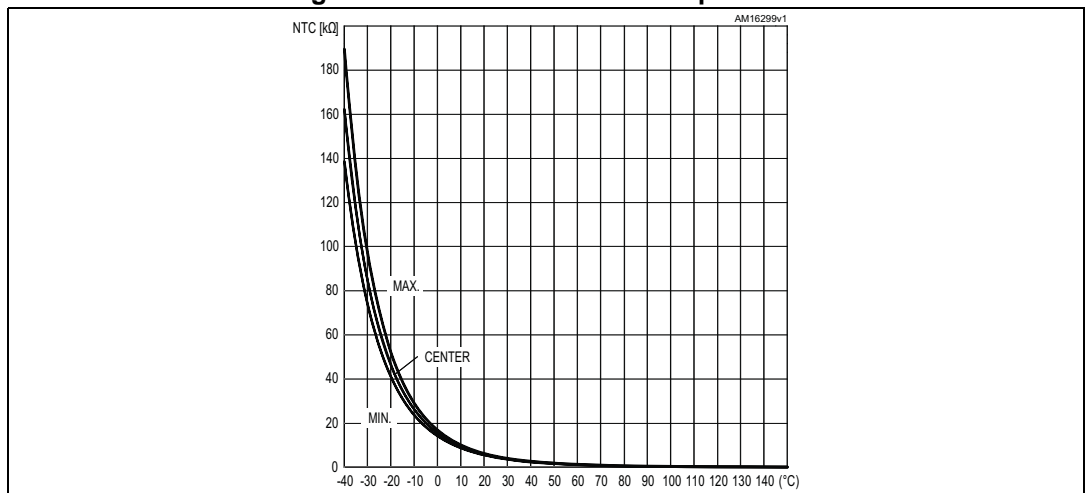
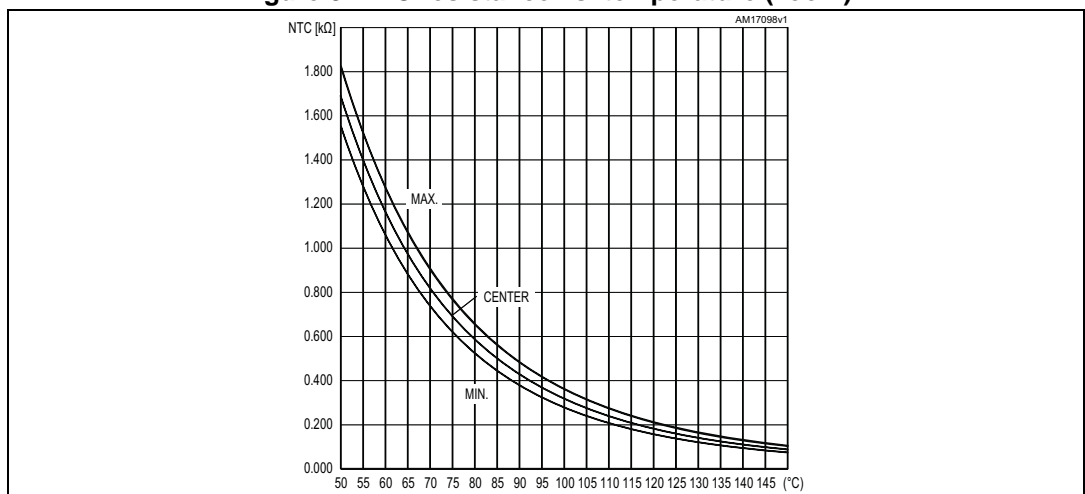
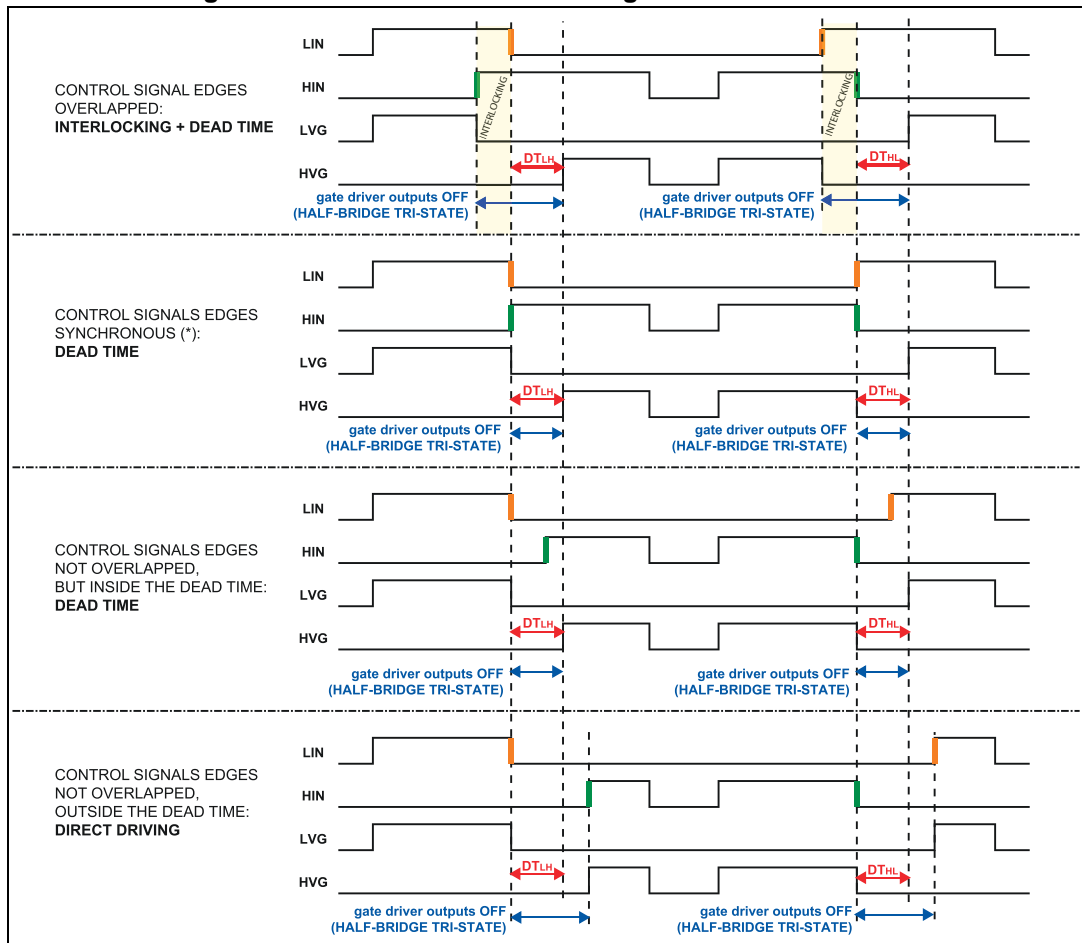


Figure 8. NTC resistance vs. temperature (zoom)



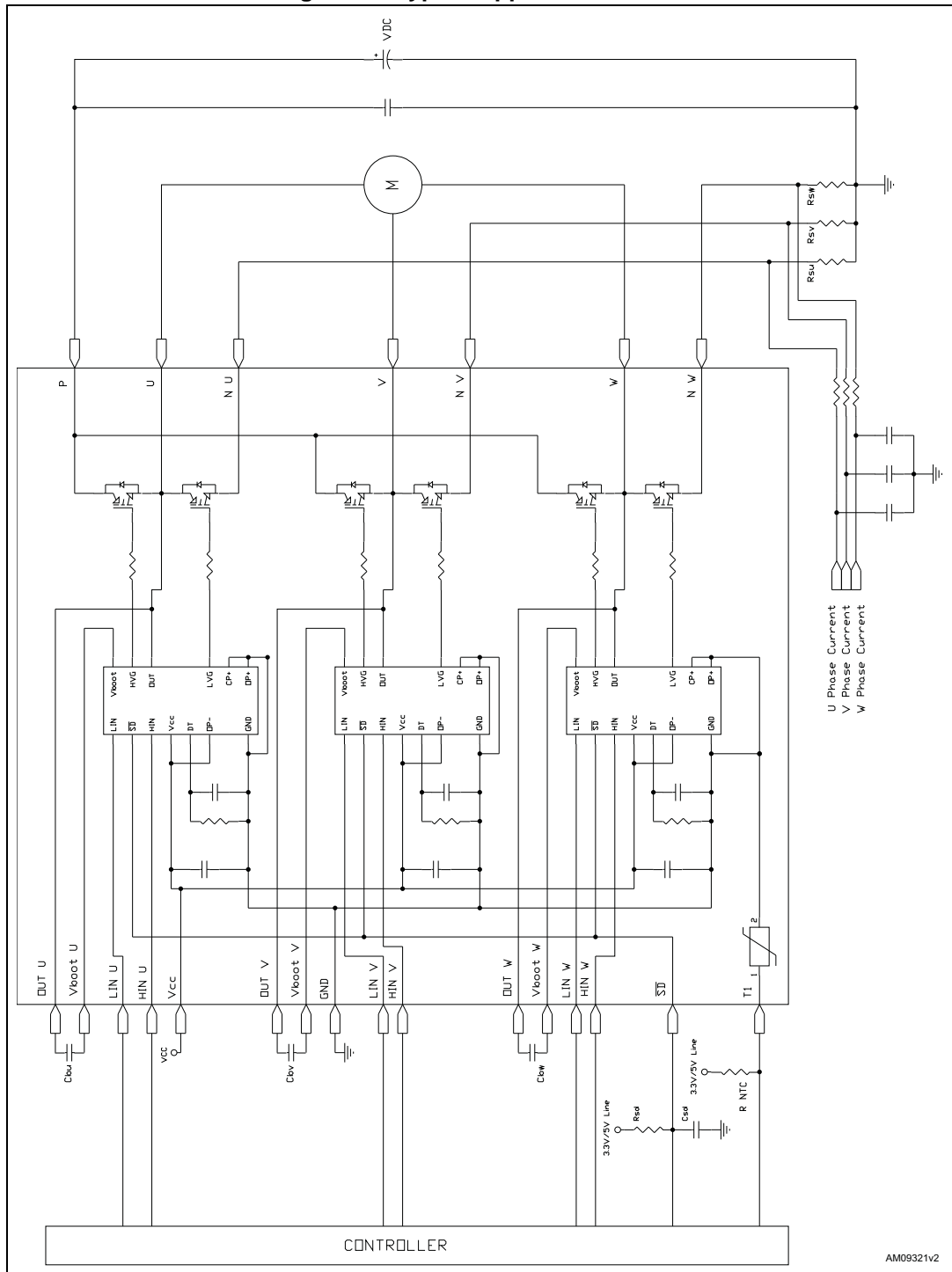
3.2 Waveform definitions

Figure 9. Dead time and interlocking waveforms definition



4 Application information

Figure 10. Typical application circuit



4.1 Recommendations

- Input signals HIN, LIN are active high logic. A 375 k Ω (typ.) pull down resistor is built-in for each input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The \overline{SD} signal should be pulled up to 5 V / 3.3 V with an external resistor.

Table 14. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V _{PN}	Supply Voltage	Applied between P-Nu,Nv,Nw		300	400	V
V _{CC}	Control supply voltage	Applied between V _{CC} -GND	13.5	15	18	V
V _{BS}	High side bias voltage	Applied between V _{BOOTi} -OUT _i for i=U,V,W	13		18	V
t _{dead}	Blanking time to prevent Arm-short	For each input signal	1.5			μ s
f _{PWM}	PWM input signal	-40°C < T _c < 100°C -40°C < T _j < 125°C			20	kHz
T _C	Case operation temperature				100	°C

Note: For further details refer to AN3338.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

5.1 SDIP-25L package information

Figure 11. SDIP-25L package outline

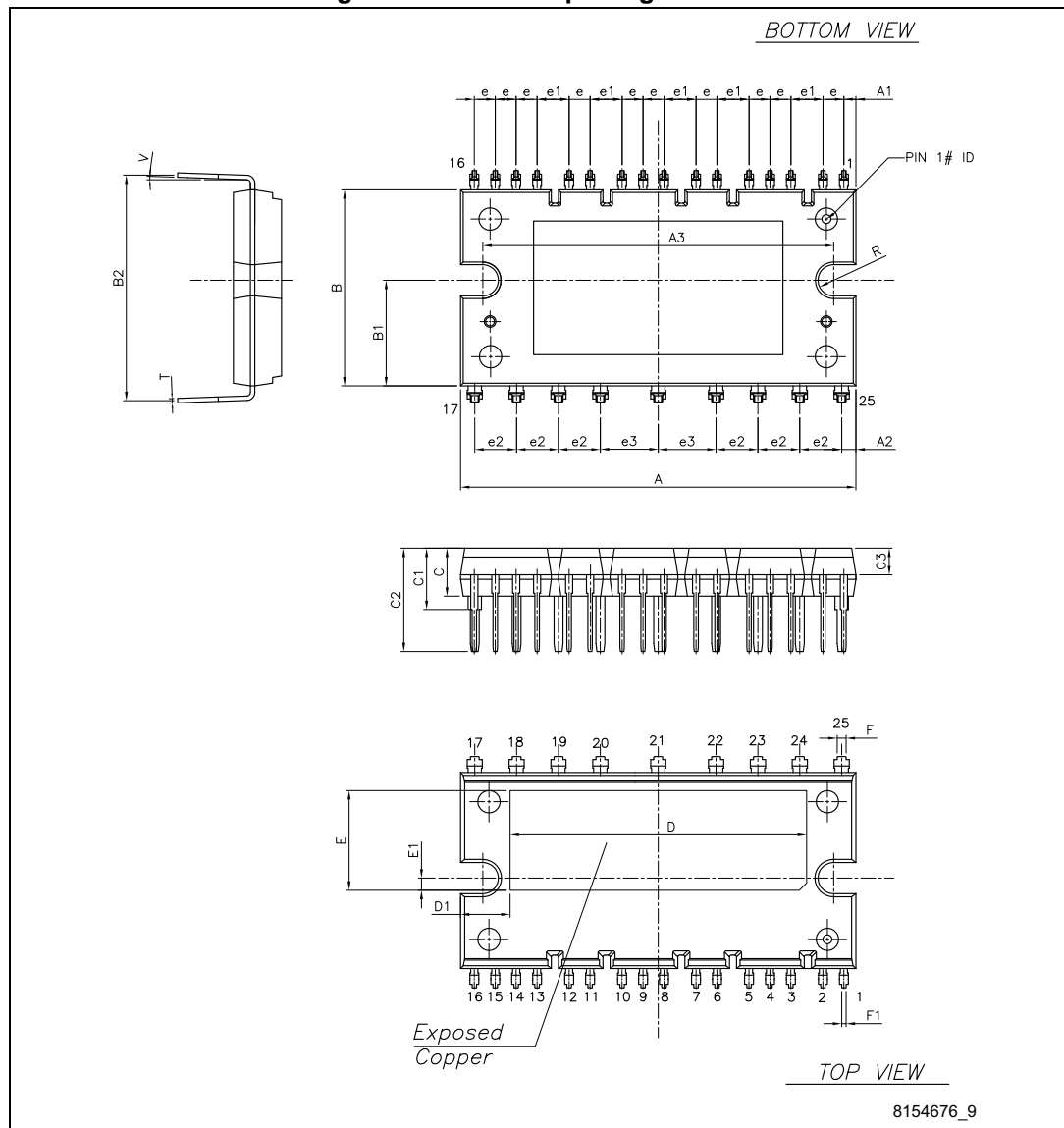
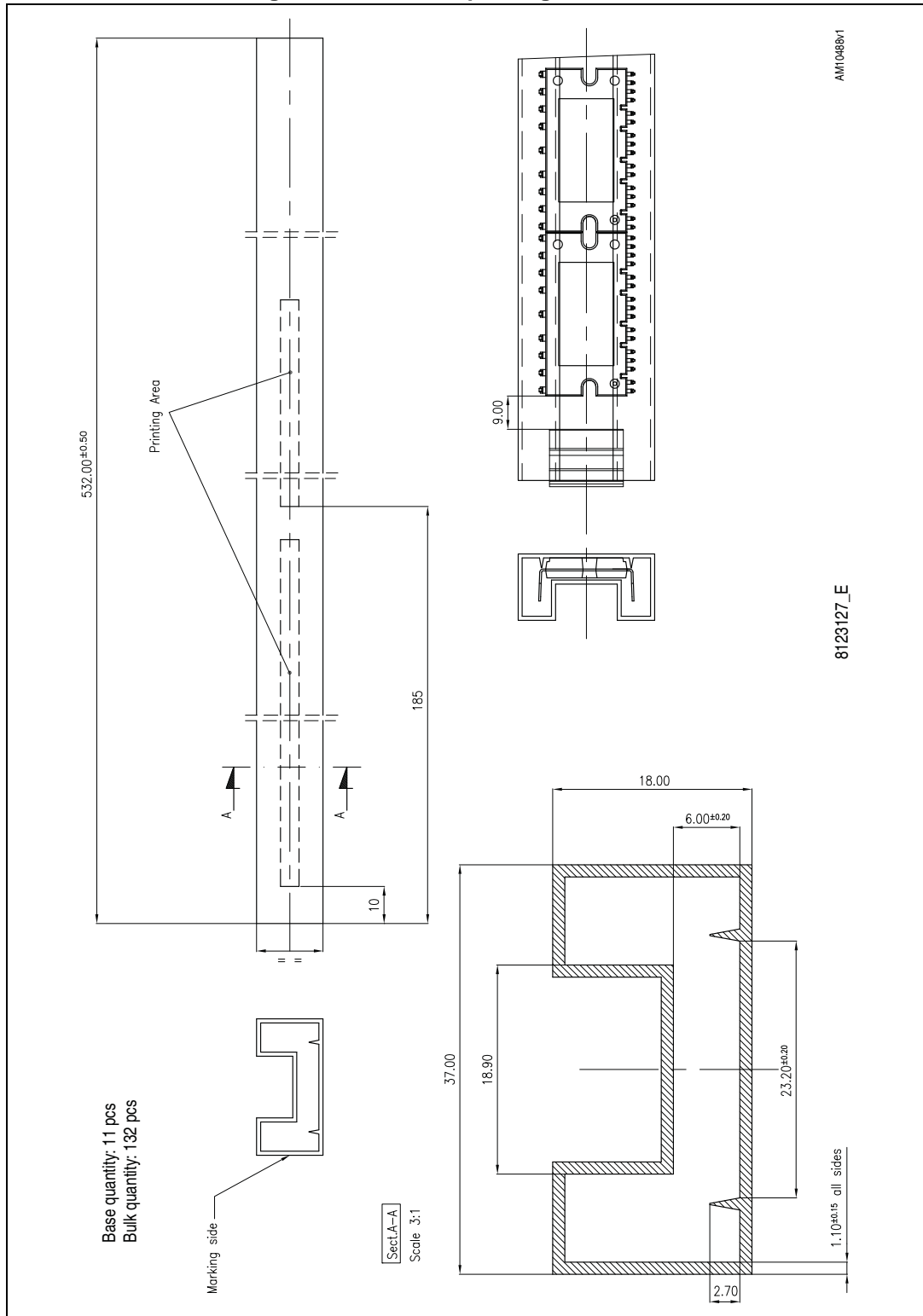


Table 15. SDIP-25L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	43.90	44.40	44.90
A1	1.15	1.35	1.55
A2	1.40	1.60	1.80
A3	38.90	39.40	39.90
B	21.50	22.00	22.50
B1	11.25	11.85	12.45
B2	24.83	25.23	25.63
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	11.20	11.70	12.20
C3	2.90	3.00	3.10
e	2.15	2.35	2.55
e1	3.40	3.60	3.80
e2	4.50	4.70	4.90
e3	6.30	6.50	6.70
D		33.30	
D1		5.55	
E		11.20	
E1		1.40	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

5.2 Packing information

Figure 12. SDIP-25L packing information



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
09-Oct-2014	1	Initial release
10-Apr-2015	2	Text edits and formatting changes throughout document Updated Figure 2: Pin layout (bottom view) Updated Section 5: Package information

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