

## P-channel 60 V, 0.13 $\Omega$ typ., 12 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

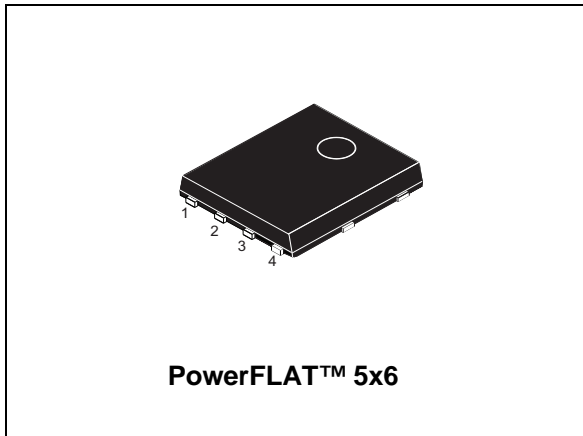
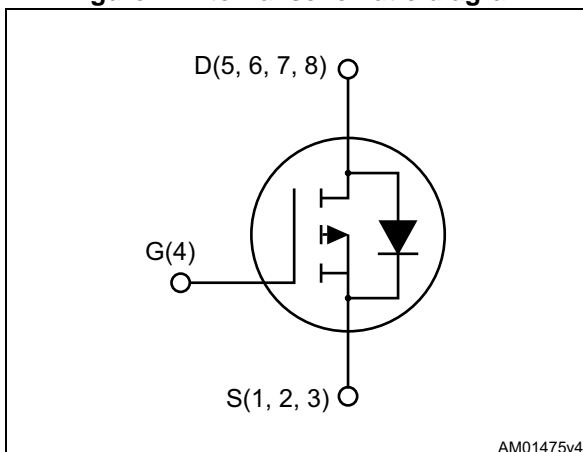


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS}$	$R_{DS(on)max}$	$I_D$
STL12P6F6	60 V	0.16 $\Omega$ @ 10 V	12 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits a very low  $R_{DS(on)}$  in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL12P6F6	12P6F6	PowerFLAT 5x6	Tape and reel

*Note:* For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.5	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	48	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	2.8	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	75	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
$T_j$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. The value is according to  $R_{thj-case}$
2. Pulse width is limited by safe operating area.
3. The value is according to  $R_{thj-pcb}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of  $15\text{ mm}^2$ , 2 Oz Cu,  $t < 10\text{ sec}$

**Note:** For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified).

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA	60			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0, V <sub>DS</sub> = 60 V			1	μA
		V <sub>GS</sub> = 0, V <sub>DS</sub> = 60 V, T <sub>C</sub> = 125 °C			10	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0, V <sub>GS</sub> = ± 20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		0.13	0.16	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 48 V, f = 1 MHz	-	340	-	pF
C <sub>oss</sub>	Output capacitance		-	40	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	20	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14</a> )	-	6.4	-	nC
Q <sub>gs</sub>	Gate-source charge		-	1.7	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	1.7	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 48 V, I <sub>D</sub> = 1.5 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13</a> )	-	64	-	ns
t <sub>r</sub>	Rise time		-	5.3	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	14	-	ns
t <sub>f</sub>	Fall time		-	3.7	-	ns

*Note:* For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 3 \text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	20		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 16 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	17.8		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15</a> )	-	1.8		A

1. Pulse width limited by safe operating area.

2. Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

*Note:* For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

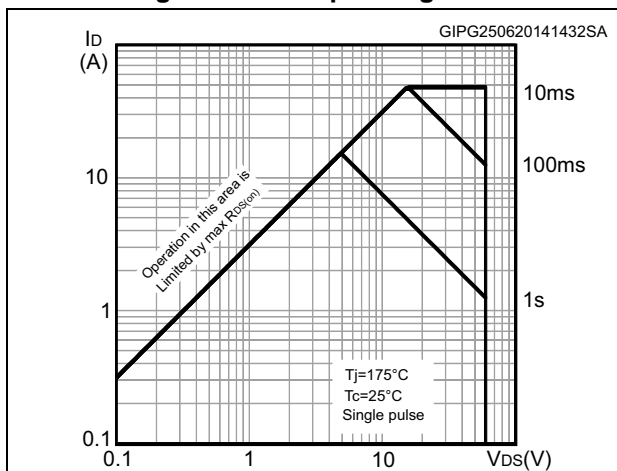


Figure 3. Thermal impedance

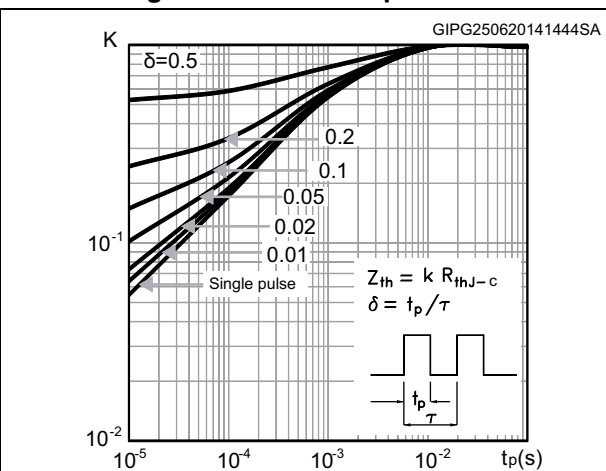


Figure 4. Output characteristics

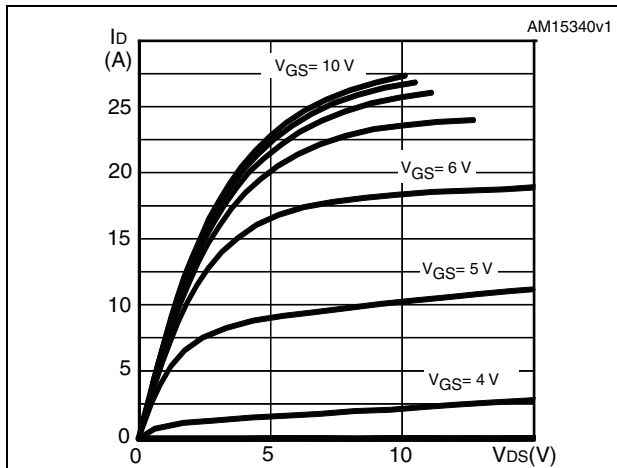


Figure 5. Transfer characteristics

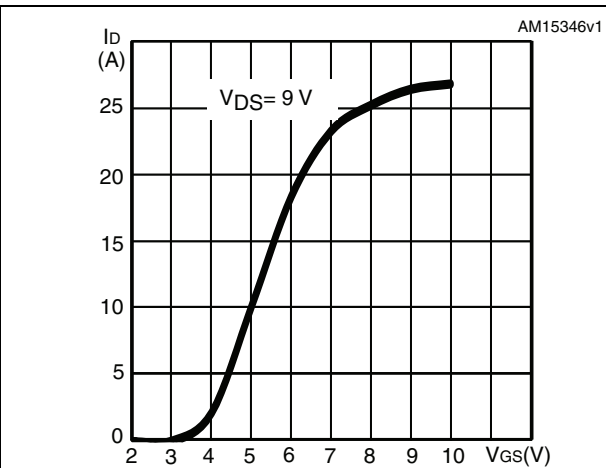


Figure 6. Gate charge vs gate-source voltage

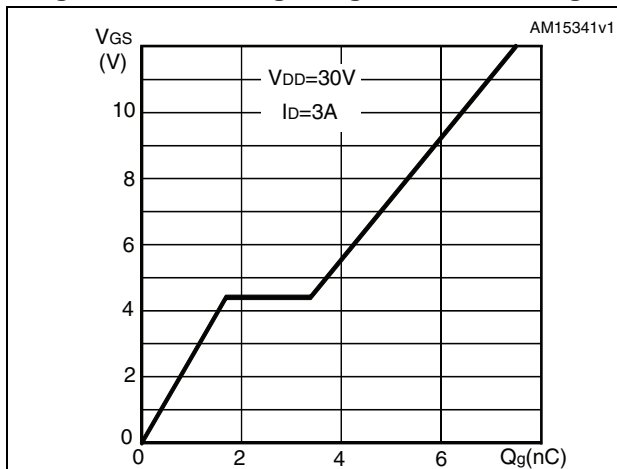


Figure 7. Static drain-source on-resistance

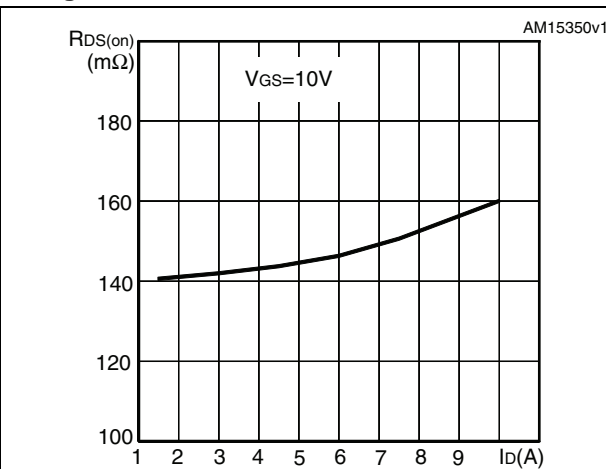


Figure 8. Capacitance variations

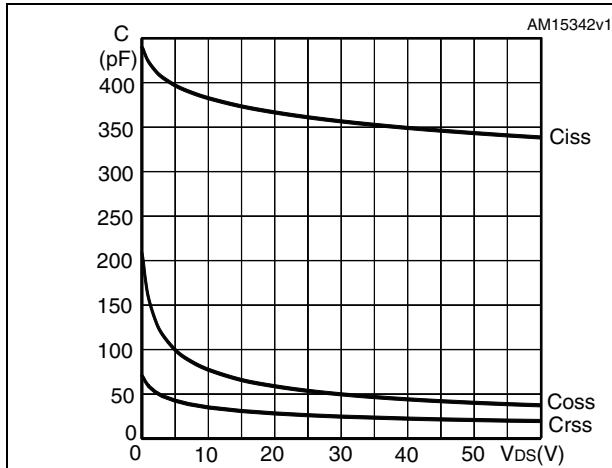


Figure 9. Normalized  $V_{(BR)DSS}$  vs temperature

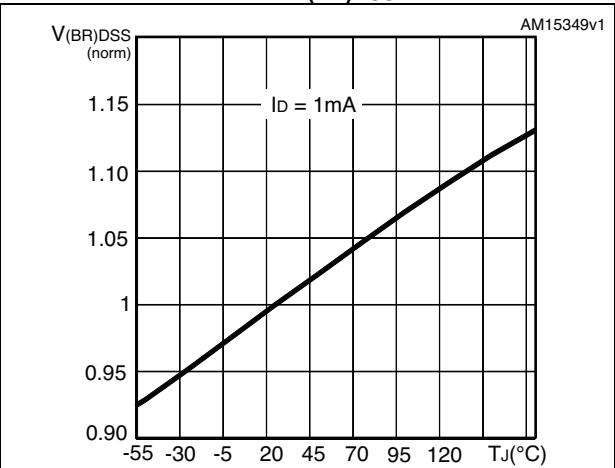


Figure 10. Normalized gate threshold voltage vs temperature

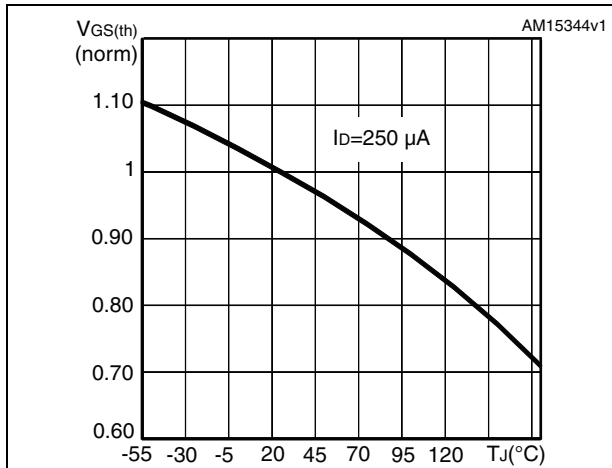


Figure 11. Normalized on-resistance vs temperature

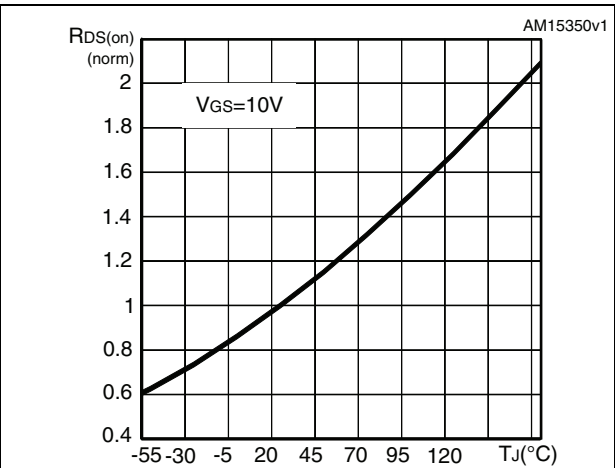
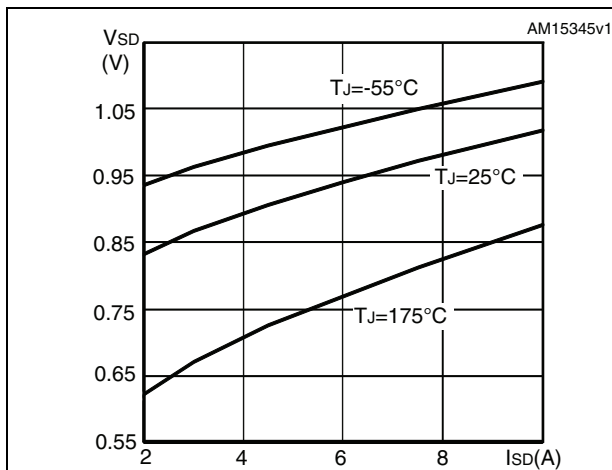
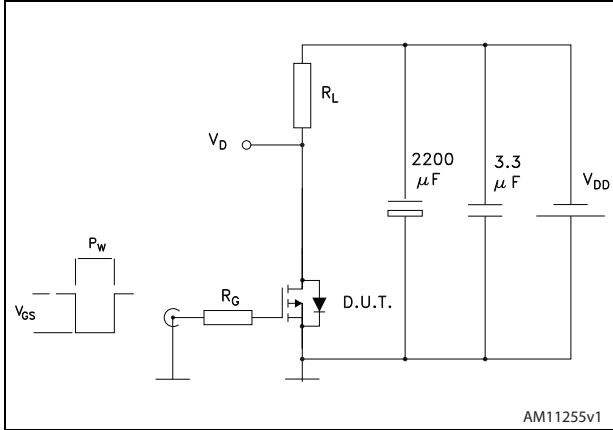


Figure 12. Source-drain diode forward characteristics

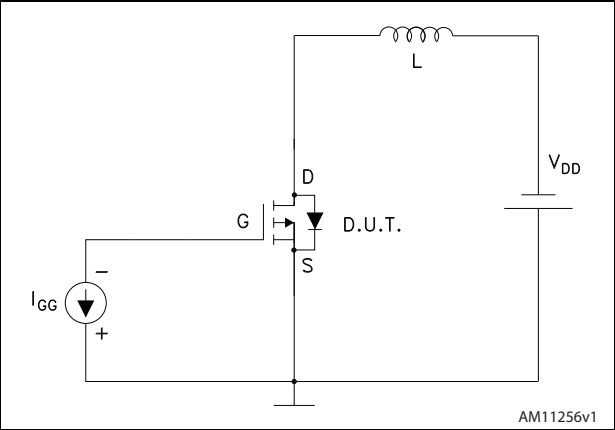


### 3 Test circuits

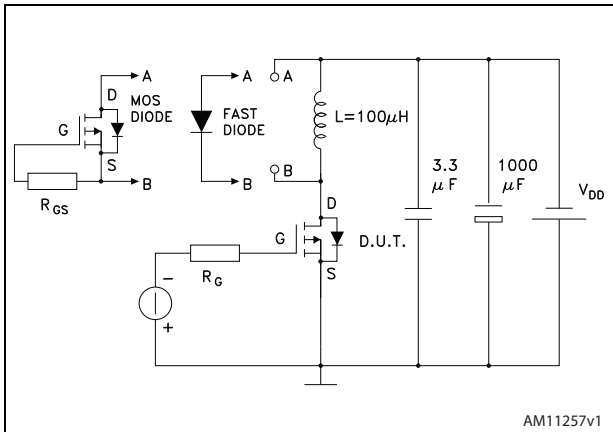
**Figure 13. Switching times test circuit for resistive load**



**Figure 14. Gate charge test circuit**



**Figure 15. Test circuit for inductive load switching and diode recovery times**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 16. PowerFLAT™ 5x6 type S-R drawing

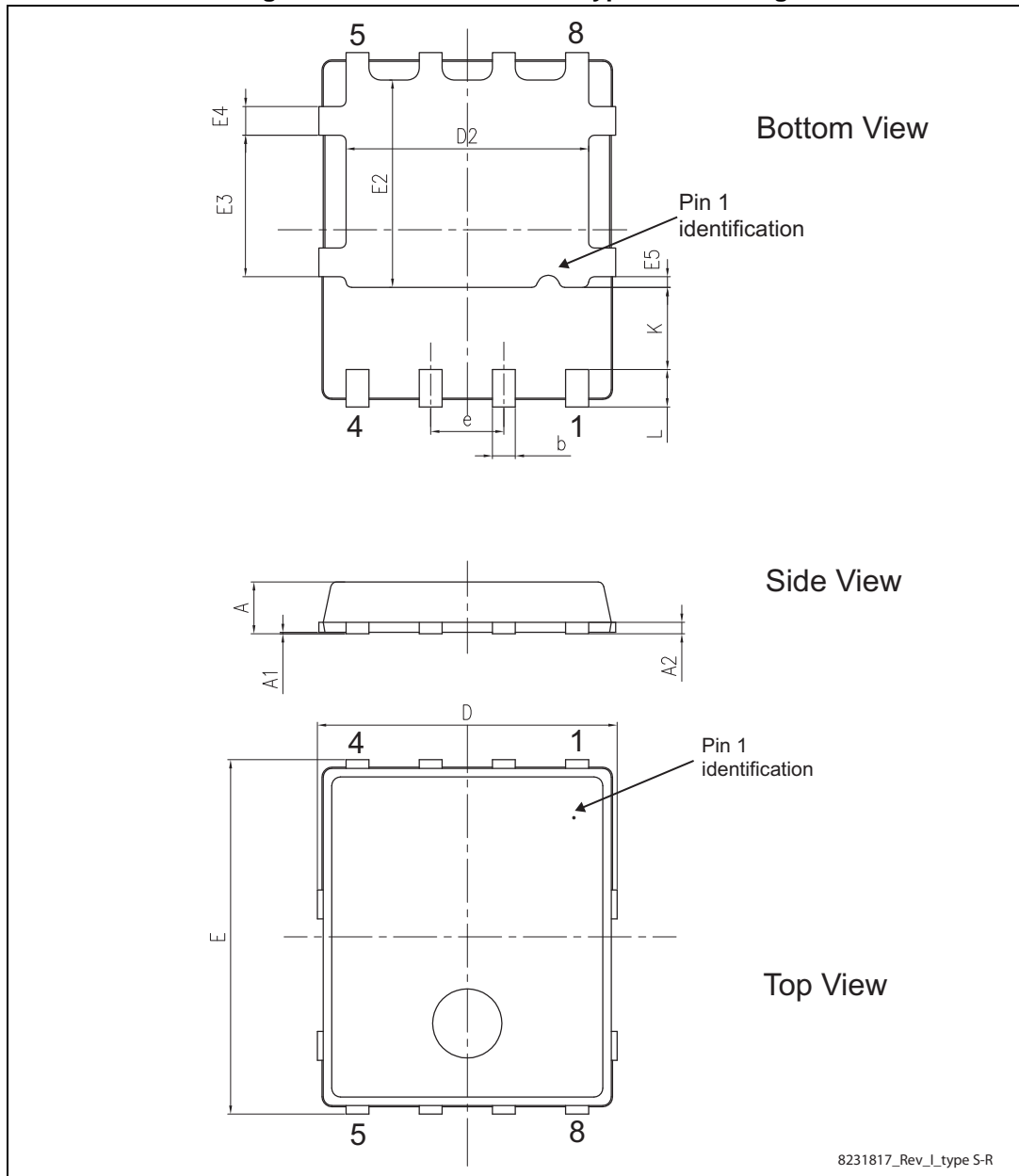
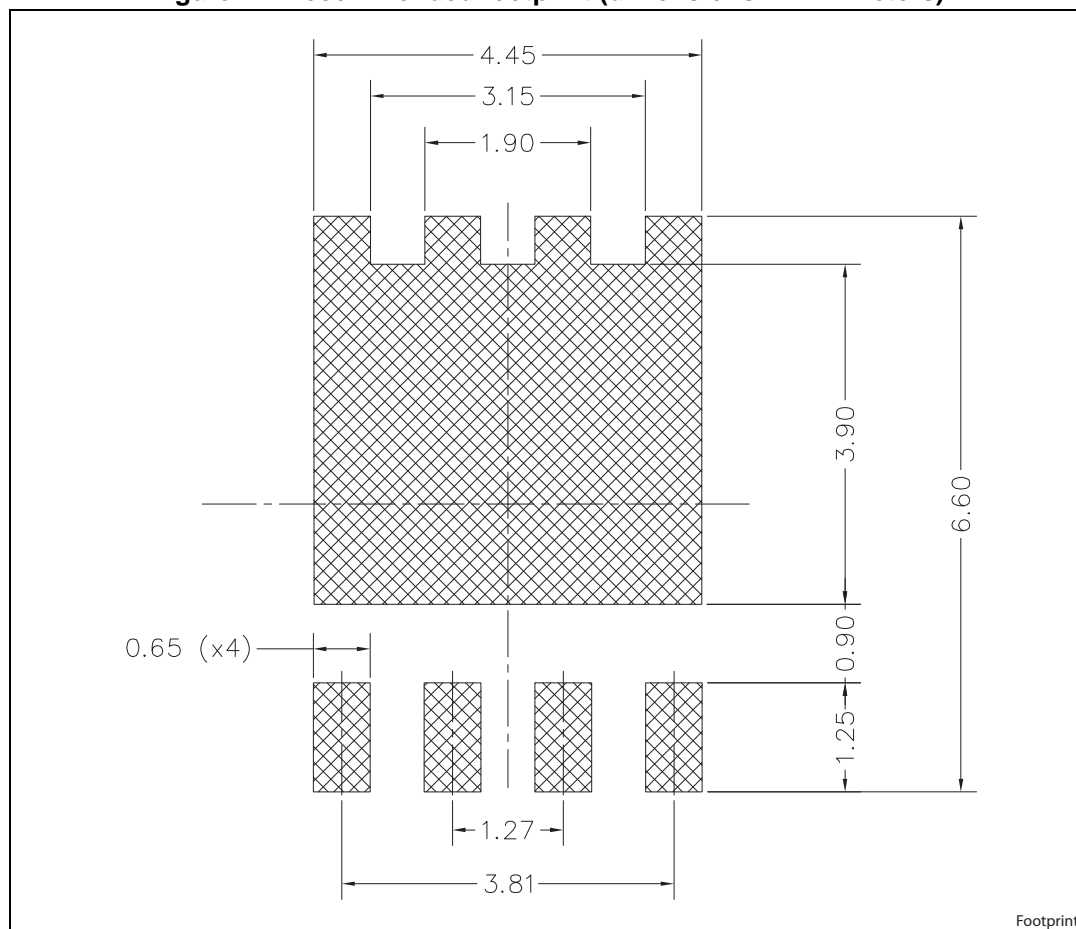


Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	4.11		4.31
E	5.95	6.15	6.35
e		1.27	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.275		1.575
L	0.60		0.80

Figure 17. Recommended footprint (dimensions in millimeters)



# 5 Packaging mechanical data

Figure 18. PowerFLAT™ 5x6 tape<sup>(a)</sup>

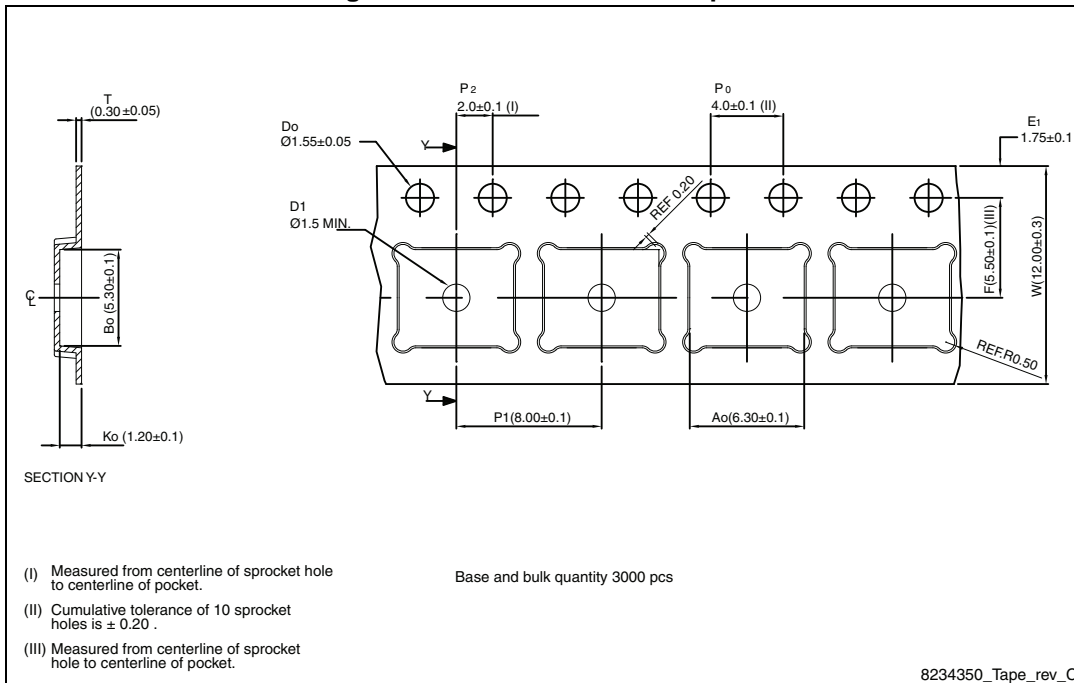
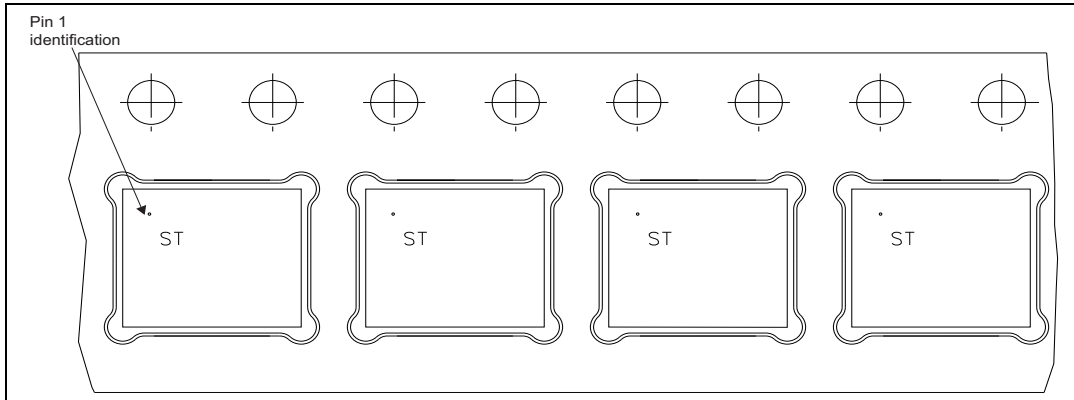
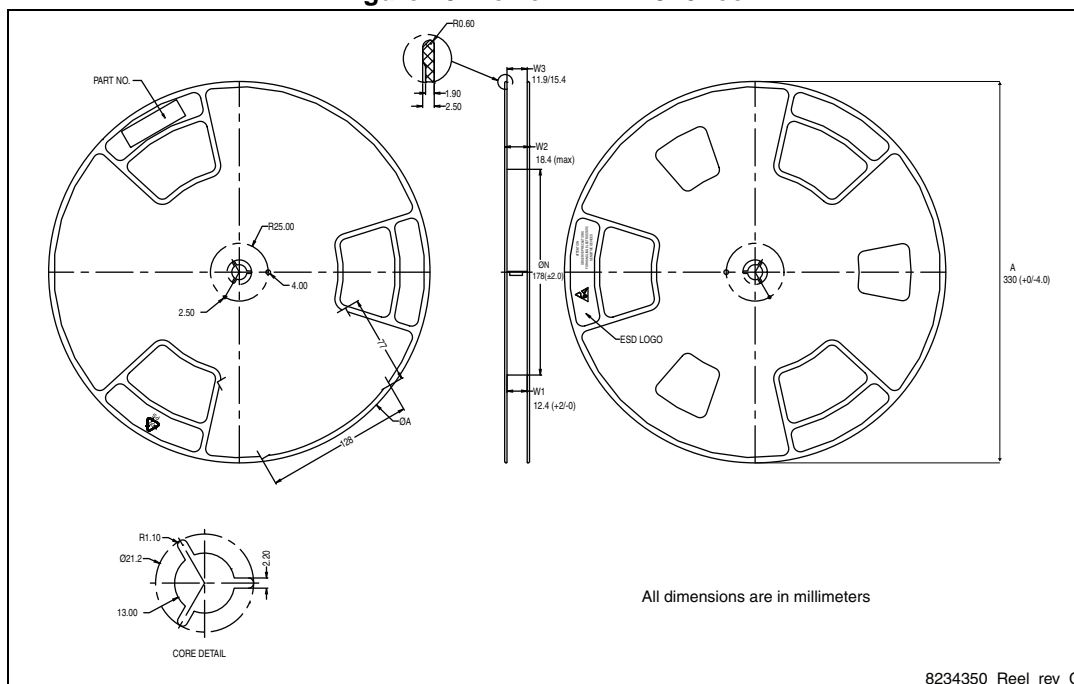


Figure 19. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 20. PowerFLAT™ 5x6 reel



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-Mar-2013	1	First release.
14-Jul-2014	2	<ul style="list-style-type: none"><li>– Modified: <math>I_D</math> and <math>I_{DM}</math> values in <a href="#">Table 2</a></li><li>– Modified: the entire typical values in <a href="#">Table 6</a></li><li>– Modified: <math>I_{SD}</math> and <math>I_{SDM}</math> max values in <a href="#">Table 7</a></li><li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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