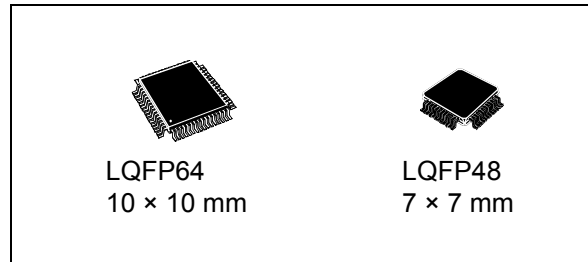


Medium-density USB access line, ARM<sup>®</sup>-based 32-bit MCU with 64/128KB Flash, USB FS, 6 timers, ADC & 8 com. interfaces

Datasheet - production data

## Features

- Core: ARM<sup>®</sup> 32-bit Cortex<sup>®</sup>-M3 CPU
  - 48 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 WS memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 64 or 128 Kbytes of Flash memory
  - 10 or 16 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V<sub>BAT</sub> supply for RTC and backup registers
- Debug mode
  - Serial wire debug (SWD) and JTAG interfaces
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I<sup>2</sup>Cs and USARTs
- 1 × 12-bit, 1.2 μs A/D converter (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- Up to 51 fast I/O ports
  - 37/51 I/Os all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



- Up to 6 timers
  - Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: 24-bit downcounter
- Up to 8 communication interfaces
  - Up to 2 × I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 SPIs (12 Mbit/s)
  - One USB 2.0 full speed interface
- CRC calculation unit, 96-bit unique ID
- ECOPACK<sup>®</sup> packages

**Table 1. Device summary**

Reference	Part number
STM32F102x8	STM32F102C8, STM32F102R8
STM32F102xB	STM32F102CB, STM32F102RB

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x8 and STM32F102xB medium-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the Cortex<sup>®</sup>-M3 core please refer to the Cortex<sup>®</sup>-M3 Technical Reference Manual, available from the ARM<sup>®</sup> website.



## 2 Description

The STM32F102xx medium-density USB access line incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory of 64 or 128 Kbytes and SRAM of 10 or 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I<sup>2</sup>Cs, two SPIs, one USB and three USARTs), one 12-bit ADC and three general-purpose 16-bit timers.

The STM32F102xx family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F102xx medium-density USB access line is delivered in the LQFP48 7 × 7 mm and LQFP64 10 × 10 mm packages.

The STM32F102xx medium-density USB access line microcontrollers are suitable for a wide range of applications.

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

*Figure 1* shows the general block diagram of the device family.

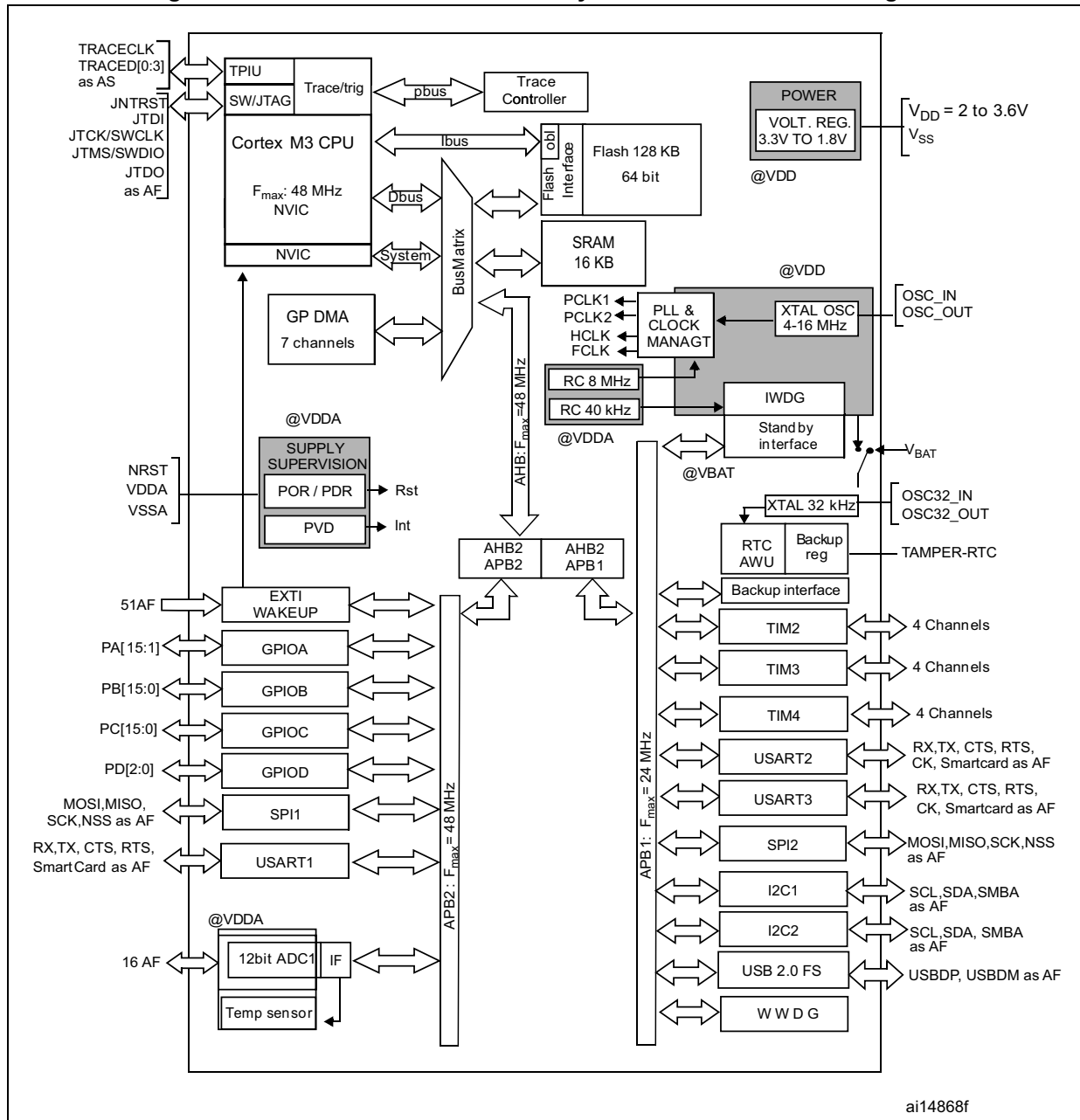


## 2.1 Device overview

Table 2. STM32F102x8 and STM32F102xB medium-density USB access line features and peripheral counts

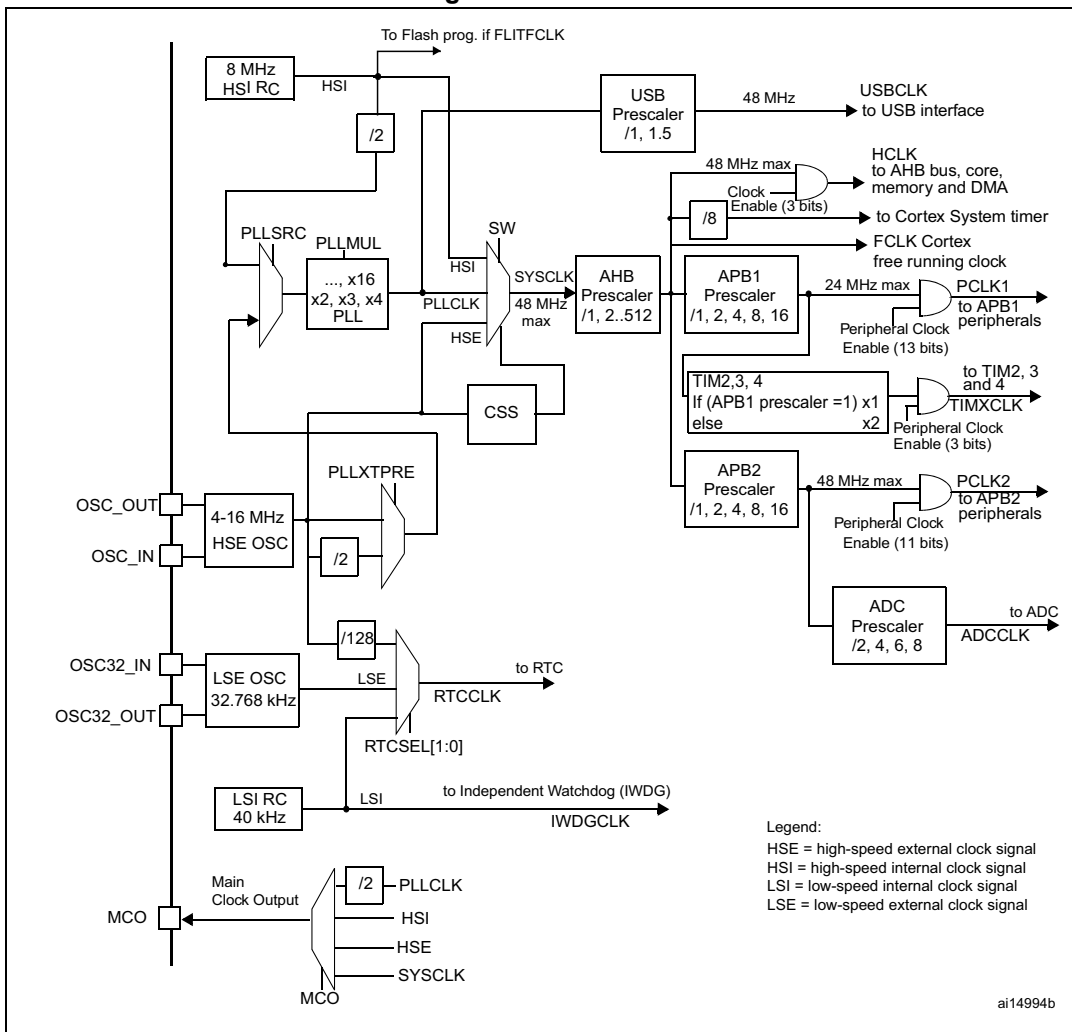
Peripheral		STM32F102Cx		STM32F102Rx	
Flash - Kbytes		64	128	64	128
SRAM - Kbytes		10	16	10	16
Timers	General-purpose	3	3	3	3
Communication interfaces	SPI	2	2	2	2
	I <sup>2</sup> C	2	2	2	2
	USART	3	3	3	3
	USB	1	1	1	1
12-bit synchronized ADC number of channels		1 10 channels		1 16 channels	
GPIOs		37		51	
CPU frequency		48 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperatures		Ambient temperature: -40 to +85 °C (see <a href="#">Table 8</a> ) Junction temperature: -40 to +105 °C (see <a href="#">Table 8</a> )			
Packages		LQFP48		LQFP64	

Figure 1. STM32F102T8 medium-density USB access line block diagram



1. AF = alternate function on I/O port pin.
2.  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  (junction temperature up to  $105\text{ }^\circ\text{C}$ ).

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the USB clock output (USBCLK) at 48 MHz.
2. To have an ADC conversion time of 1.2 μs, APB2 must be at 12 MHz, 24 MHz or 48 MHz.
3. The Flash memory programming interface clock (FLITFCLK) is always the HSI clock.

## 2.2 Full compatibility throughout the family

The STM32F102xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F102x4 and STM32F102x6 are referred to as low-density devices and the STM32F102x8 and STM32F102xB are referred to as medium-density devices.

Low-density devices are an extension of the STM32F102x8/B devices, they are specified in the STM32F102x4/6 datasheet. Low-density devices feature lower Flash memory and RAM capacities, a timer and a few communication interfaces less.

The STM32F102x4 and STM32F102x6 are a drop-in replacement for the STM32F102x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover the STM32F102xx family is fully compatible with all existing STM32F101xx access line and STM32F103xx performance line devices.

**Table 3. STM32F102xx USB access line family**

Pinout	Low-density STM32F102xx devices		Medium-density STM32F102xx devices	
	16 KB Flash	32 KB Flash <sup>(1)</sup>	64 KB Flash	128 KB Flash
	4 KB RAM	6 KB RAM	10 KB RAM	16 KB RAM
64	2 × USARTs, 2 × 16-bit timers		3 × USARTs, 3 × 16-bit timers	
48	1 × SPI, 1 × I <sup>2</sup> C, 1 × ADC, 1 × USB		2 × SPIs, 2 × I <sup>2</sup> Cs, 1 × ADC, 1 × USB	
36	-	-	2 × USARTs, 3 × 16-bit timers 1 × SPI, 1 × I <sup>2</sup> C, 1 × ADC, 1 × USB	-

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F102x8/B medium-density devices.

## 2.3 Overview

### ARM<sup>®</sup> Cortex<sup>®</sup>-M3 core with embedded Flash and SRAM

The ARM<sup>®</sup> Cortex<sup>®</sup>-M3 processor is the latest generation of ARM<sup>®</sup> processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM<sup>®</sup> Cortex<sup>®</sup>-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM<sup>®</sup> core in the memory size usually associated with 8- and 16-bit devices.

The STM32F102xx medium-density USB access line having an embedded ARM<sup>®</sup> core is therefore compatible with all ARM<sup>®</sup> tools and software.

### Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

### CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### Embedded SRAM

10 or 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### Nested vectored interrupt controller (NVIC)

The STM32F102xx medium-density USB access line embeds a nested vectored interrupt controller able to handle up to 36 maskable interrupt channels (not including the 16 interrupt lines of Cortex<sup>®</sup>-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detectors lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect external line with pulse width lower than the Internal APB2 clock period. Up to 51 GPIOs are connected to the 16 external interrupt lines.

### Clocks and startup

System clock selection is performed on startup. however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 48 MHz. See [Figure 2](#) for details on the clock tree.

### Boot modes

At startup, boot pins are used to select one of five boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

### Power supply schemes

- $V_{DD} = 2.0$  to  $3.6$  V: External power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 2.0$  to  $3.6$  V: External analog power supplies for ADC. Reset blocks, RCs and PLL (minimum voltage to be applied to  $V_{DDA}$  is  $2.4$  V when the ADC is used).  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.
- $V_{BAT} = 1.8$  to  $3.6$  V: Power supply for RTC, external clock  $32$  kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

For more details on how to connect power pins, refer to [Figure 8: Power supply scheme](#).

### Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to  $2$  V. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to [Table 10: Embedded reset and power control block characteristics](#) for the values of  $V_{POR/PDR}$  and  $V_{PVD}$ .

### Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

### Low-power modes

The STM32F102xx medium-density USB access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.
- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and registers content are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note:* The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

### DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I<sup>2</sup>C, USART, general purpose timers TIMx and ADC.

### RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V<sub>DD</sub> supply when present or through the V<sub>BAT</sub> pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V<sub>DD</sub> power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare

register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

### General-purpose timers (TIMx)

There are 3 synchronizable general-purpose timers embedded in the STM32F102xx medium-density USB access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one-pulse mode output. This gives up to 12 input captures / output compares / PWMs on the LQFP48 and LQFP64 packages. The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode.

Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

### I<sup>2</sup>C bus

Two I<sup>2</sup>C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes. They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.



### **Universal synchronous/asynchronous receiver transmitter (USART)**

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

### **Serial peripheral interface (SPI)**

Two SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

### **Universal serial bus (USB)**

The STM32F102xx medium-density USB access line embeds an USB device peripheral compatible with the USB Full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

### **GPIOs (general-purpose inputs/outputs)**

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

### **ADC (analog to digital converter)**

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

### **Temperature sensor**

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between  $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$ . The temperature sensor is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### **Serial wire JTAG debug port (SWJ-DP)**

The ARM<sup>®</sup> SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 3 Pinout and pin description

Figure 3. STM32F102xx medium-density USB access line LQFP48 pinout

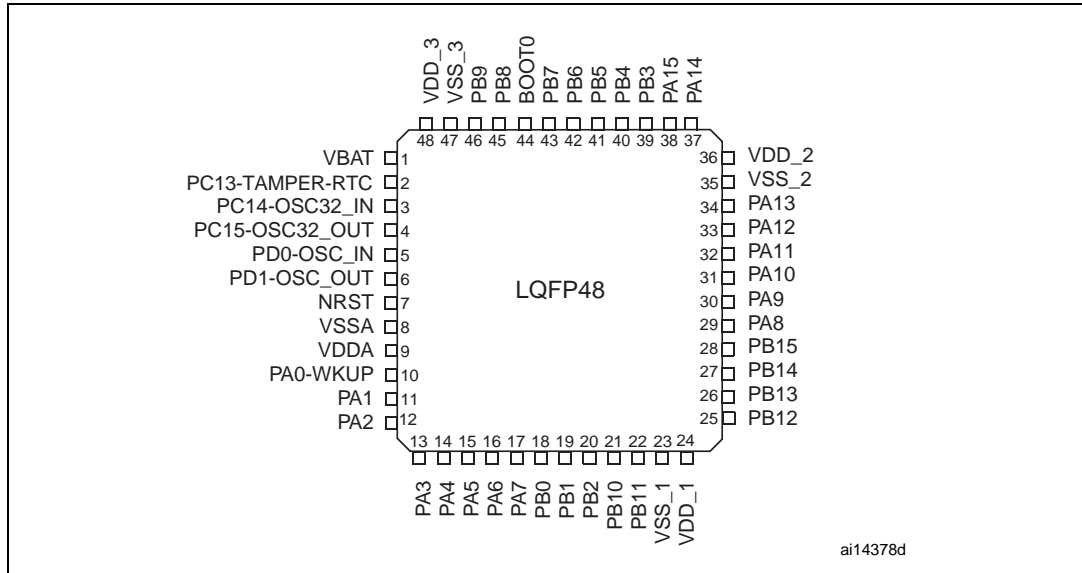


Figure 4. STM32F102xx medium-density USB access line LQFP64 pinout

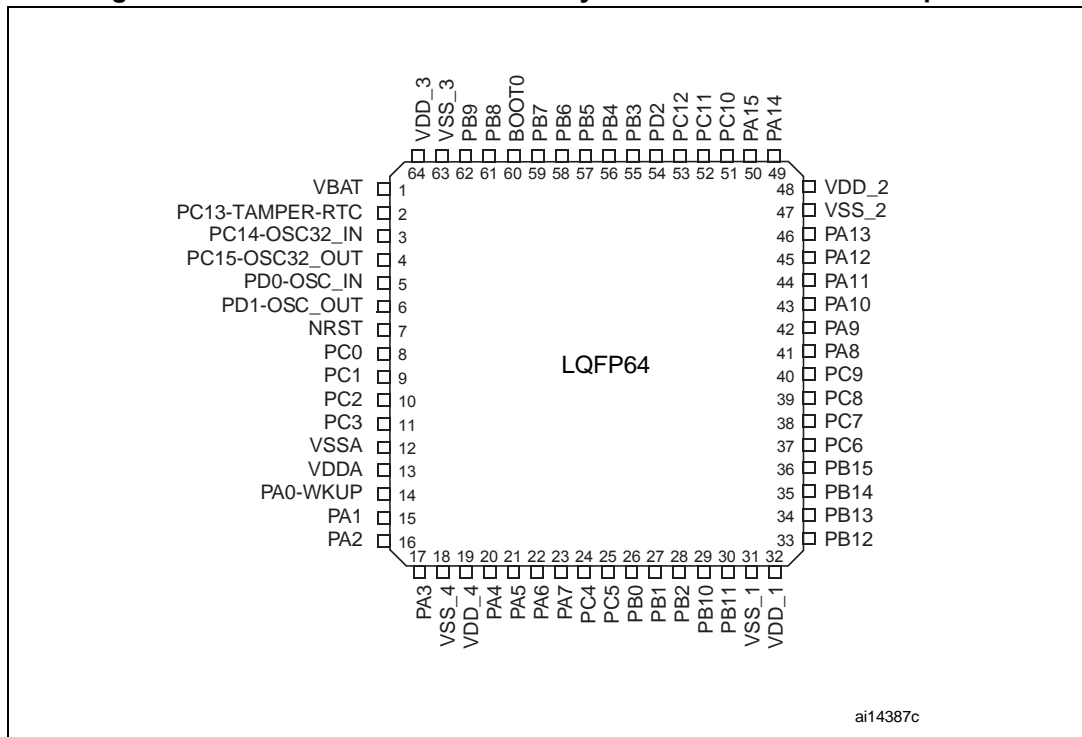


Table 4. Medium-density STM32F102xx pin definitions

Pins		Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3) (4)</sup>	
LQFP48	LQFP64					Default	Remap
1	1	V <sub>BAT</sub>	S	-	V <sub>BAT</sub>	-	-
2	2	PC13-TAMPER-RTC <sup>(5)</sup>	I/O	-	PC13 <sup>(6)</sup>	TAMPER-RTC	-
3	3	PC14-OSC32_IN <sup>(5)</sup>	I/O	-	PC14 <sup>(6)</sup>	OSC32_IN	-
4	4	PC15-OSC32_OUT <sup>(5)</sup>	I/O	-	PC15 <sup>(6)</sup>	OSC32_OUT	-
5	5	OSC_IN	I/O	FT	OSC_IN	-	PD0 <sup>(7)</sup>
6	6	OSC_OUT	I/O	FT	OSC_OUT	-	PD1 <sup>(7)</sup>
7	7	NRST	I/O	-	NRST	-	-
-	8	PC0	I/O	-	PC0	ADC_IN10	-
-	9	PC1	I/O	-	PC1	ADC_IN11	-
-	10	PC2	I/O	-	PC2	ADC_IN12	-
-	11	PC3	I/O	-	PC3	ADC_IN13	-
8	12	V <sub>SSA</sub>	S	-	V <sub>SSA</sub>	-	-
9	13	V <sub>DDA</sub>	S	-	V <sub>DDA</sub>	-	-
10	14	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC_IN0/ TIM2_CH1_ETR <sup>(8)</sup>	-
11	15	PA1	I/O	-	PA1	USART2_RTS/ ADC_IN1/TIM2_CH2 <sup>(8)</sup>	-
12	16	PA2	I/O	-	PA2	USART2_TX/ ADC_IN2/TIM2_CH3 <sup>(8)</sup>	-
13	17	PA3	I/O	-	PA3	USART2_RX/ ADC_IN3/TIM2_CH4 <sup>(8)</sup>	-
-	18	V <sub>SS_4</sub>	S	-	V <sub>SS_4</sub>	-	-
-	19	V <sub>DD_4</sub>	S	-	V <sub>DD_4</sub>	-	-
14	20	PA4	I/O	-	PA4	SPI1_NSS <sup>(8)</sup> /ADC_IN4 USART2_CK/	-
15	21	PA5	I/O	-	PA5	SPI1_SCK <sup>(8)</sup> /ADC_IN5	-
16	22	PA6	I/O	-	PA6	SPI1_MISO <sup>(8)</sup> /ADC_IN6/ TIM3_CH1 <sup>(8)</sup>	-
17	23	PA7	I/O	-	PA7	SPI1_MOSI <sup>(8)</sup> /ADC_IN7/ TIM3_CH2 <sup>(8)</sup>	-
-	24	PC4	I/O	-	PC4	ADC_IN14	-
-	25	PC5	I/O	-	PC5	ADC_IN15	-
18	26	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3 <sup>(8)</sup>	-
19	27	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4 <sup>(8)</sup>	-

Table 4. Medium-density STM32F102xx pin definitions (continued)

Pins		Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3) (4)</sup>	
LQFP48	LQFP64					Default	Remap
20	28	PB2	I/O	FT	PB2/BOOT1	-	-
21	29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX <sup>(8)</sup>	TIM2_CH3
22	30	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX <sup>(8)</sup>	TIM2_CH4
23	31	V <sub>SS_1</sub>	S	-	V <sub>SS_1</sub>	-	-
24	32	V <sub>DD_1</sub>	S	-	V <sub>DD_1</sub>	-	-
25	33	PB12	I/O	FT	PB12	SPI2_NSS / I2C2_SMBA/ USART3_CK <sup>(8)</sup>	-
26	34	PB13	I/O	FT	PB13	SPI2_SCK <sup>(8)</sup> / USART3_CTS	-
27	35	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS	-
28	36	PB15	I/O	FT	PB15	SPI2_MOSI	-
-	37	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	PA9	I/O	FT	PA9	USART1_TX <sup>(8)</sup>	-
31	43	PA10	I/O	FT	PA10	USART1_RX <sup>(8)</sup>	-
32	44	PA11	I/O	FT	PA11	USART1_CTS/USB_DM	-
33	45	PA12	I/O	FT	PA12	USART1_RTS/USB_DP	-
34	46	PA13	I/O	FT	JTMS- SWDIO	-	PA13
35	47	V <sub>SS_2</sub>	S	-	V <sub>SS_2</sub>	-	-
36	48	V <sub>DD_2</sub>	S	-	V <sub>DD_2</sub>	-	-
37	49	PA14	I/O	FT	JTCK/ SWCLK	-	PA14
38	50	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15 /SPI1_NSS
-	51	PC10	I/O	FT	PC10	-	USART3_TX
-	52	PC11	I/O	FT	PC11	-	USART3_RX
-	53	PC12	I/O	FT	PC12	-	USART3_CK
-	54	PD2	I/O	FT	PD2	TIM3_ETR	-

Table 4. Medium-density STM32F102xx pin definitions (continued)

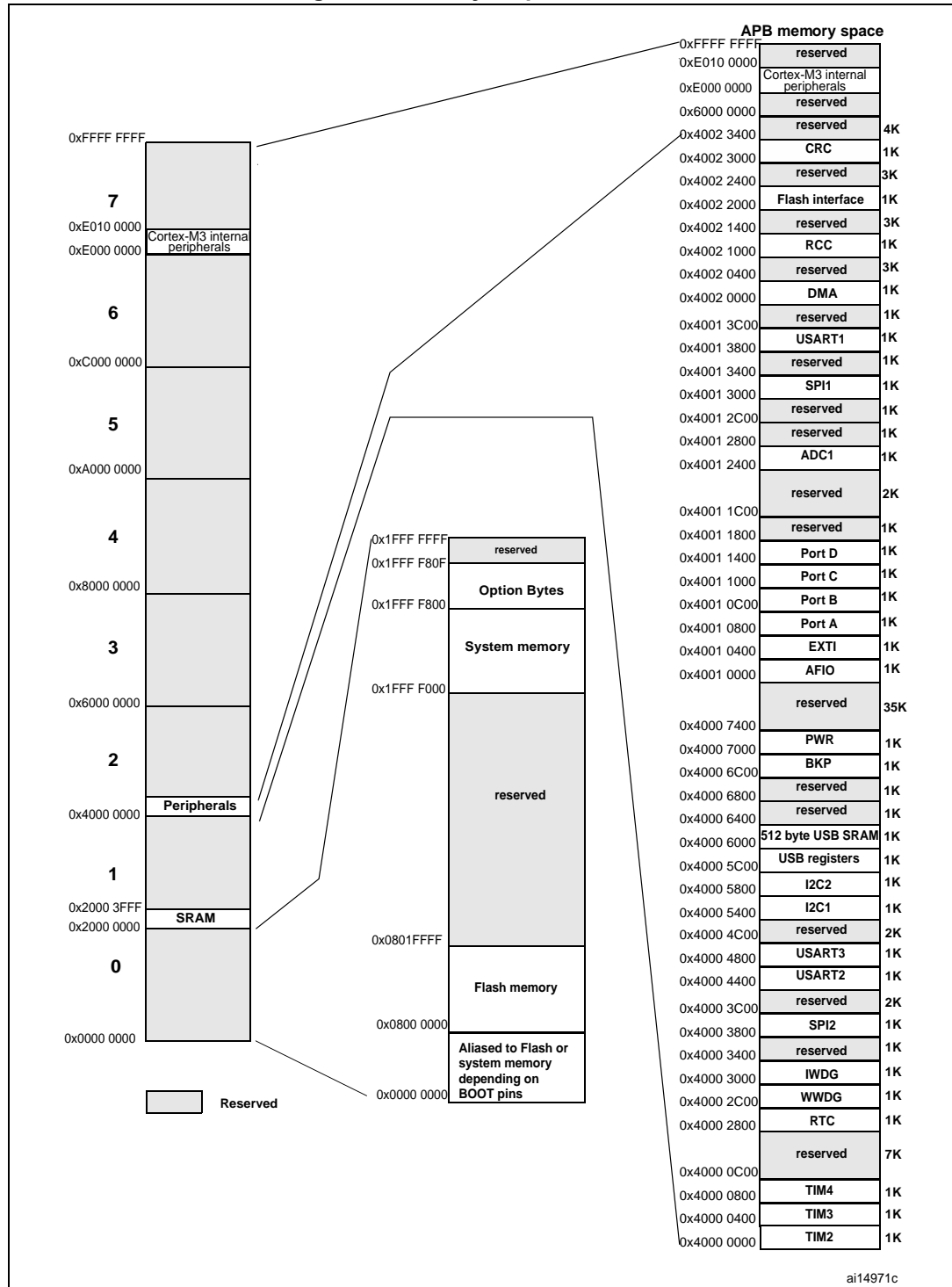
Pins		Pin name	Type <sup>(1)</sup>	I/O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)</sup> (4)	
LQFP48	LQFP64					Default	Remap
39	55	PB3	I/O	FT	JTDO	-	TIM2_CH2/PB3/ TRACESWO/ SPI1_SCK
40	56	PB4	I/O	FT	JNTRST	-	TIM3_CH1 / PB4 SPI1_MISO
41	57	PB5	I/O	-	PB5	I2C1_SMBA	TIM3_CH2 / SPI1_MOSI
42	58	PB6	I/O	FT	PB6	I2C1_SCL <sup>(8)</sup> / TIM4_CH1	USART1_TX
43	59	PB7	I/O	FT	PB7	I2C1_SDA <sup>(8)</sup> / TIM4_CH2	USART1_RX
44	60	BOOT0	I	-	BOOT0	-	-
45	61	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL
46	62	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA
47	63	V <sub>SS_3</sub>	S	-	V <sub>SS_3</sub>	-	-
48	64	V <sub>DD_3</sub>	S	-	V <sub>DD_3</sub>	-	-

1. I = input, O = output, S = supply.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 2 on page 9](#) [Table 3 on page 12](#).
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F102xx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).
7. The pins number 5 and 6 in the LQFP48 package are configured as OSC\_IN/OSC\_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).

# 4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map



## 5 Electrical characteristics

### 5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to  $V_{SS}$ .

#### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ °C}$  and  $T_A = T_{Amax}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\sigma$ ).

#### 5.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ °C}$ ,  $V_{DD} = 3.3\text{ V}$  (for the  $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\sigma$ ).

#### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

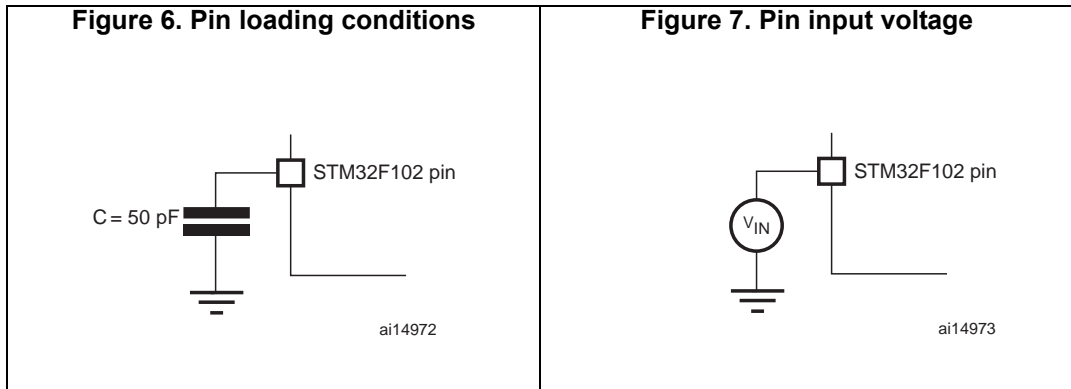
#### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 6](#).

#### 5.1.5 Pin input voltage

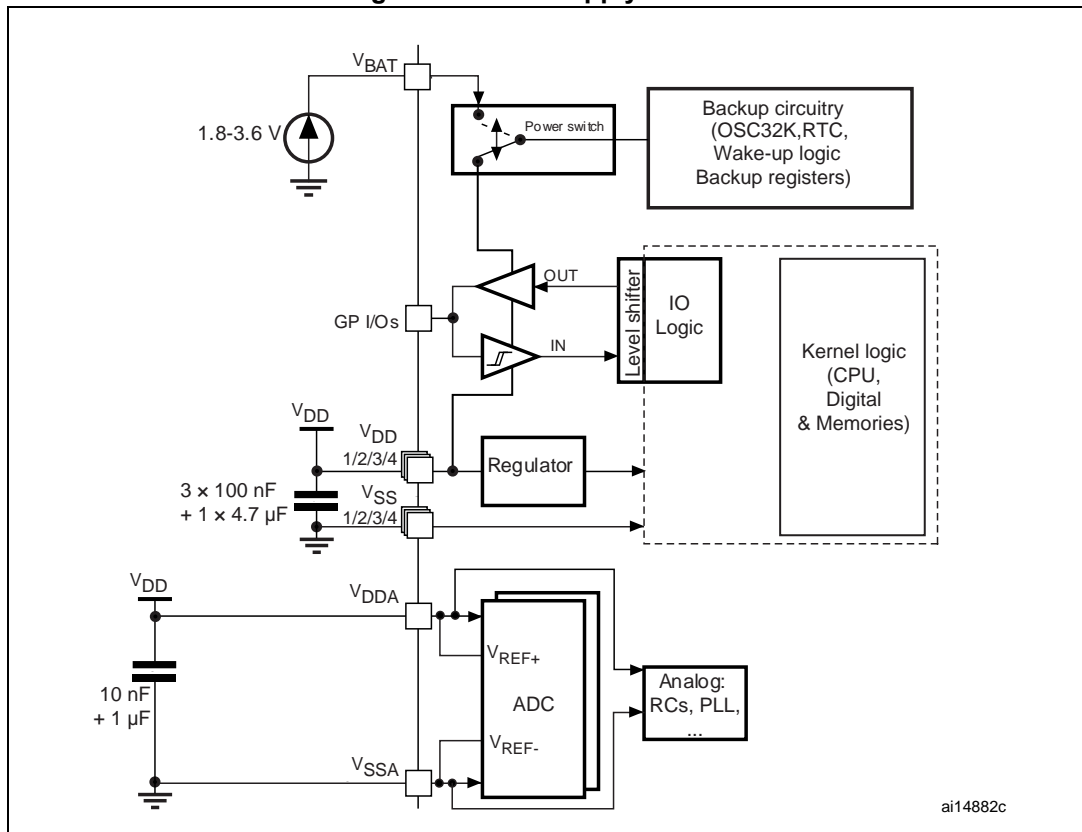
The input voltage measurement on a pin of the device is described in [Figure 7](#).





**5.1.6 Power supply scheme**

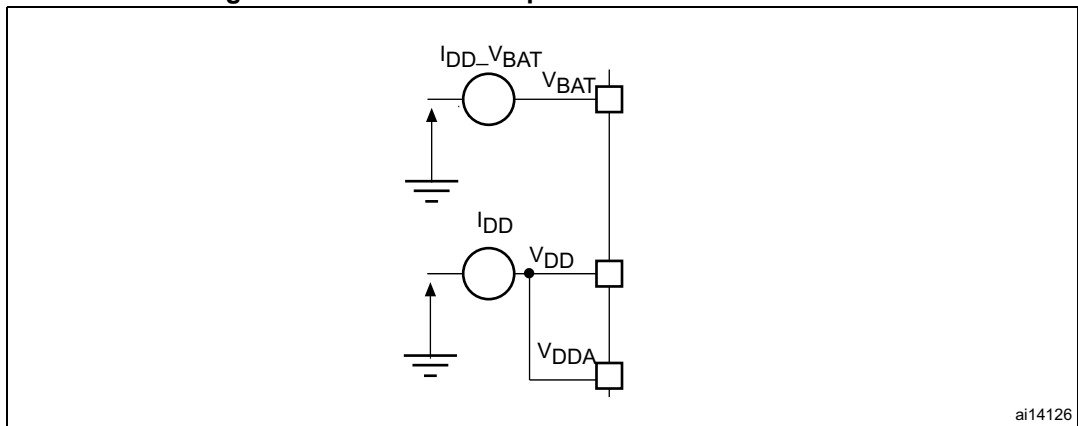
**Figure 8. Power supply scheme**



**Caution:** In [Figure 8](#), the 4.7  $\mu$ F capacitor must be connected to  $V_{DD3}$ .

### 5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 5: Voltage characteristics](#), [Table 6: Current characteristics](#), and [Table 7: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup>	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 5.3.11: Absolute maximum ratings (electrical sensitivity)</a>		

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $V_{IN}$  maximum must always be respected. Refer to [Table 6: Current characteristics](#) for the maximum allowed injected current values.

**Table 6. Current characteristics**

Symbol	Ratings	Max.	Unit
$I_{VDD}$	Total current into $V_{DD}/V_{DDA}$ power lines (source) <sup>(1)</sup>	150	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	150	
$I_{IO}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ <sup>(2)</sup>	Injected current five volt tolerant pins <sup>(3)</sup>	-5/+0	
	Injected current on any other pin <sup>(4)</sup>	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) <sup>(5)</sup>	± 25	

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device.
3. Positive injection is not possible on these I/Os. A negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 5](#) for maximum allowed input voltage values.
4. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 5](#) for maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 7. Thermal characteristics**

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	150	°C

### 5.3 Operating conditions

#### 5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit	
f <sub>HCLK</sub>	Internal AHB clock frequency	-	0	48	MHz	
f <sub>PCLK1</sub>	Internal APB1 clock frequency	-	0	24		
f <sub>PCLK2</sub>	Internal APB2 clock frequency	-	0	48		
V <sub>DD</sub>	Standard operating voltage	-	2	3.6	V	
V <sub>DDA</sub> <sup>(1)</sup>	Analog operating voltage (ADC not used)	Must be the same potential as V <sub>DD</sub> <sup>(2)</sup>	2	3.6	V	
	Analog operating voltage (ADC used)		2.4	3.6		
V <sub>IN</sub>	I/O input voltage	Standard IO	-0.3	V <sub>DD</sub> +0.3	V	
		FTIO <sup>(3)</sup>	2 V < V <sub>DD</sub> ≤ 3.6 V	-0.3		5.5
			V <sub>DD</sub> = 2 V	-0.3		5.2
	BOOT0	0	5.5			
P <sub>D</sub>	Power dissipation at T <sub>A</sub> = 85 °C <sup>(4)</sup>	LQFP48	-	363	mW	
		LQFP64	-	444		
T <sub>A</sub>	Ambient temperature	Maximum power dissipation	-40	85	°C	
		Low power dissipation <sup>(5)</sup>	-40	105	°C	
T <sub>J</sub>	Junction temperature range	-	-40	105	°C	

1. When the ADC is used, refer to [Table 45: ADC characteristics](#).
2. It is recommended to power V<sub>DD</sub> and V<sub>DDA</sub> from the same source. A maximum difference of 300 mV between V<sub>DD</sub> and V<sub>DDA</sub> can be tolerated during power-up and operation.
3. To sustain a voltage higher than V<sub>DD</sub>+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T<sub>A</sub> is lower, higher P<sub>D</sub> values are allowed as long as T<sub>J</sub> does not exceed T<sub>Jmax</sub> (see [Section 6.3: Thermal characteristics](#)).
5. In low power dissipation state, T<sub>A</sub> can be extended to this range as long as T<sub>J</sub> does not exceed T<sub>Jmax</sub> (see [Section 6.3: Thermal characteristics](#)).

#### 5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T<sub>A</sub>.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t <sub>VDD</sub>	V <sub>DD</sub> rise time rate	-	0	∞	μs/V
	V <sub>DD</sub> fall time rate		20	∞	

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 10](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 10. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2.0	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V		
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(1)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(2)}$	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

2. Guaranteed by design, not tested in production.

### 5.3.4 Embedded reference voltage

The parameters given in [Table 11](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT}$	Internal reference voltage	$-40\text{ °C} < T_A < +85\text{ °C}$	1.16	1.20	1.24	V
$T_{S\_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1 <sup>(2)</sup>	$\mu\text{s}$
$V_{RERINT}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V} \pm 10\text{ mV}$	-	-	10	mV
$T_{Coeff}^{(2)}$	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 9: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled  $f_{PCLK1} = f_{HCLK}/2$ ,  $f_{PCLK2} = f_{HCLK}$

The parameters given in [Table 12](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 12. Maximum current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Max <sup>(1)</sup>	Unit
				T <sub>A</sub> = 85 °C	
I <sub>DD</sub>	Supply current in Run mode	External clock <sup>(2)</sup> , all peripherals enabled	48 MHz	36.1	mA
			36 MHz	28.6	
			24 MHz	19.9	
			16 MHz	14.7	
			8 MHz	8.6	
		External clock <sup>(2)</sup> , all peripherals Disabled	48 MHz	24.4	
			36 MHz	19.8	
			24 MHz	13.9	
			16 MHz	10.7	
			8 MHz	6.8	

1. Based on characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

**Table 13. Maximum current consumption in Run mode, code with data processing running from RAM**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Max	Unit
				T <sub>A</sub> = 85 °C <sup>(1)</sup>	
I <sub>DD</sub>	Supply current in Run mode	External clock <sup>(2)</sup> , all peripherals enabled	48 MHz	31.5	mA
			36 MHz	24	
			24 MHz	17.5	
			16 MHz	12.5	
			8 MHz	7.5	
		External clock <sup>(2)</sup> all peripherals disabled	48 MHz	20.5	
			36 MHz	16	
			24 MHz	11.5	
			16 MHz	8.5	
			8 MHz	5.5	

1. Based on characterization, tested in production at V<sub>DD</sub> max, f<sub>HCLK</sub> max.
2. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

Figure 10. Typical current consumption in Run mode versus temperature (at 3.6 V) - code with data processing running from RAM, peripherals enabled

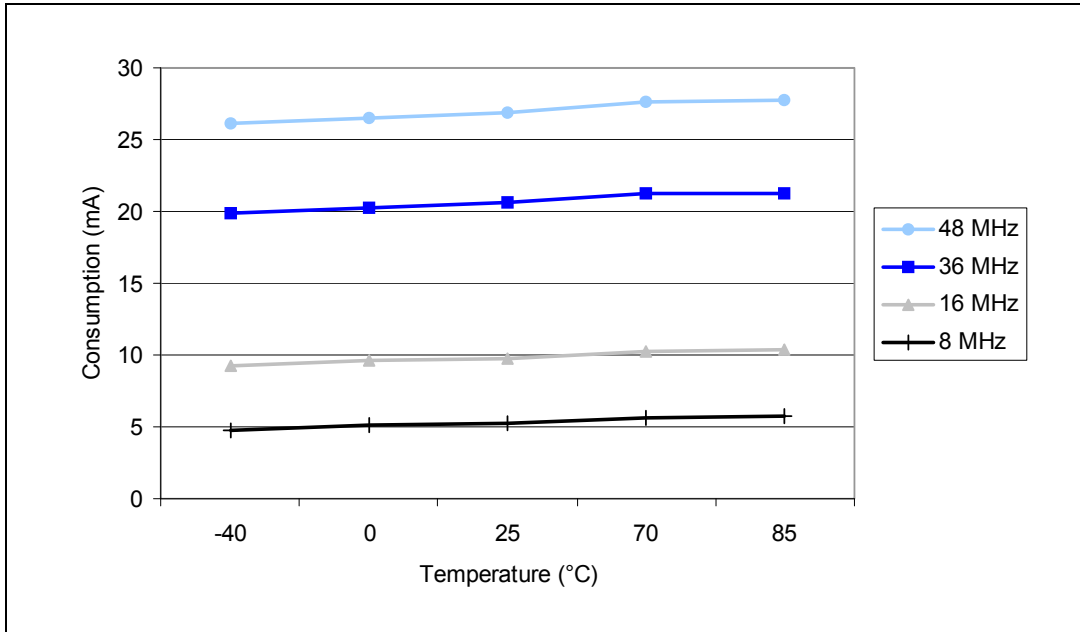
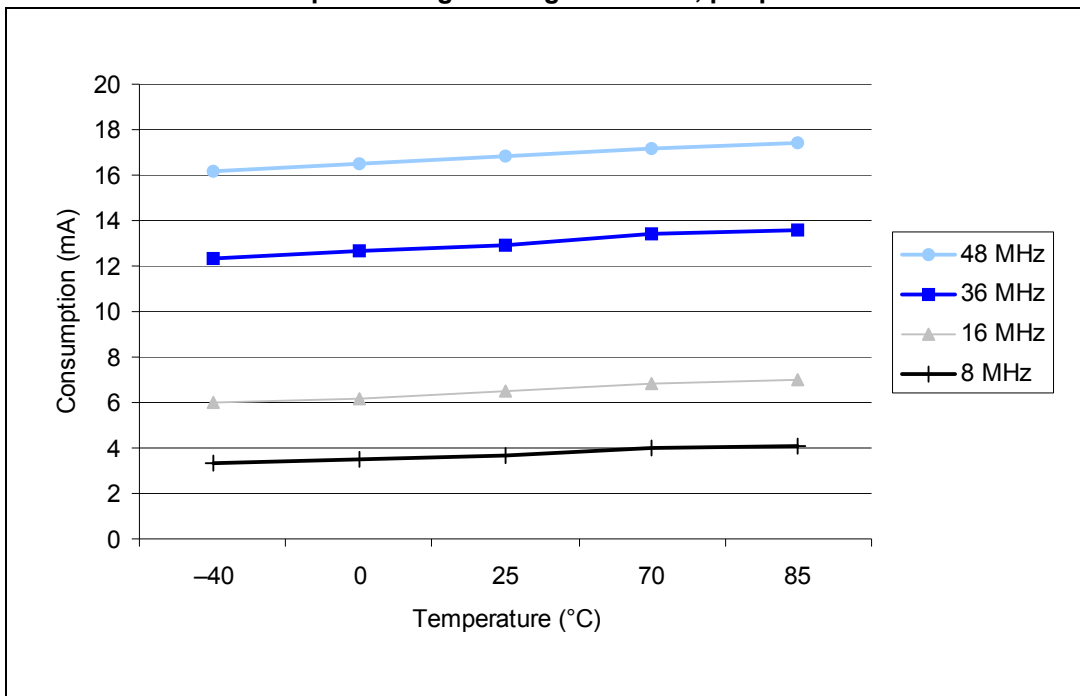


Figure 11. Typical current consumption in Run mode versus temperature (at 3.6 V) - code with data processing running from RAM, peripherals disabled





**Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Max <sup>(1)</sup>	Unit
				T <sub>A</sub> = 85 °C	
I <sub>DD</sub>	Supply current in Sleep mode	External clock <sup>(2)</sup> , all peripherals enabled	48 MHz	20	mA
			36 MHz	15.5	
			24 MHz	11.5	
			16 MHz	8.5	
			8 MHz	5.5	
		External clock <sup>(2)</sup> , all peripherals disabled	48 MHz	6	
			36 MHz	5	
			24 MHz	4.5	
			16 MHz	4	
			8 MHz	3	

1. Based on characterization, tested in production at V<sub>DD</sub> max and f<sub>HCLK</sub> max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

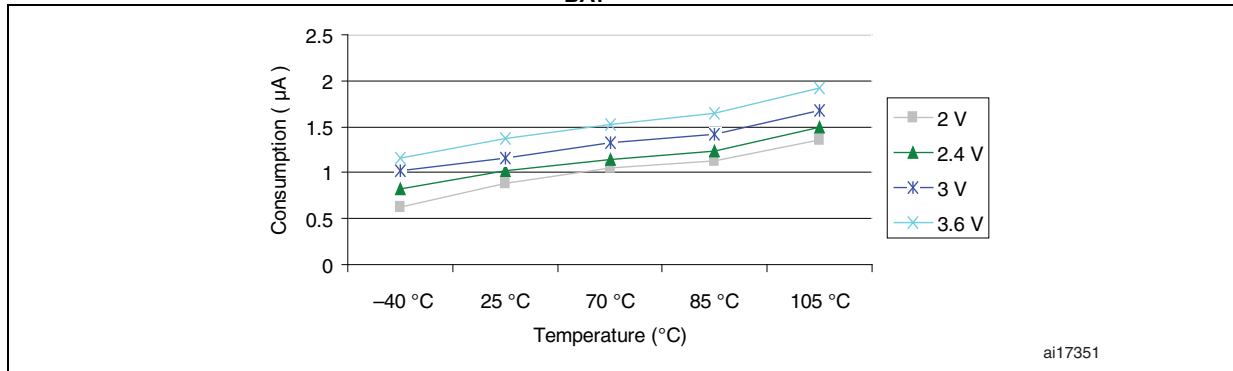
**Table 15. Typical and maximum current consumptions in Stop and Standby modes**

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>			Max	Unit
			V <sub>DD</sub> /V <sub>BAT</sub> = 2.4 V	V <sub>DD</sub> /V <sub>BAT</sub> = 3.3 V	V <sub>DD</sub> /V <sub>BAT</sub> = 2.0 V	T <sub>A</sub> = 85 °C	
I <sub>DD</sub>	Supply current in Stop mode	Regulator in Run mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	23.5	24	-	200	µA
		Regulator in Low Power mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	13.5	14	-	180	
	Supply current in Standby mode <sup>(2)</sup>	Low-speed internal RC oscillator and independent watchdog ON	2.6	3.4	-	-	mA
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.7	2	-	4	
I <sub>DD_VBAT</sub>	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	0.9	1.9 <sup>(3)</sup>	µA

1. Typical values are measured at T<sub>A</sub> = 25 °C.

- To have the Standby consumption with RTC ON, add  $I_{DD\_VBAT}$  (Low-speed oscillator and RTC ON) to  $I_{DD}$  Standby (when  $V_{DD}$  is present the Backup Domain is powered by  $V_{DD}$  supply).
- Based on characterization, not tested in production.

**Figure 12. Typical current consumption on  $V_{BAT}$  with RTC on versus temperature at different  $V_{BAT}$  values**



**Figure 13. Typical current consumption in Stop mode with regulator in Run mode versus temperature at  $V_{DD} = 3.3$  V and 3.6 V**

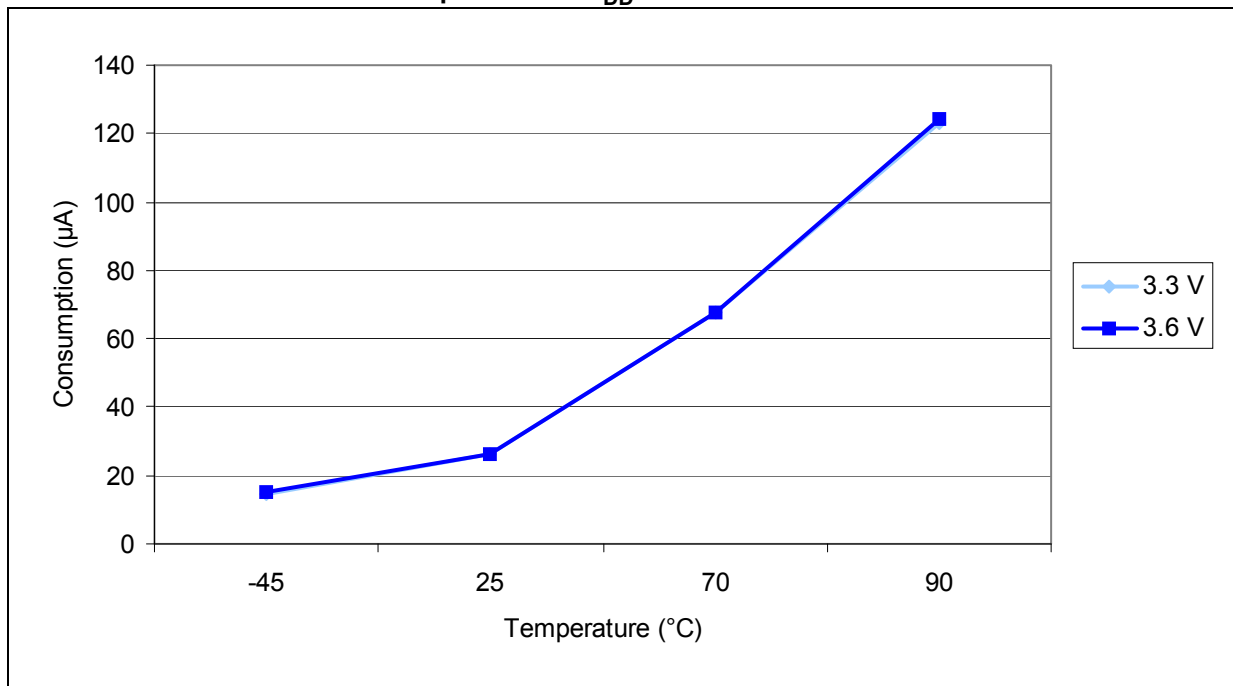


Figure 14. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at  $V_{DD} = 3.3\text{ V}$  and  $3.6\text{ V}$

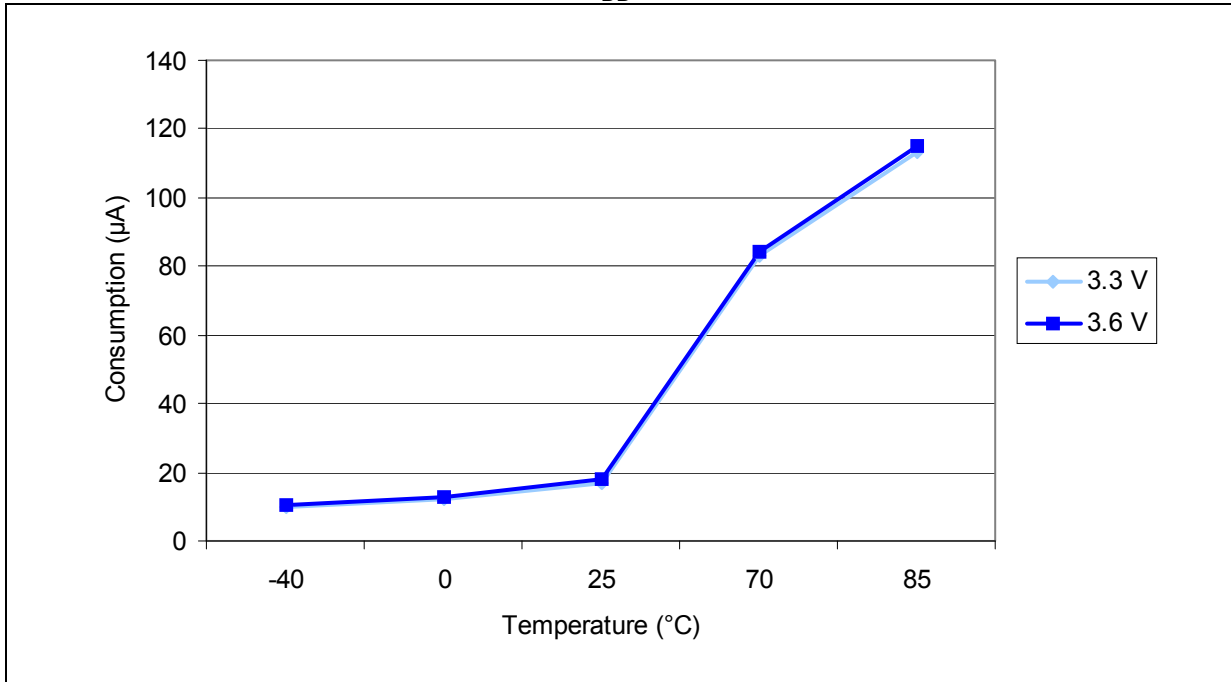
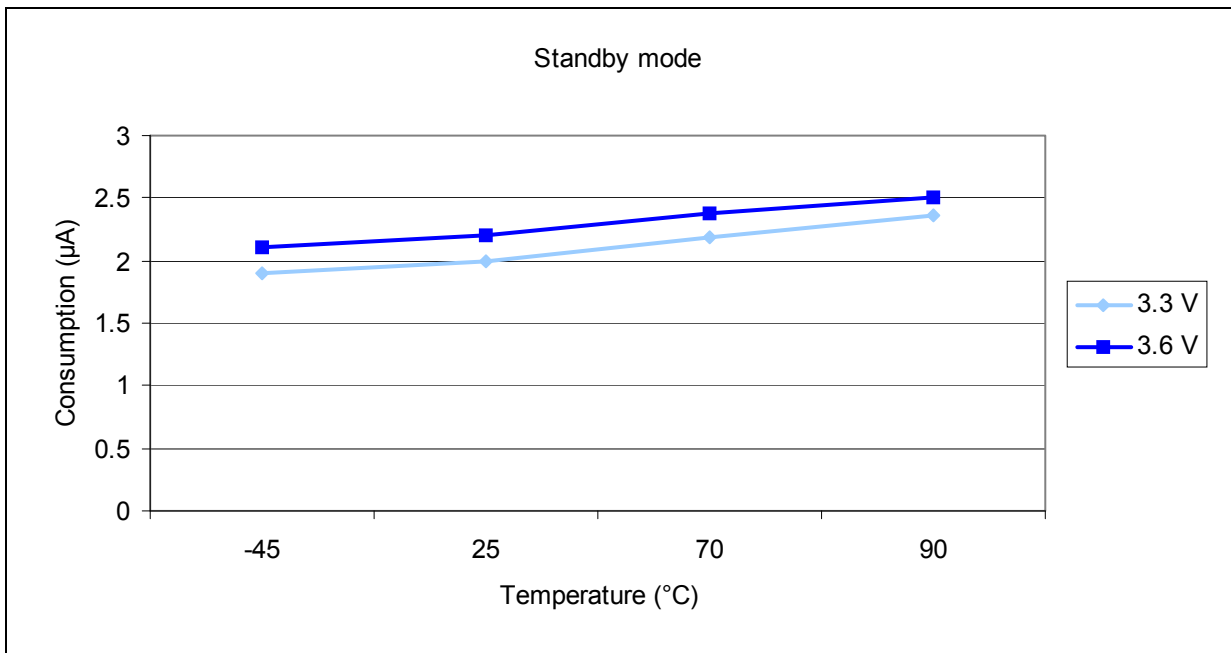


Figure 15. Typical current consumption in Standby mode versus temperature at  $V_{DD} = 3.3\text{ V}$  and  $3.6\text{ V}$



**Typical current consumption**

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f<sub>HCLK</sub> frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled f<sub>PCLK1</sub> = f<sub>HCLK</sub>/4, f<sub>PCLK2</sub> = f<sub>HCLK</sub>/2, f<sub>ADCCLK</sub> = f<sub>PCLK2</sub>/4

The parameters given in [Table 16](#) are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 8](#).

**Table 16. Typical current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typ <sup>(1)</sup>		Unit
				All peripherals enabled <sup>(2)</sup>	All peripherals disabled	
I <sub>DD</sub>	Supply current in Run mode	External clock <sup>(3)</sup>	48 MHz	24.2	18.6	mA
			36 MHz	19	14.8	
			24 MHz	12.9	10.1	
			16 MHz	9.3	7.4	
			8 MHz	5.5	4.6	
			4 MHz	3.3	2.8	
			2 MHz	2.2	1.9	
			1 MHz	1.6	1.45	
			500 kHz	1.3	1.25	
			125 kHz	1.08	1.06	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	23.5	17.9	
			36 MHz	18.3	14.1	
			24 MHz	12.2	9.5	
			16 MHz	8.5	6.8	
			8 MHz	4.9	4	
			4 MHz	2.7	2.2	
			2 MHz	1.6	1.4	
			1 MHz	1.02	0.9	
			500 kHz	0.73	0.67	
			125 kHz	0.5	0.48	

1. Typical values are measures at T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V.  
 2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC\_CR2 register).



3. External clock is 8 MHz and PLL is on when  $f_{HCLK} > 8$  MHz.

**Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM**

Symbol	Parameter	Conditions	$f_{HCLK}$	Typ <sup>(1)</sup>	Typ <sup>(1)</sup>	Unit
				All peripherals enabled <sup>(2)</sup>	All peripherals disabled	
$I_{DD}$	Supply current in Sleep mode	External clock <sup>(3)</sup>	48 MHz	9.9	3.9	mA
			36 MHz	7.6	3.1	
			24 MHz	5.3	2.3	
			16 MHz	3.8	1.8	
			8 MHz	2.1	1.2	
			4 MHz	1.6	1.1	
			2 MHz	1.3	1	
			1 MHz	1.11	0.98	
			500 kHz	1.04	0.96	
			125 kHz	0.98	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	9.3	3.3	
			36 MHz	7	2.5	
			24 MHz	4.8	1.8	
			16 MHz	3.2	1.2	
			8 MHz	1.6	0.6	
			4 MHz	1	0.5	
			2 MHz	0.72	0.47	
			1 MHz	0.56	0.44	
			500 kHz	0.49	0.42	
			125 kHz	0.43	0.41	

1. Typical values are measures at  $T_A = 25$  °C,  $V_{DD} = 3.3$  V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC\_CR2 register).
3. External clock is 8 MHz and PLL is on when  $f_{HCLK} > 8$  MHz.

**On-chip peripheral current consumption**

The current consumption of the on-chip peripherals is given in [Table 18](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V<sub>DD</sub> supply voltage conditions as summarized in [Table 5](#).

**Table 18. Peripheral current consumption<sup>(1)</sup>**

Peripheral		µA/MHz
AHB (up to 48 MHz)	DMA1	16.53
	BusMatrix <sup>(2)</sup>	8.33
APB1 (up to 24 MHz)	APB1-Bridge	10.28
	TIM2	32.50
	TIM3	31.39
	TIM4	31.94
	SPI2	4.17
	USART2	12.22
	USART3	12.22
	I2C1	10.00
	I2C2	10.00
	USB	17.78
	WWDG	2.50
	PWR	1.67
	BKP	2.50
IWDG	11.67	
APB2 (up to 48 MHz)	APB2-Bridge	3.75
	GPIOA	6.67
	GPIOB	6.53
	GPIOC	6.53
	GPIOD	6.53
	SPI1	4.72
	USART1	11.94
	ADC1 <sup>(3) (4)</sup>	17.50

1. f<sub>HCLK</sub> = 48 MHz, f<sub>APB1</sub> = f<sub>HCLK</sub>/2, f<sub>APB2</sub> = f<sub>HCLK</sub>, default prescaler value for each peripheral.

2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC:  $f_{HCLK} = 48 \text{ MHz}$ ,  $f_{APB1} = f_{HCLK}/2$ ,  $f_{APB2} = f_{HCLK}$ ,  $f_{ADCCLK} = f_{APB2}/4$ .
4. When ADON bit in the ADC\_CR2 register is set to 1, there is an additional current consumption equal to 0,65 mA. When we enable the ADC, there is an additional current consumption of 0,05 mA.

### 5.3.6 External clock source characteristics

#### High-speed external user clock generated from an external source

The characteristics given in [Table 19](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 8](#).

**Table 19. High-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	User external clock source frequency <sup>(1)</sup>	-	1	8	25	MHz
$V_{HSEH}$	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	$V_{DD}$	V
$V_{HSEL}$	OSC_IN input pin low level voltage		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time <sup>(1)</sup>		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time <sup>(1)</sup>		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance <sup>(1)</sup>		-	5	-	pF
DuCy <sub>(HSE)</sub>	Duty cycle		45	-	55	%
$I_L$	OSC_IN Input leakage current		$V_{SS} \leq V_{IN} \leq V_{DD}$		-	$\pm 1$

1. Guaranteed by design, not tested in production.

#### Low-speed external user clock generated from an external source

The characteristics given in [Table 20](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 8](#).

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User external clock source frequency <sup>(1)</sup>	-	-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	$V_{DD}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time <sup>(1)</sup>		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time <sup>(1)</sup>		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance <sup>(1)</sup>		-	5	-	pF
DuCy(LSE)	Duty cycle		30	-	70	%
$I_L$	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

1. Guaranteed by design, not tested in production.

Figure 16. High-speed external clock source AC timing diagram

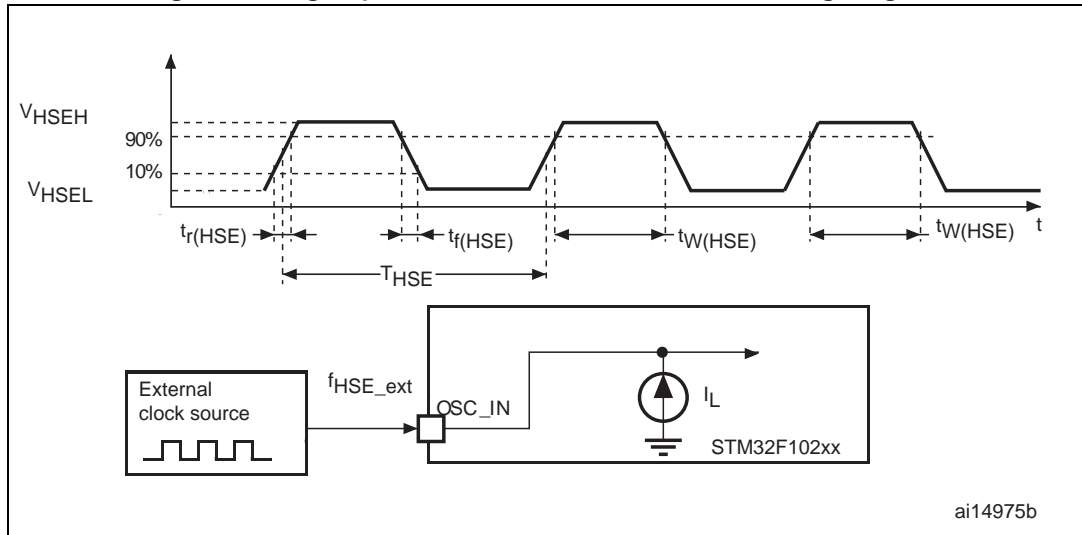
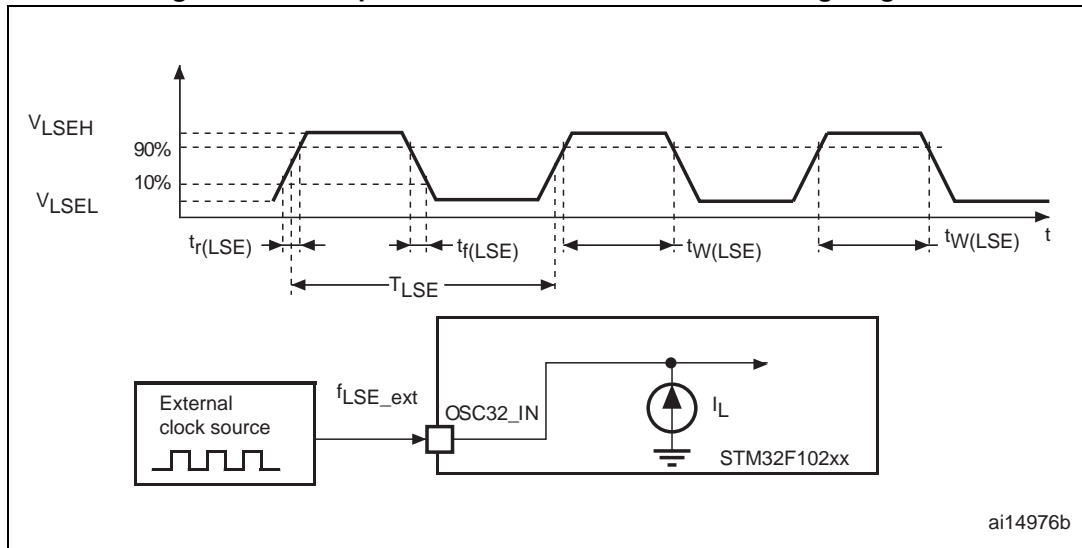




Figure 17. Low-speed external clock source AC timing diagram



### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 21](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

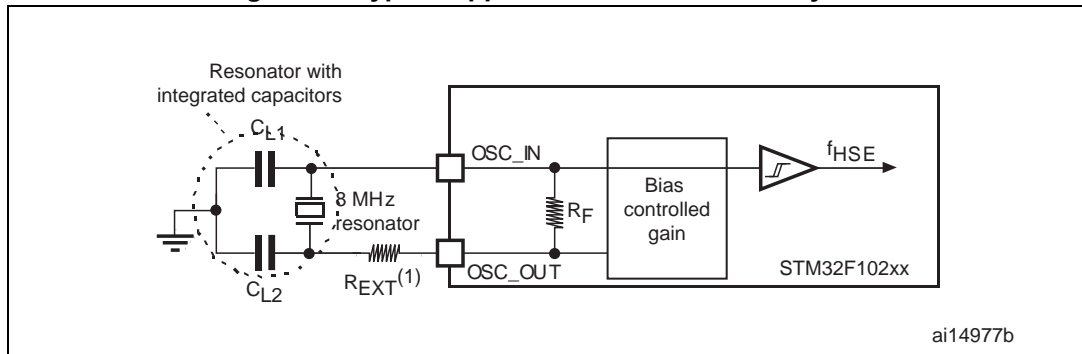
**Table 21. HSE 4-16 MHz oscillator characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency	-	4	8	16	MHz
$R_F$	Feedback resistor	-	-	200	-	k $\Omega$
C	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(3)</sup>	$R_S = 30 \Omega$	-	30	-	pF
$i_2$	HSE driving current	$V_{DD} = 3.3 V$ $V_{IN} = V_{SS}$ with 30 pF load	-	-	1	mA
$g_m$	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$ <sup>(4)</sup>	Startup time	$V_{DD}$ is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 18](#)).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

Figure 18. Typical application with an 8 MHz crystal



1.  $R_{EXT}$  value depends on the crystal characteristics.

**Low-speed external clock generated from a crystal/ceramic resonator**

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 22](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. LSE oscillator characteristics ( $f_{LSE} = 32.768 \text{ kHz}$ )

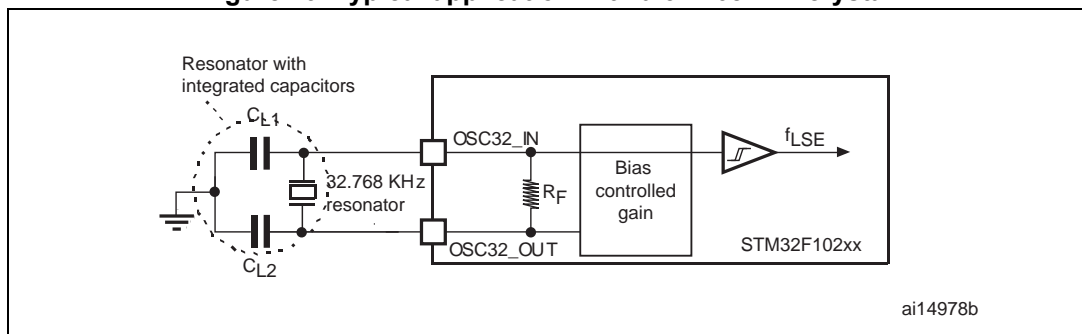
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_F$	Feedback resistor	-	-	5	-	$M\Omega$	
$C^{(1)}$	Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ )	$R_S = 30 \text{ k}\Omega$	-	-	15	pF	
$I_2$	LSE driving current	$V_{DD} = 3.3 \text{ V}$ $V_{IN} = V_{SS}$	-	-	1.4	$\mu\text{A}$	
$g_m$	Oscillator transconductance	-	5	-	-	$\mu\text{A/V}$	
$t_{SU(LSE)}^{(2)}$	Startup time	$V_{DD}$ is stabilized	$T_A = 50 \text{ }^\circ\text{C}$	-	1.5	-	s
			$T_A = 25 \text{ }^\circ\text{C}$	-	2.5	-	
			$T_A = 10 \text{ }^\circ\text{C}$	-	4.0	-	
			$T_A = 0 \text{ }^\circ\text{C}$	-	6.0	-	
			$T_A = -10 \text{ }^\circ\text{C}$	-	10.0	-	
			$T_A = -20 \text{ }^\circ\text{C}$	-	17.0	-	
			$T_A = -30 \text{ }^\circ\text{C}$	-	32.0	-	
$T_A = -40 \text{ }^\circ\text{C}$	-	60.0	-				

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled by software to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and can vary significantly with the crystal manufacturer, PCB layout and humidity.

**Note:** For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.  
 Load capacitance CL has the following formula:  $CL = CL1 \times CL2 / (CL1 + CL2) + C_{stray}$  where  $C_{stray}$  is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

**Caution:** To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance  $CL \leq 7$  pF. Never use a resonator with a load capacitance of 12.5 pF.  
 Example: if you choose a resonator with a load capacitance of  $CL = 6$  pF, and  $C_{stray} = 2$  pF, then  $CL1 = CL2 = 8$  pF.

**Figure 19. Typical application with a 32.768 kHz crystal**



### 5.3.7 Internal clock source characteristics

The parameters given in [Table 23](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

#### High-speed internal (HSI) RC oscillator

**Table 23. HSI oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$f_{HSI}$	Frequency	-	-	8	-	MHz	
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%	
$ACC_{HSI}$	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register <sup>(2)</sup>	-	-	1 <sup>(3)</sup>	%	
		Factory-calibrated <sup>(4)(5)</sup>	$T_A = -40$ to $105$ °C	-2.0	-	2.5	%
			$T_A = -10$ to $85$ °C	-1.5	-	2.2	%
			$T_A = 0$ to $70$ °C	-1.3	-	2	%
$T_A = 25$ °C	-1.1	-	1.8	%			
$t_{su(HSI)}^{(4)}$	HSI oscillator startup time	-	1	-	2	$\mu$ s	
$I_{DD(HSI)}^{(4)}$	HSI oscillator power consumption	-	-	80	100	$\mu$ A	

1.  $V_{DD} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.

2. Refer to application note AN2868 "STM32F10xxx internal RC oscillator (HSI) calibration" available from the ST website [www.st.com](http://www.st.com).
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

**Low-speed internal (LSI) RC oscillator**

**Table 24. LSI oscillator characteristics <sup>(1)</sup>**

Symbol	Parameter	Min <sup>(2)</sup>	Typ	Max	Unit
f <sub>LSI</sub>	Frequency	30	40	60	kHz
t <sub>su(LSI)</sub> <sup>(3)</sup>	LSI oscillator startup time	-	-	85	μs
I <sub>DD(LSI)</sub> <sup>(3)</sup>	LSI oscillator power consumption	-	0.65	1.2	μA

1. V<sub>DD</sub> = 3 V, T<sub>A</sub> = -40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

**Wakeup time from low-power mode**

The wakeup times given in [Table 25](#) is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 8](#).

**Table 25. Low-power mode wakeup timings**

Symbol	Parameter	Typ	Unit
t <sub>WUSLEEP</sub> <sup>(1)</sup>	Wakeup from Sleep mode	1.8	μs
t <sub>WUSTOP</sub> <sup>(1)</sup>	Wakeup from Stop mode (regulator in run mode)	3.6	μs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
t <sub>WUSTDBY</sub> <sup>(1)</sup>	Wakeup from Standby mode	50	μs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

**5.3.8 PLL characteristics**

The parameters given in [Table 26](#) are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 8](#).

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	
f <sub>PLL_IN</sub>	PLL input clock <sup>(2)</sup>	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f <sub>PLL_OUT</sub>	PLL multiplier output clock	16	-	48	MHz
t <sub>LOCK</sub>	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f<sub>PLL\_OUT</sub>.

### 5.3.9 Memory characteristics

#### Flash memory

The characteristics are given at T<sub>A</sub> = -40 to 85 °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
t <sub>prog</sub>	16-bit programming time	T <sub>A</sub> = -40 to +85 °C	40	52.5	70	µs
t <sub>ERASE</sub>	Page (1 KB) erase time	T <sub>A</sub> = -40 to +85 °C	20	-	40	ms
t <sub>ME</sub>	Mass erase time	T <sub>A</sub> = -40 to +85 °C	20	-	40	ms
I <sub>DD</sub>	Supply current	Read mode f <sub>HCLK</sub> = 48 MHz with 2 wait states, V <sub>DD</sub> = 3.3 V	-	-	20	mA
		Write / Erase modes f <sub>HCLK</sub> = 48 MHz, V <sub>DD</sub> = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V <sub>DD</sub> = 3.0 to 3.6 V	-	-	50	µA
V <sub>prog</sub>	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 28. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min <sup>(1)</sup>	Typ	Max	
N <sub>END</sub>	Endurance		10	-	-	kcycles
t <sub>RET</sub>	Data retention	T <sub>A</sub> = 85 °C, 1000 cycles	30	-	-	Years

1. Based on characterization not tested in production.

### 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 29](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 29. EMS characteristics**

Symbol	Parameter	Conditions	Level/Class
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 61000-4-2	2B
$V_{EFTB}$	Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , $T_A = +25\text{ °C}$ , $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 61000-4-4	4A

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

**Software recommendations:** the software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers, etc.)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports), This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 30. EMI characteristics**

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ]	Unit
				8/48 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C.	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

**5.3.11 Absolute maximum ratings (electrical sensitivity)**

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 31. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (human body model)	T <sub>A</sub> = +25 °C, conforming to JESD22-A114	2	2000	V
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (charge device model)	T <sub>A</sub> = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

**Static latch-up**

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

**Table 32. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +105 °C conforming to JESD78A	II level A





### 5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DD}$  (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in [Table 33](#).

**Table 33. I/O current injection susceptibility**

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
$I_{INJ}$	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

### 5.3.13 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under the conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Low level input voltage	Standard IO input low level voltage	-	-	0.28*(V <sub>DD</sub> -2 V)+0.8 V <sup>(1)</sup>	V
		IO FT <sup>(3)</sup> input low level voltage	-	-	0.32*(V <sub>DD</sub> -2V)+0.75 V <sup>(1)</sup>	
		All I/Os except BOOT0	-	-	0.35V <sub>DD</sub> <sup>(2)</sup>	
V <sub>IH</sub>	High level input voltage	Standard IO input high level voltage	0.41*(V <sub>DD</sub> -2 V)+1.3 V <sup>(1)</sup>	-	-	V
		IO FT <sup>(3)</sup> input high level voltage	0.42*(V <sub>DD</sub> -2 V)+1 V <sup>(1)</sup>	-	-	
		All I/Os except BOOT0	0.65V <sub>DD</sub> <sup>(2)</sup>	-	-	
V <sub>hys</sub>	Standard IO Schmitt trigger voltage hysteresis <sup>(4)</sup>	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis <sup>(4)</sup>	-	5% V <sub>DD</sub> <sup>(5)</sup>	-	-	
I <sub>lkg</sub>	Input leakage current <sup>(6)</sup>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> Standard I/Os	-	-	±1	µA
		V <sub>IN</sub> = 5 V I/O FT	-	-	3	
R <sub>PU</sub>	Weak pull-up equivalent resistor <sup>(7)</sup>	V <sub>IN</sub> = V <sub>SS</sub>	30	40	50	kΩ
R <sub>PD</sub>	Weak pull-down equivalent resistor <sup>(7)</sup>	V <sub>IN</sub> = V <sub>DD</sub>	30	40	50	
C <sub>IO</sub>	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant, In order to sustain a voltage higher than V<sub>DD</sub>+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max, if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 20](#) and [Figure 21](#) for standard I/Os, and in [Figure 22](#) and [Figure 23](#) for 5 V tolerant I/Os.

Figure 20. Standard I/O input characteristics - CMOS port

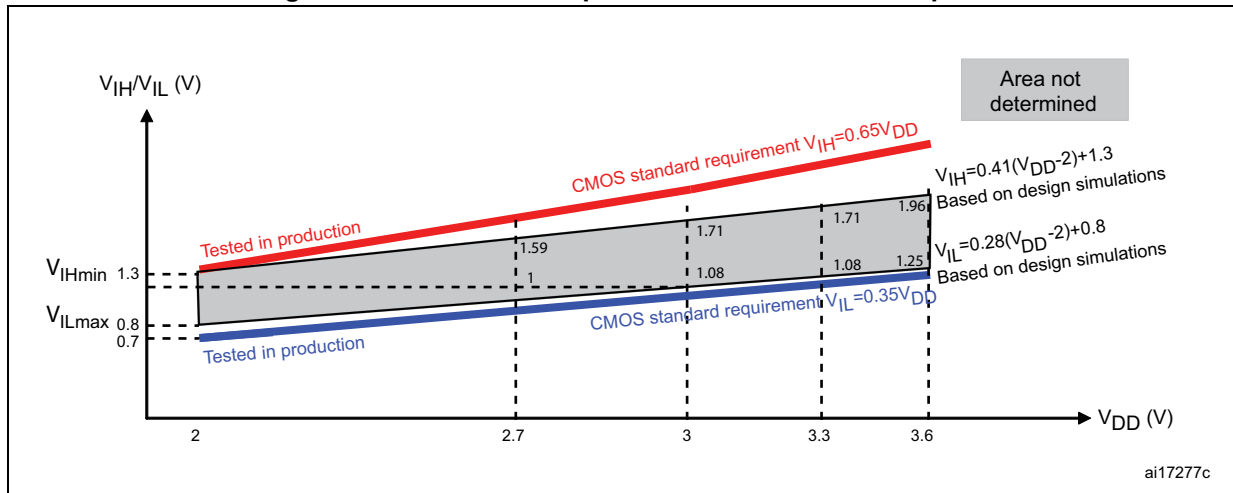


Figure 21. Standard I/O input characteristics - TTL port

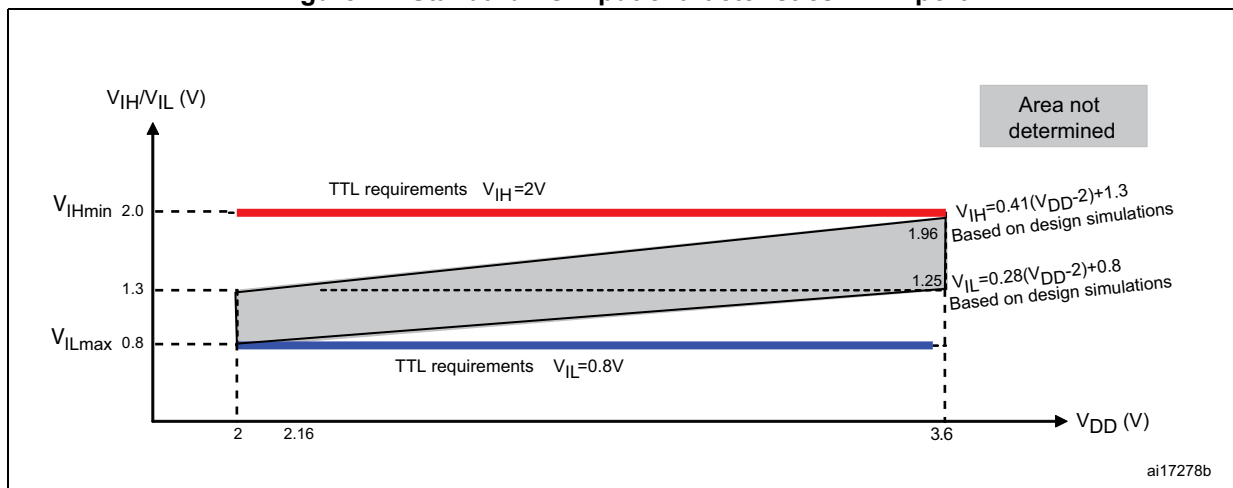


Figure 22. 5 V tolerant I/O input characteristics - CMOS port

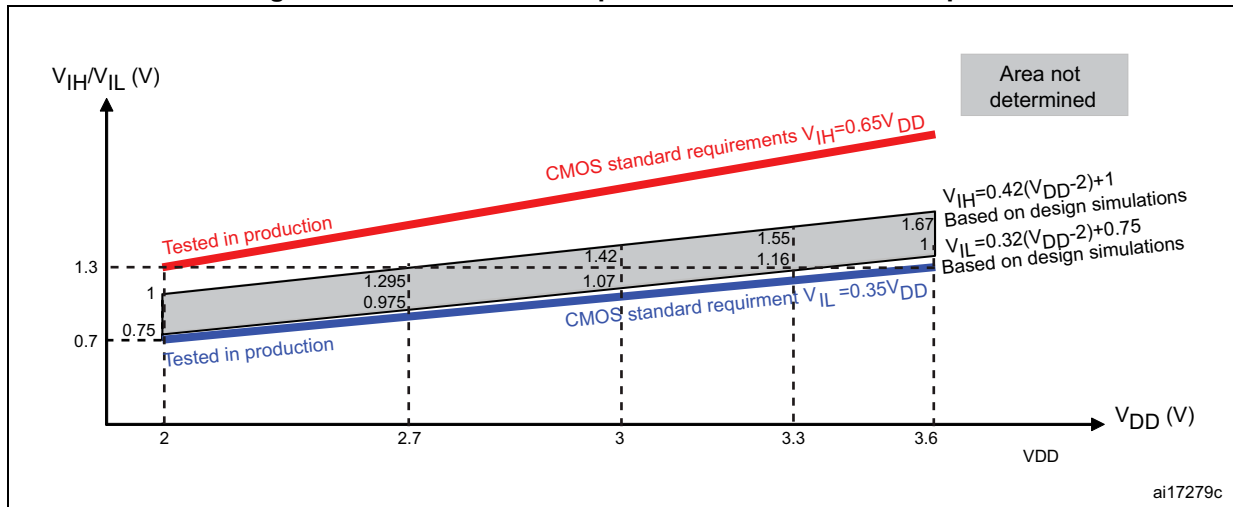
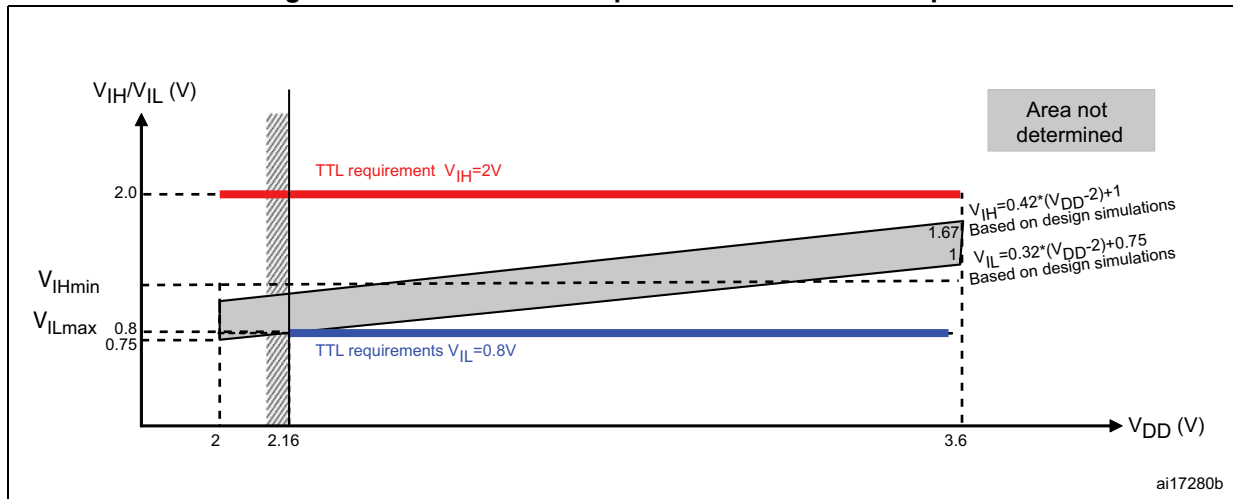


Figure 23. 5 V tolerant I/O input characteristics - TTL port



**Output driving current**

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ) except PC13, PC14 and PC15 which can sink or source up to  $\pm 3$  mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum ratings specified in [Section 5.2](#).

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $I_{VDD}$  (see [Table 6](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $I_{VSS}$  (see [Table 6](#)).

### Output voltage levels

Unless otherwise specified, the parameters given in [Table 35](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

**Table 35. Output voltage characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port <sup>(2)</sup> . $I_{IO} = +8 \text{ mA}$ . $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port <sup>(2)</sup> . $I_{IO} = +8 \text{ mA}$ . $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +20 \text{ mA}^{(4)}$ . $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-1.3$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +6 \text{ mA}^{(4)}$ . $2.0 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$	-	

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ .
4. Based on characterization data, not tested in production.

**Input/output AC characteristics**

The definition and values of input/output AC characteristics are given in [Figure 24](#) and [Table 36](#), respectively.

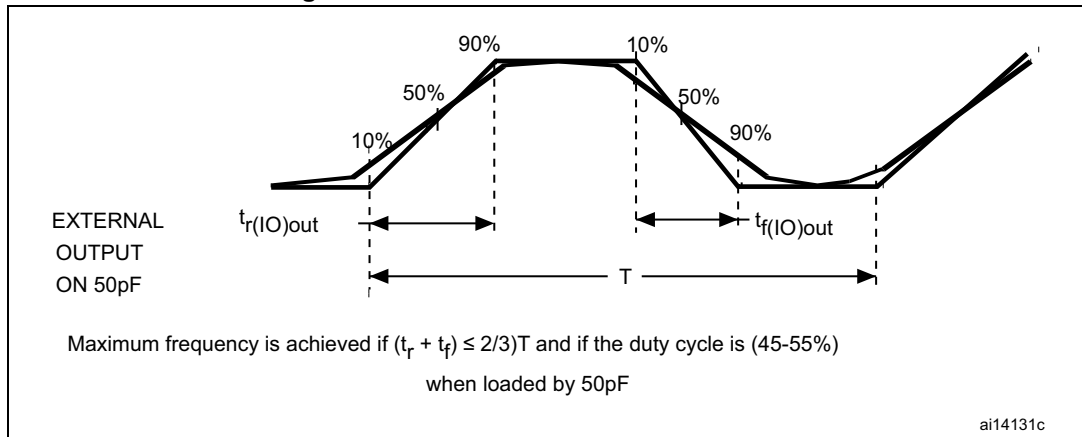
Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

**Table 36. I/O AC characteristics<sup>(1)</sup>**

MODEx [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(I/O)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	2	MHz
	$t_{f(I/O)out}$	Output high to low level fall time	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	125 <sup>(3)</sup>	ns
	$t_{r(I/O)out}$	Output low to high level rise time		125 <sup>(3)</sup>	
01	$f_{max(I/O)out}$	Maximum frequency <sup>(2)</sup>	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	10	MHz
	$t_{f(I/O)out}$	Output high to low level fall time	$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	25 <sup>(3)</sup>	ns
	$t_{r(I/O)out}$	Output low to high level rise time		25 <sup>(3)</sup>	
11	$F_{max(I/O)out}$	Maximum Frequency <sup>(2)</sup>	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	50	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	30	MHz
			$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	20	MHz
	$t_{f(I/O)out}$	Output high to low level fall time	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 <sup>(3)</sup>	ns
			$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 <sup>(3)</sup>	
			$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 <sup>(3)</sup>	
	$t_{r(I/O)out}$	Output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 <sup>(3)</sup>	
			$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 <sup>(3)</sup>	
			$C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 <sup>(3)</sup>	
-	$t_{EXTIpw}$	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 24](#).
3. Guaranteed by design, not tested in production.

Figure 24. I/O AC characteristics definition



### 5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 34](#)).

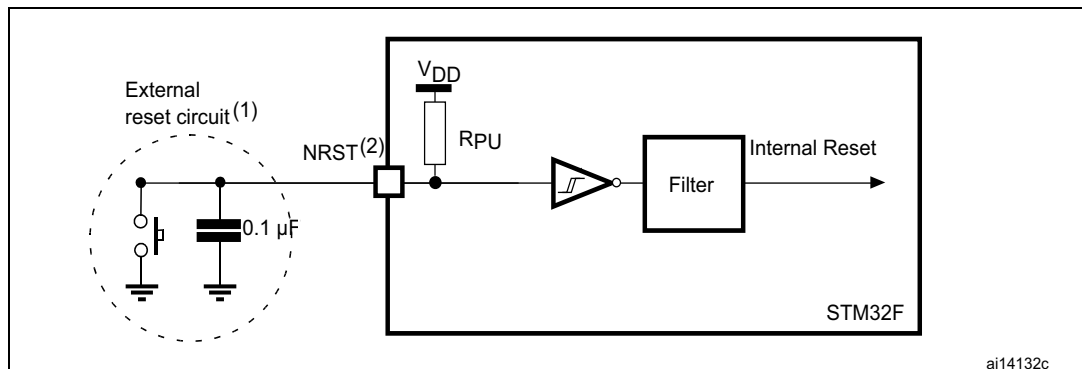
Unless otherwise specified, the parameters given in [Table 37](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	-	2	-	$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
$R_{PU}$	Weak pull-up equivalent resistor <sup>(2)</sup>	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 25. Recommended NRST pin protection



ai14132c

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 39](#). Otherwise the reset will not be taken into account by the device.



### 5.3.15 TIM timer characteristics

The parameters given in [Table 38](#) are guaranteed by design.

Refer to [Section 5.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 38. TIMx<sup>(1)</sup> characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	20.84	-	ns
$f_{EXT}$	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 48 \text{ MHz}$	0	24	MHz
$Res_{TIM}$	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	0.0208	1365	$\mu\text{s}$
$t_{MAX\_COUNT}$	Maximum possible count	-	-	$65536 \times 65536$	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	-	89.48	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

### 5.3.16 Communications interfaces

#### I<sup>2</sup>C interface characteristics

The STM32F102xx medium-density USB access line I<sup>2</sup>C interface meets the requirements of the standard I<sup>2</sup>C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and  $V_{DD}$  is disabled, but is still present.

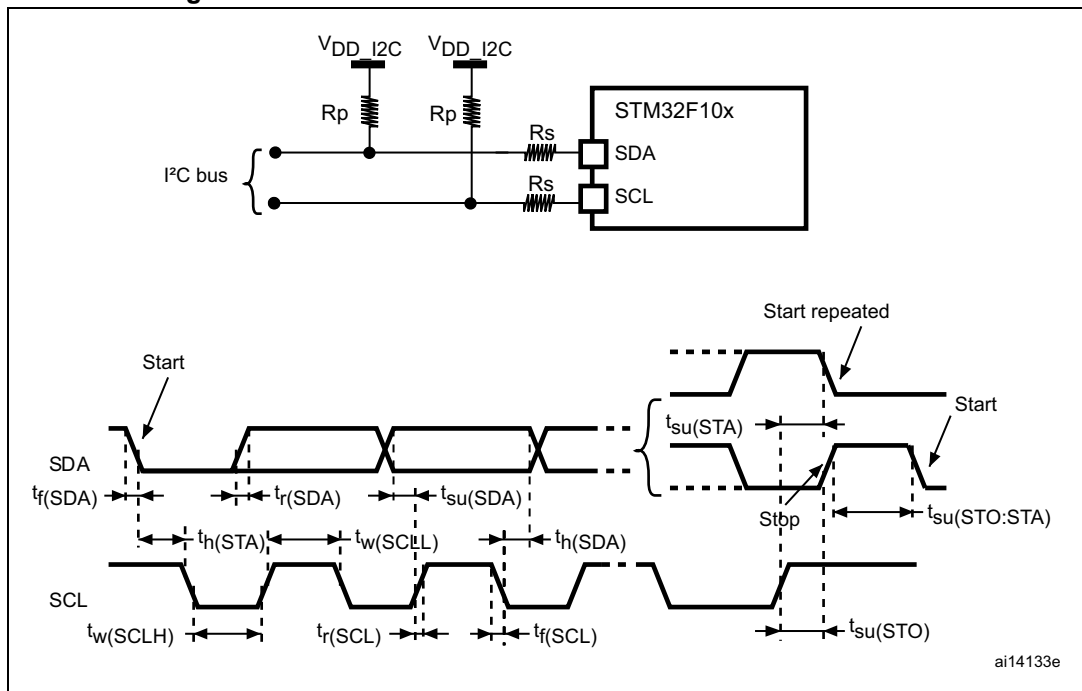
The I<sup>2</sup>C characteristics are described in [Table 39](#). Refer also to [Section 5.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I<sup>2</sup>C characteristics

Symbol	Parameter	Standard mode I <sup>2</sup> C <sup>(1)(2)</sup>		Fast mode I <sup>2</sup> C <sup>(1)(2)</sup>		Unit
		Min	Max	Min	Max	
t <sub>w(SCLL)</sub>	SCL clock low time	4.7	-	1.3	-	μs
t <sub>w(SCLH)</sub>	SCL clock high time	4.0	-	0.6	-	
t <sub>su(SDA)</sub>	SDA setup time	250	-	100	-	ns
t <sub>h(SDA)</sub>	SDA data hold time	-	3450 <sup>(3)</sup>	-	900 <sup>(3)</sup>	
t <sub>r(SDA)</sub> t <sub>r(SCL)</sub>	SDA and SCL rise time	-	1000	-	300	
t <sub>f(SDA)</sub> t <sub>f(SCL)</sub>	SDA and SCL fall time	-	300	-	300	μs
t <sub>h(STA)</sub>	Start condition hold time	4.0	-	0.6	-	
t <sub>su(STA)</sub>	Repeated Start condition setup time	4.7	-	0.6	-	μs
t <sub>su(STO)</sub>	Stop condition setup time	4.0	-	0.6	-	μs
t <sub>w(STO:STA)</sub>	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
t <sub>SP</sub>	Pulse width of spikes that are suppressed by the analog filter	0	50 <sup>(4)</sup>	0	50 <sup>(4)</sup>	ns
C <sub>b</sub>	Capacitive load for each bus line	-	400	-	400	pF

1. Values guaranteed by design, not tested in production.
2. f<sub>PCLK1</sub> must be at least 2 MHz to achieve standard mode I<sup>2</sup>C frequencies. It must be at least 4 MHz to achieve fast mode I<sup>2</sup>C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I<sup>2</sup>C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.
4. The analog filter minimum filtered spikes is above t<sub>SP(max)</sub> to ensure that spikes width up to t<sub>SP(max)</sub> are filtered.

Figure 26. I<sup>2</sup>C bus AC waveforms and measurement circuit<sup>(1)</sup>



1. Measurement points are done at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Table 40. SCL frequency (f<sub>PCLK1</sub> = 36 MHz, V<sub>DD\_I2C</sub> = 3.3 V)<sup>(1)(2)</sup>

f <sub>SCL</sub> (kHz)	I2C_CCR value
	R <sub>p</sub> = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R<sub>p</sub> = External pull-up resistance, f<sub>SCL</sub> = I<sup>2</sup>C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

**SPI interface characteristics**

Unless otherwise specified, the parameters given in [Table 41](#) are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 8](#).

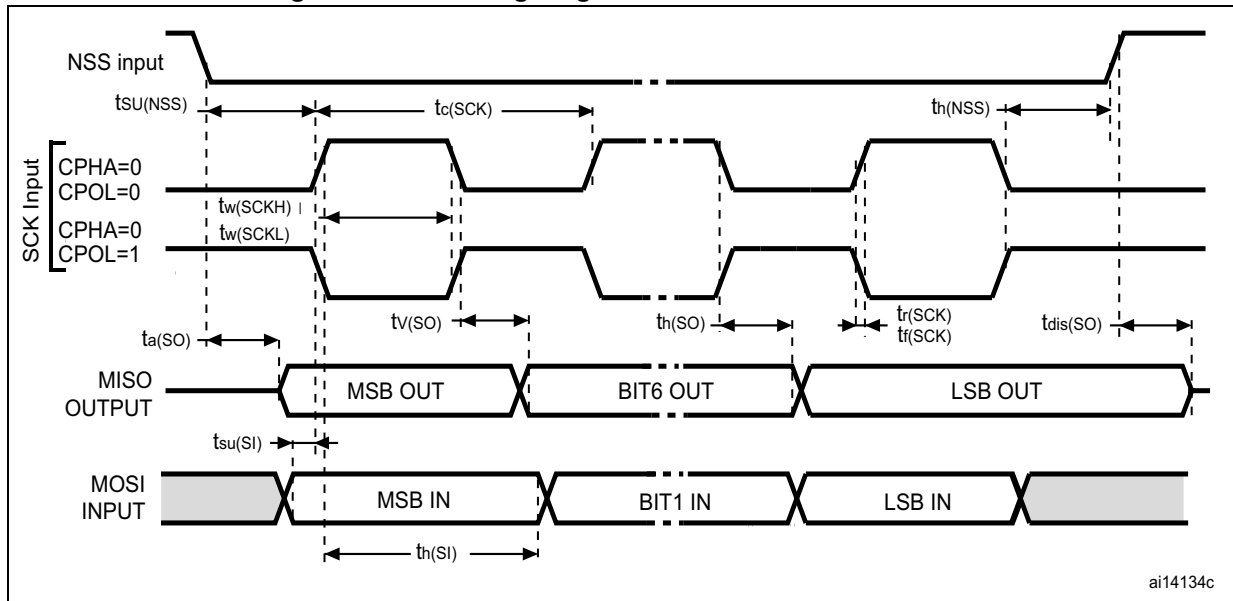
Refer to [Section 5.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 41. SPI characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}$ $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, $f_{PCLK} = 36$ MHz, presc = 4	50	60	
$t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}^{(1)}$ $t_{h(SI)}^{(1)}$	Data input hold time	Master mode	5	-	
		Slave mode	4	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, $f_{PCLK} = 20$ MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}^{(1)(3)}$	Data output disable time	Slave mode	2	10	
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}^{(1)}$ $t_{h(MO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	15	-	
		Master mode (after enable edge)	2	-	

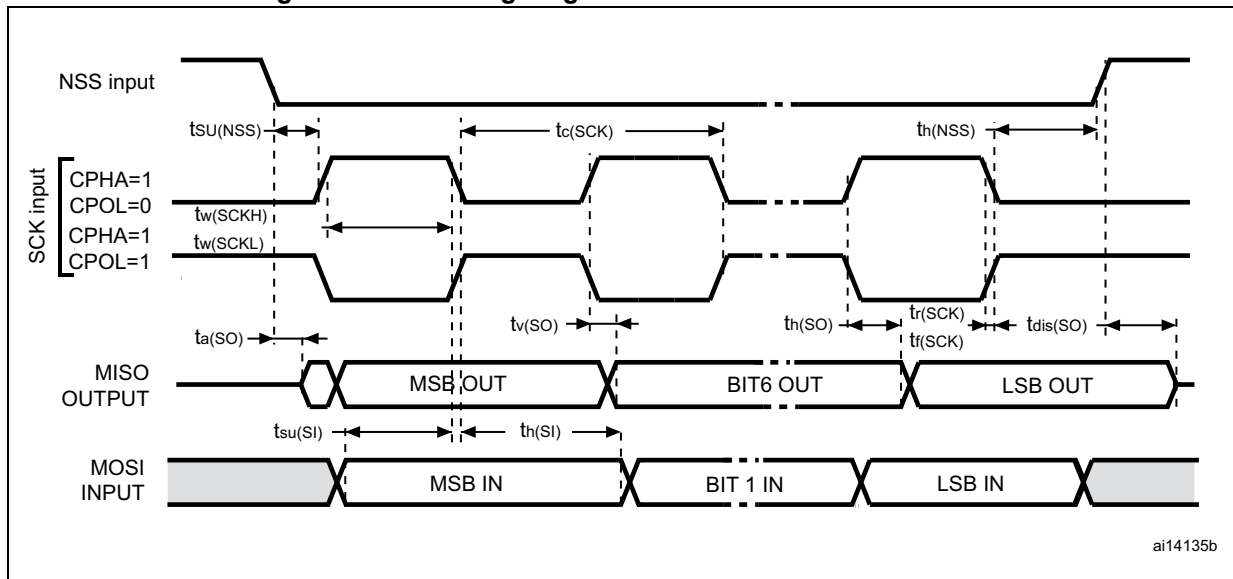
1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 27. SPI timing diagram - slave mode and CPHA=0



ai14134c

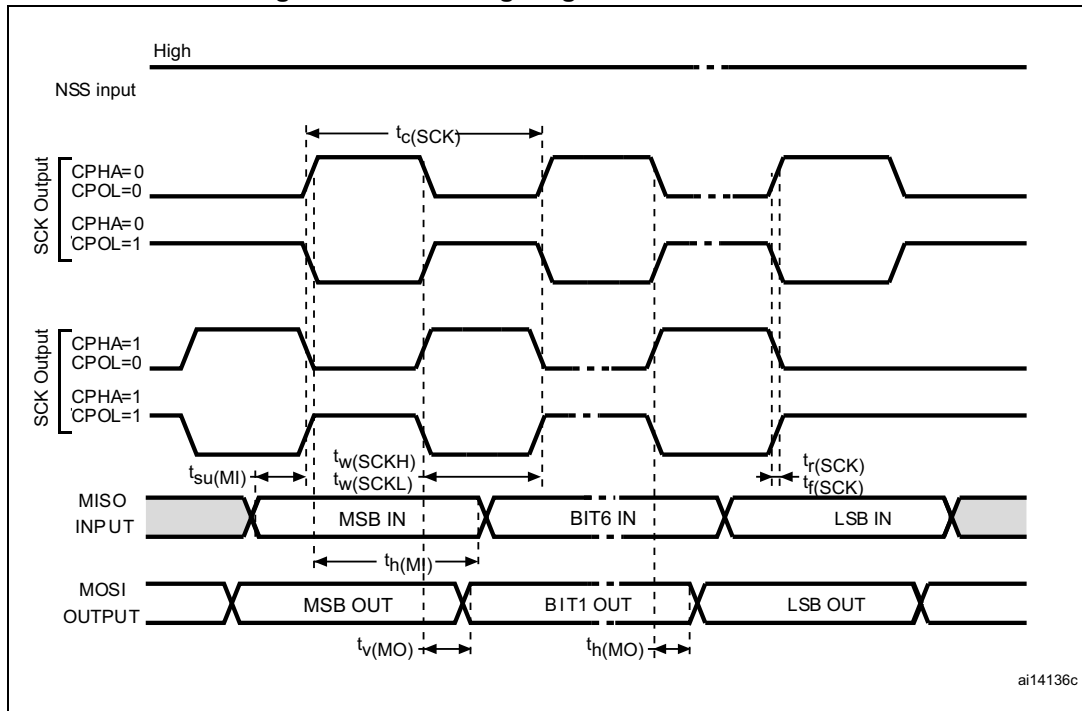
Figure 28. SPI timing diagram - slave mode and CPHA=1<sup>(1)</sup>



ai14135b

1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

Figure 29. SPI timing diagram - master mode<sup>(1)</sup>



1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

**USB characteristics**

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$	USB transceiver startup time	1	$\mu s$

Table 43. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. <sup>(1)</sup>	Max. <sup>(1)</sup>	Unit	
Input levels	V <sub>DD</sub>	USB operating voltage <sup>(2)</sup>	-	3.0 <sup>(3)</sup>	3.6	V
	V <sub>DI</sub> <sup>(4)</sup>	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
	V <sub>CM</sub> <sup>(4)</sup>	Differential common mode range	Includes V <sub>DI</sub> range	0.8	2.5	
	V <sub>SE</sub> <sup>(4)</sup>	Single ended receiver threshold	-	1.3	2.0	
Output levels	V <sub>OL</sub>	Static output level low	R <sub>L</sub> of 1.5 kΩ to 3.6 V <sup>(5)</sup>	-	0.3	V
	V <sub>OH</sub>	Static output level high	R <sub>L</sub> of 15 kΩ to V <sub>SS</sub> <sup>(5)</sup>	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB\_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F102xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V<sub>DD</sub> voltage range.
4. Guaranteed by design, not tested in production.
5. R<sub>L</sub> is the load connected on the USB drivers

Figure 30. USB timings: definition of data signal rise and fall time

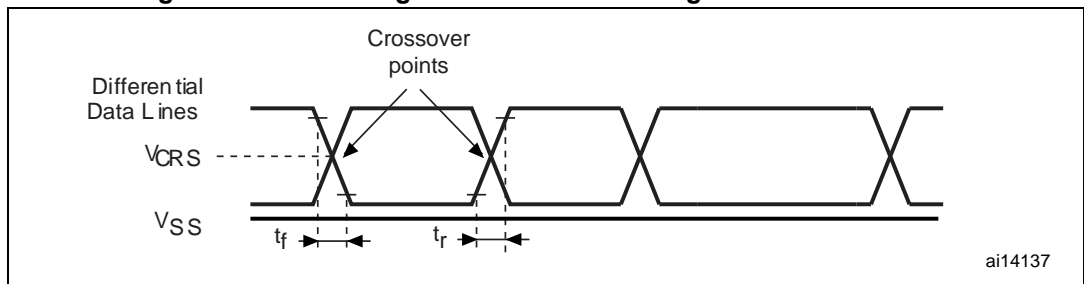


Table 44. USB: Full speed electrical characteristics of the driver<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
t <sub>r</sub>	Rise time <sup>(2)</sup>	C <sub>L</sub> = 50 pF	4	20	ns
t <sub>f</sub>	Fall time <sup>(2)</sup>	C <sub>L</sub> = 50 pF	4	20	ns
t <sub>rfm</sub>	Rise/ fall time matching	t <sub>r</sub> / t <sub>f</sub>	90	110	%
V <sub>CRS</sub>	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

### 5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature, f<sub>PCLK2</sub> frequency and V<sub>DDA</sub> supply voltage conditions summarized in [Table 8](#).

*Note:* It is recommended to perform a calibration after each power-up.

Table 45. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	Power supply	-	2.4	-	3.6	V
f <sub>ADC</sub>	ADC clock frequency	-	0.6	-	12	MHz
f <sub>S</sub> <sup>(1)</sup>	Sampling rate	-	0.05	-	0.85	Msp/s
f <sub>TRIG</sub> <sup>(1)</sup>	External trigger frequency	f <sub>ADC</sub> = 12 MHz	-	-	823	kHz
		-	-	-	17	1/f <sub>ADC</sub>
V <sub>AIN</sub>	Conversion voltage range <sup>(2)</sup>	-	0 (V <sub>SSA</sub> or V <sub>REF-</sub> tied to ground)	-	V <sub>REF+</sub>	V
R <sub>AIN</sub> <sup>(1)</sup>	External input impedance	See <a href="#">Equation 1</a> and <a href="#">Table 46</a> for details	-	-	50	κΩ
R <sub>ADC</sub> <sup>(1)</sup>	Sampling switch resistance	-	-	-	1	κΩ
C <sub>ADC</sub> <sup>(1)</sup>	Internal sample and hold capacitor	-	-	-	8	pF
t <sub>CAL</sub> <sup>(1)</sup>	Calibration time	f <sub>ADC</sub> = 12 MHz	5.9			μs
		-	83			1/f <sub>ADC</sub>
t <sub>lat</sub> <sup>(1)</sup>	Injection trigger conversion latency	f <sub>ADC</sub> = 12 MHz	-	-	0.214	μs
		-	-	-	3 <sup>(3)</sup>	1/f <sub>ADC</sub>
t <sub>latr</sub> <sup>(1)</sup>	Regular trigger conversion latency	f <sub>ADC</sub> = 12 MHz	-	-	0.143	μs
		-	-	-	2 <sup>(3)</sup>	1/f <sub>ADC</sub>
t <sub>S</sub> <sup>(1)</sup>	Sampling time	f <sub>ADC</sub> = 12 MHz	0.125	-	19.95	μs
		-	1.5	-	239.5	1/f <sub>ADC</sub>
t <sub>STAB</sub> <sup>(1)</sup>	Power-up time	-	0	0	1	μs
t <sub>CONV</sub> <sup>(1)</sup>	Total conversion time (including sampling time)	f <sub>ADC</sub> = 12 MHz	1.2	-	21	μs
		-	14 to 252 (t <sub>S</sub> for sampling + 12.5 for successive approximation)			1/f <sub>ADC</sub>

1. Guaranteed by design, not tested in production.
2. V<sub>REF+</sub> is internally connected to V<sub>DDA</sub> and V<sub>REF-</sub> is internally connected to V<sub>SSA</sub>.
3. For external triggers, a delay of 1/f<sub>PCLK2</sub> must be added to the latency specified in [Table 46](#).

**Equation 1: R<sub>AIN</sub> max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).



**Table 46.  $R_{AIN}$  max for  $f_{ADC} = 12\text{ MHz}^{(1)}$**

$T_s$ (cycles)	$t_s$ ( $\mu\text{s}$ )	$R_{AIN}$ max ( $\text{k}\Omega$ )
1.5	0.13	0.4
7.5	0.63	5.9
13.5	1.13	11.4
28.5	2.38	25.2
41.5	3.46	37.2
55.5	4.63	50
71.5	5.96	NA
239.5	19.96	NA

1. Data guaranteed by design, not tested in production.

**Table 47. ADC accuracy - limited test conditions<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Typ	Max <sup>(2)</sup>	Unit
ET	Total unadjusted error	$f_{PCLK2} = 48\text{ MHz}$ . $f_{ADC} = 12\text{ MHz}$ , $R_{AIN} < 10\text{ k}\Omega$ . $V_{DDA} = 3\text{ V to } 3.6\text{ V}$ $T_A = 25\text{ }^\circ\text{C}$ Measurements made after ADC calibration	$\pm 1.3$	$\pm 2$	LSB
EO	Offset error		$\pm 1$	$\pm 1.5$	
EG	Gain error		$\pm 0.5$	$\pm 1.5$	
ED	Differential linearity error		$\pm 0.7$	$\pm 1$	
EL	Integral linearity error		$\pm 0.8$	$\pm 1.5$	

1. ADC DC accuracy values are measured after internal calibration.

2. Based on characterization, not tested in production.

**Table 48. ADC accuracy<sup>(1) (2) (3)</sup>**

Symbol	Parameter	Test conditions	Typ	Max <sup>(4)</sup>	Unit
ET	Total unadjusted error	$f_{PCLK2} = 48\text{ MHz}$ . $f_{ADC} = 12\text{ MHz}$ , $R_{AIN} < 10\text{ k}\Omega$ . $V_{DDA} = 2.4\text{ V to } 3.6\text{ V}$ Measurements made after ADC calibration	$\pm 2$	$\pm 5$	LSB
EO	Offset error		$\pm 1.5$	$\pm 2.5$	
EG	Gain error		$\pm 1.5$	$\pm 3$	
ED	Differential linearity error		$\pm 1$	$\pm 2$	
EL	Integral linearity error		$\pm 1.5$	$\pm 3$	

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted  $V_{DD}$ , frequency and temperature ranges.

3. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.  
 Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 5.3.13](#) does not affect the ADC accuracy.

4. Based on characterization, not tested in production.

Figure 31. ADC accuracy characteristics

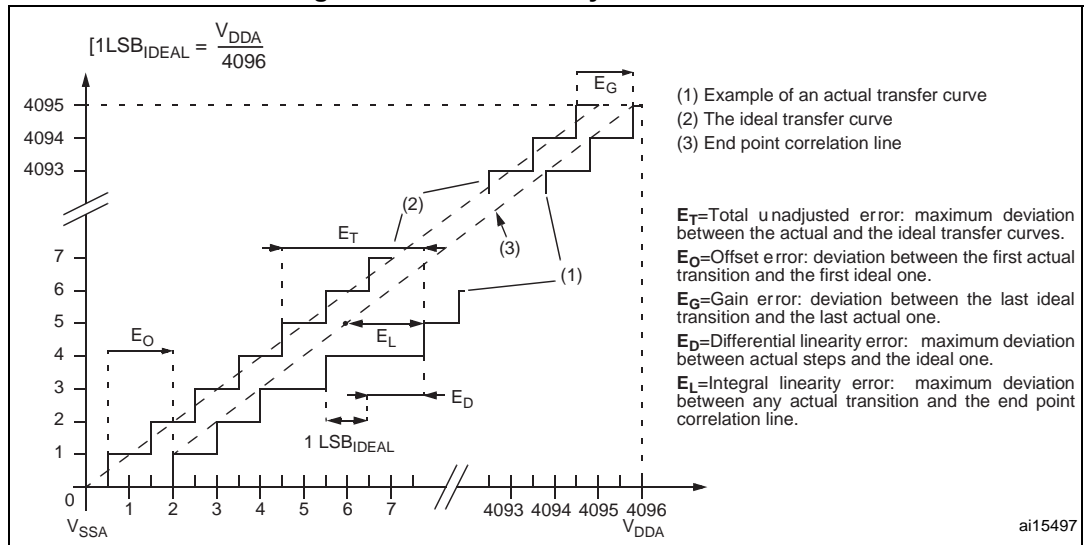
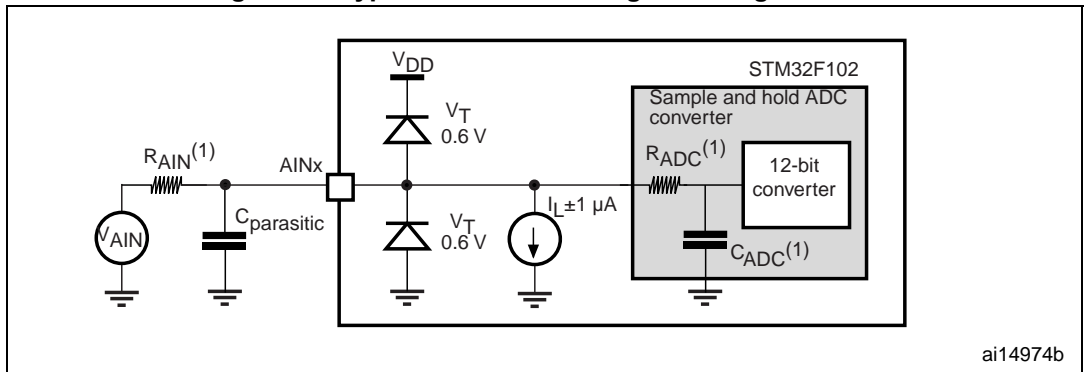


Figure 32. Typical connection diagram using the ADC

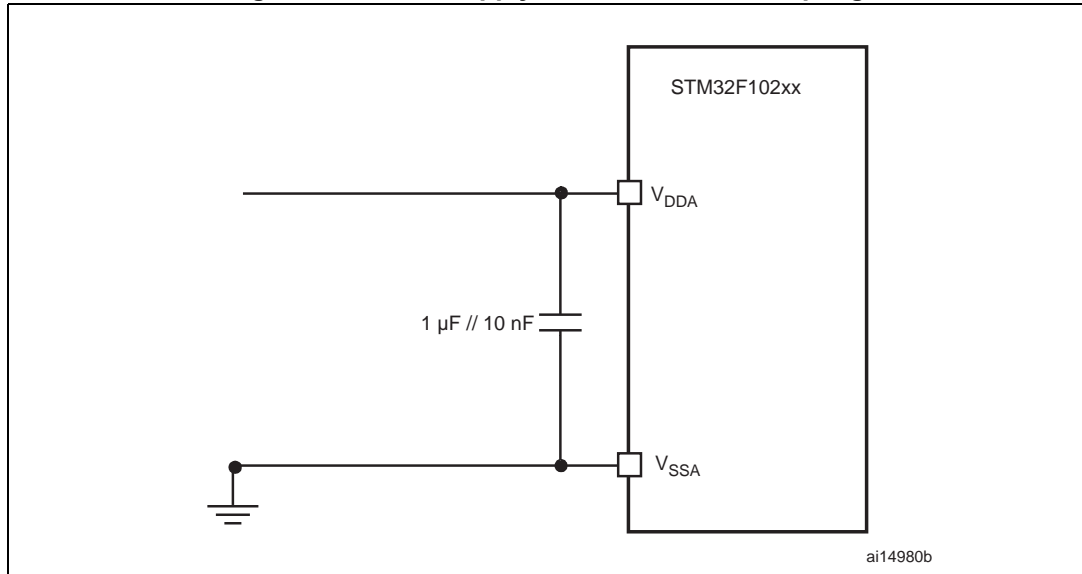


1. Refer to [Table 46](#) for the values of  $R_{\text{AIN}}$ ,  $R_{\text{ADC}}$  and  $C_{\text{ADC}}$ .
2.  $C_{\text{parasitic}}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{\text{parasitic}}$  value will downgrade conversion accuracy. To remedy this,  $f_{\text{ADC}}$  should be reduced.

**General PCB design guidelines**

Power supply decoupling should be performed as shown in [Figure 33](#). The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Figure 33. Power supply and reference decoupling**



**5.3.18 Temperature sensor characteristics**

**Table 49. TS characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature	-	±1.5	-	°C
Avg_Slope <sup>(1)</sup>	Average slope	-	4.35	-	mV/°C
$V_{25}^{(1)}$	Voltage at 25°C	-	1.42	-	V
$t_{START}^{(2)}$	Startup time	4	-	10	µs
$T_{S\_temp}^{(3)(2)}$	ADC sampling time when reading the temperature	-	-	17.1	µs

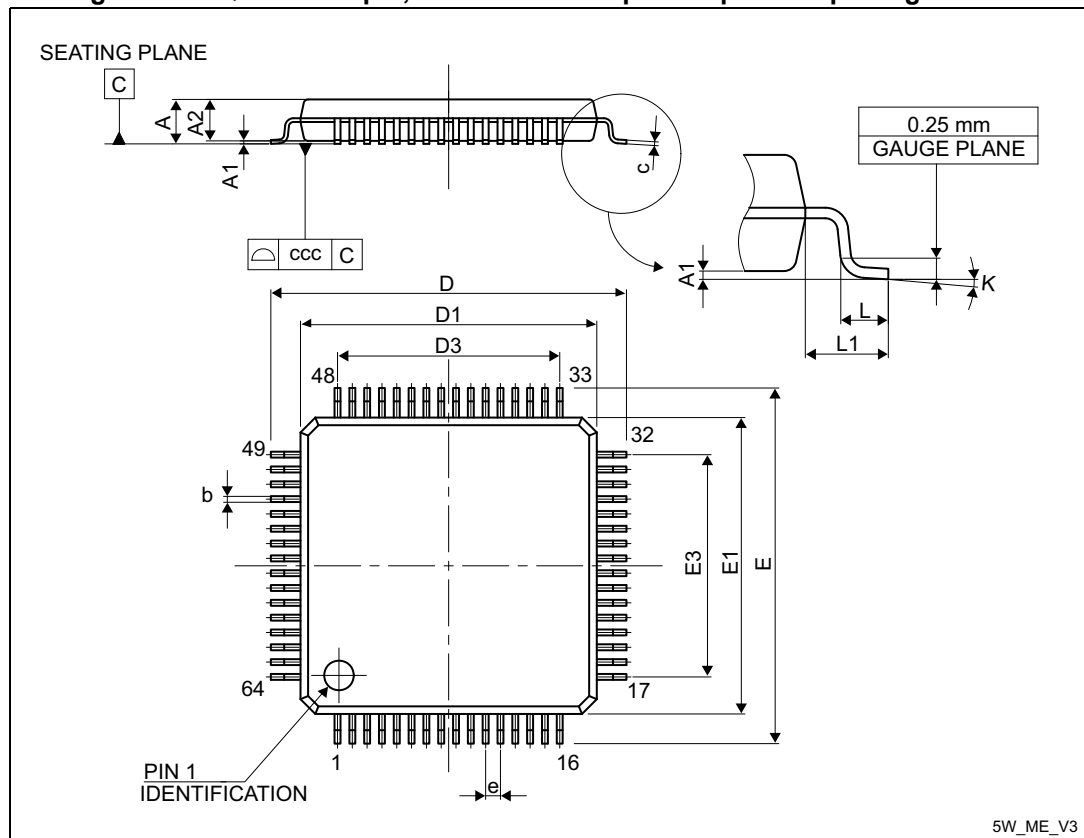
1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

## 6 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 6.1 LQFP64 package information

Figure 34. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

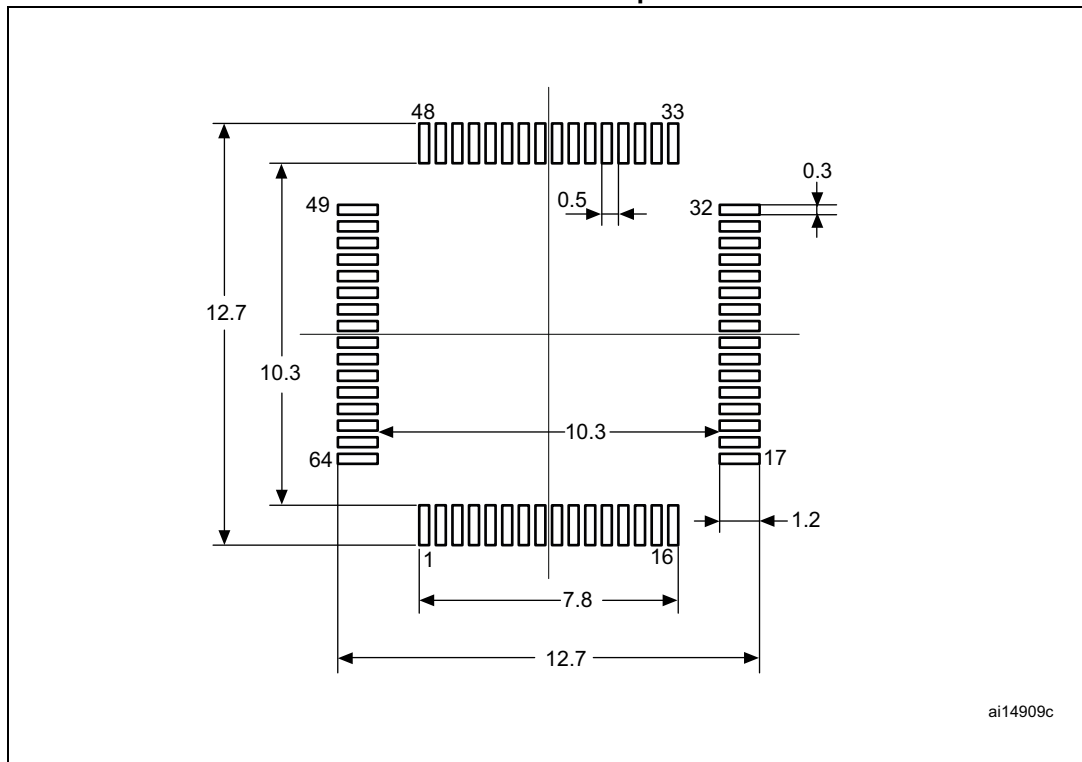
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

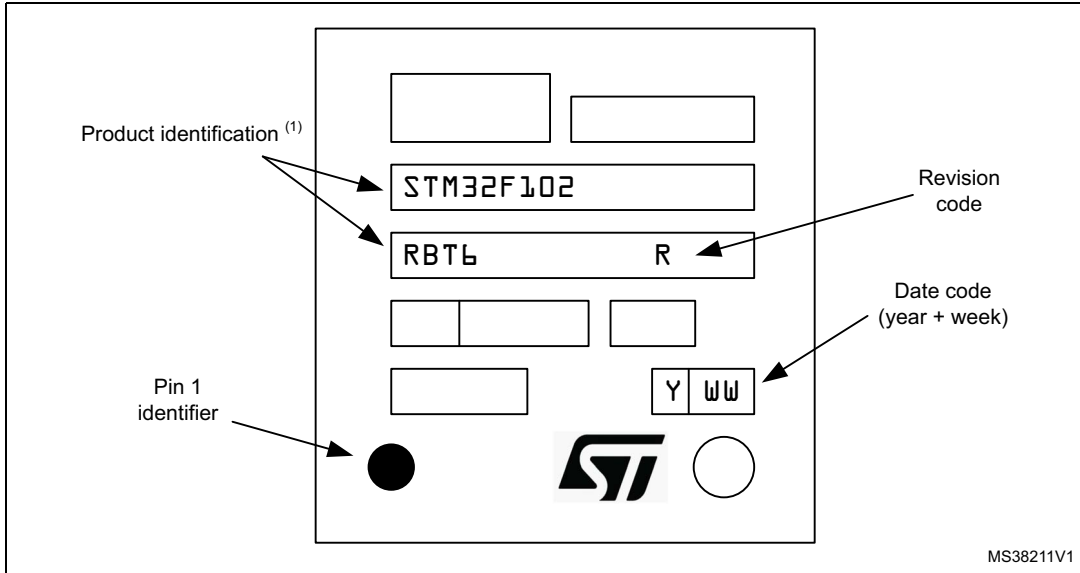


1. Dimensions are expressed in millimeters.

### Device marking for LQFP64

Figure 36 is an example of topside marking orientation versus pin 1 identifier location.

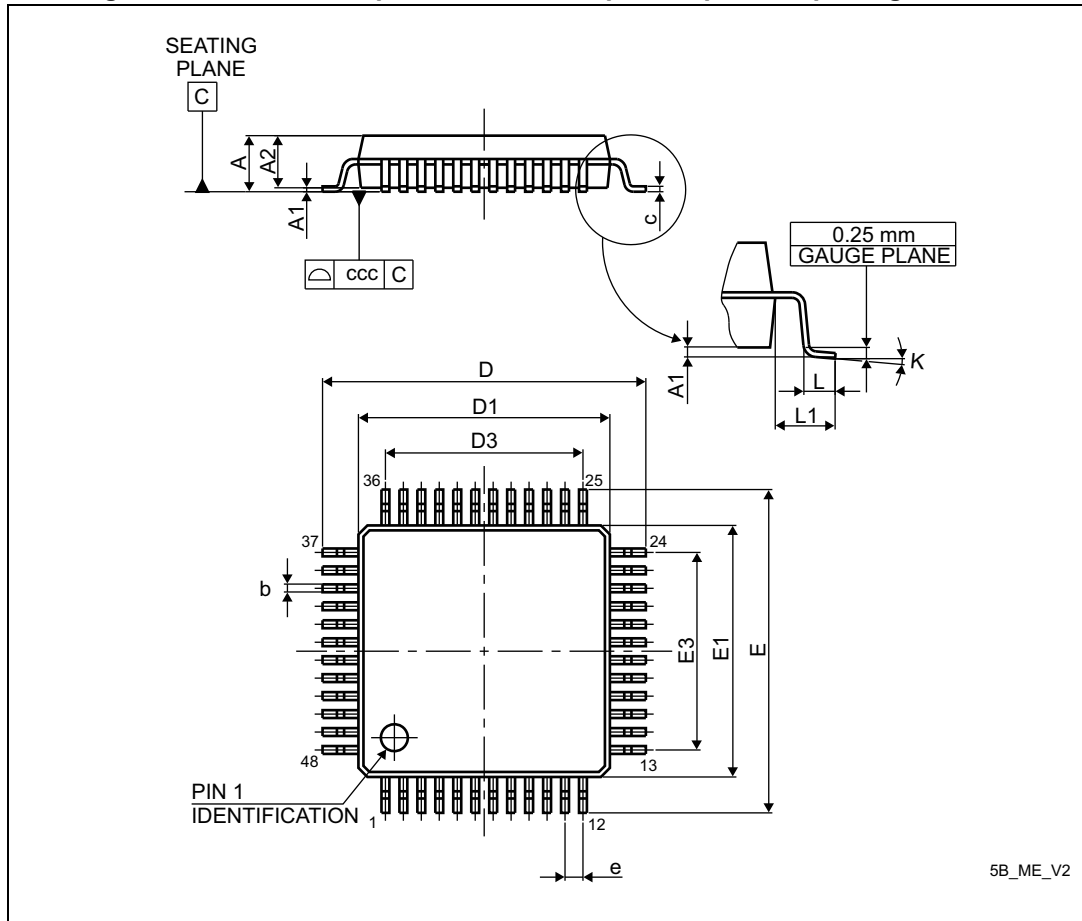
Figure 36. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 6.2 LQFP48 package information

Figure 37. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

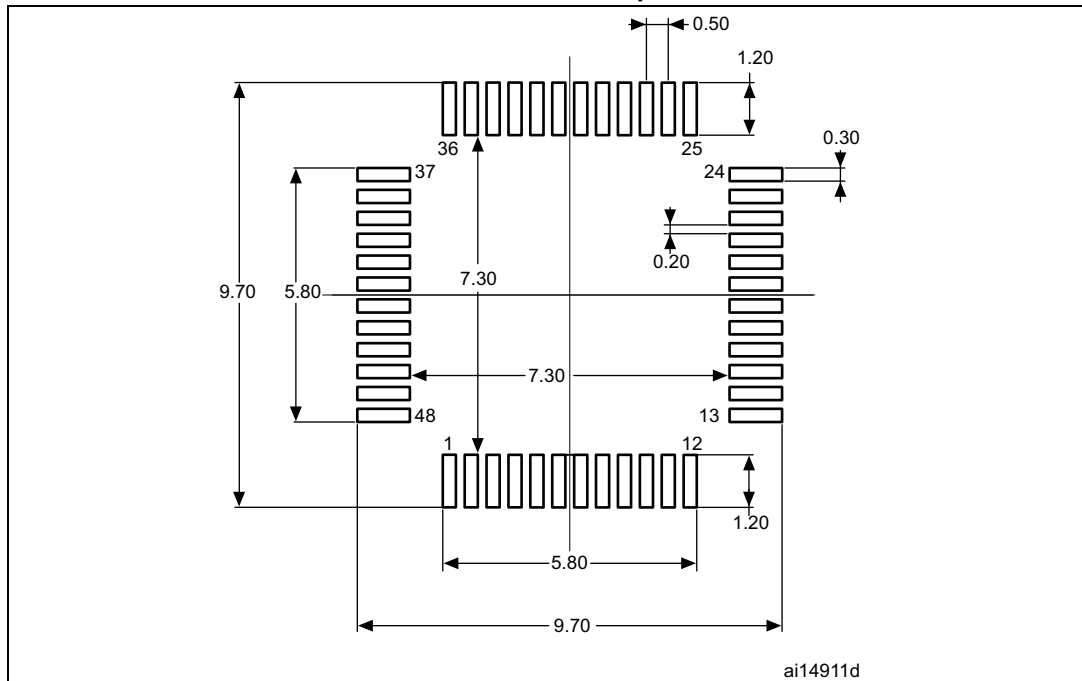
Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 38. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

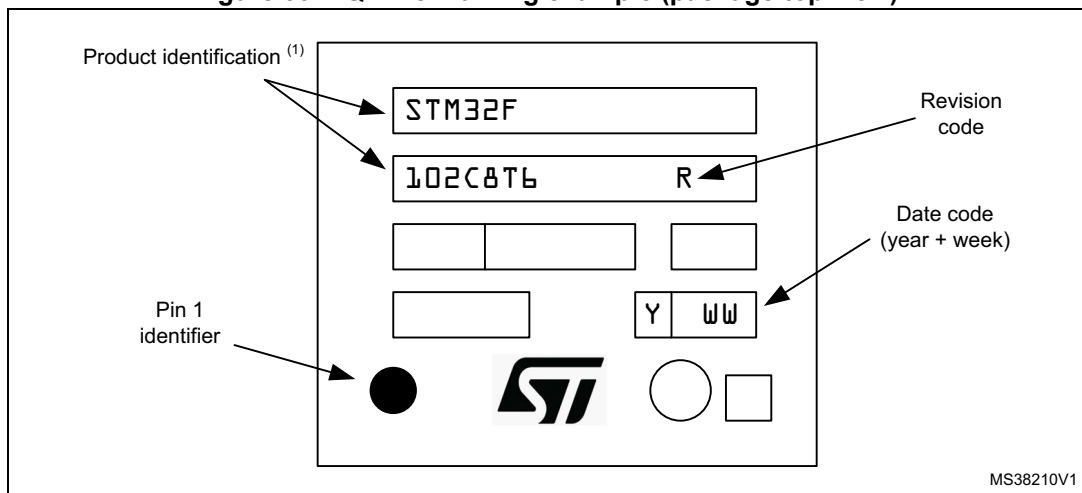


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

Figure 39 gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. LQFP48 marking example (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

### 6.3 Thermal characteristics

The maximum chip junction temperature ( $T_{Jmax}$ ) must never exceed the values given in [Table 8: General operating conditions](#).

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D$  max =  $P_{INT}$  max +  $P_{I/O}$ max),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 52. Package thermal characteristics**

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm / 0.5 mm pitch	55	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

### 6.4 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).

### 6.4.1 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 53: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (−40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F102xx junction temperature range.

#### Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 8 I/Os used at the same time in output mode at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 272\text{ mW}$

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus:  $P_{Dmax} = 447\text{ mW}$

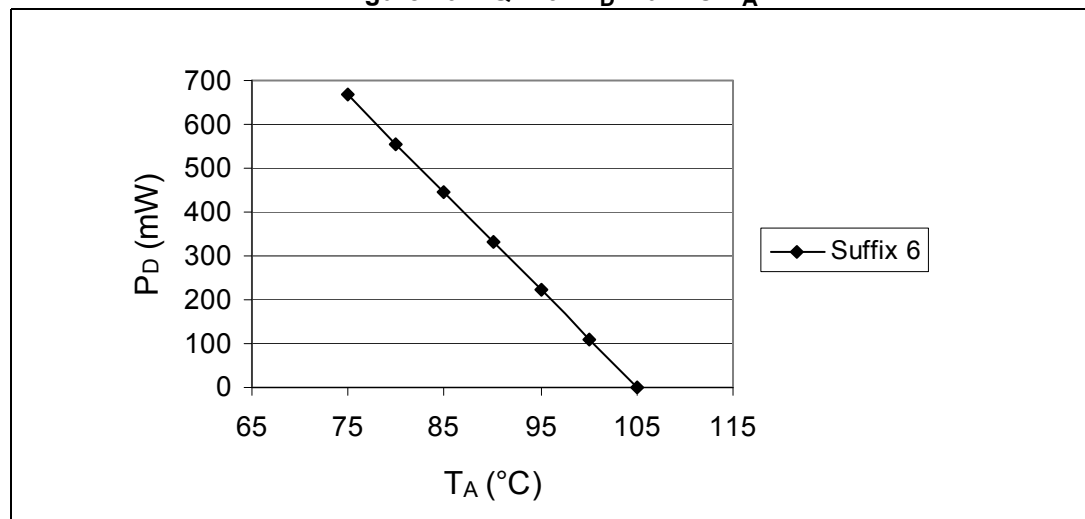
Using the values obtained in [Table 52](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64, 45 °C/W

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.1\text{ °C} = 102.1\text{ °C}$$

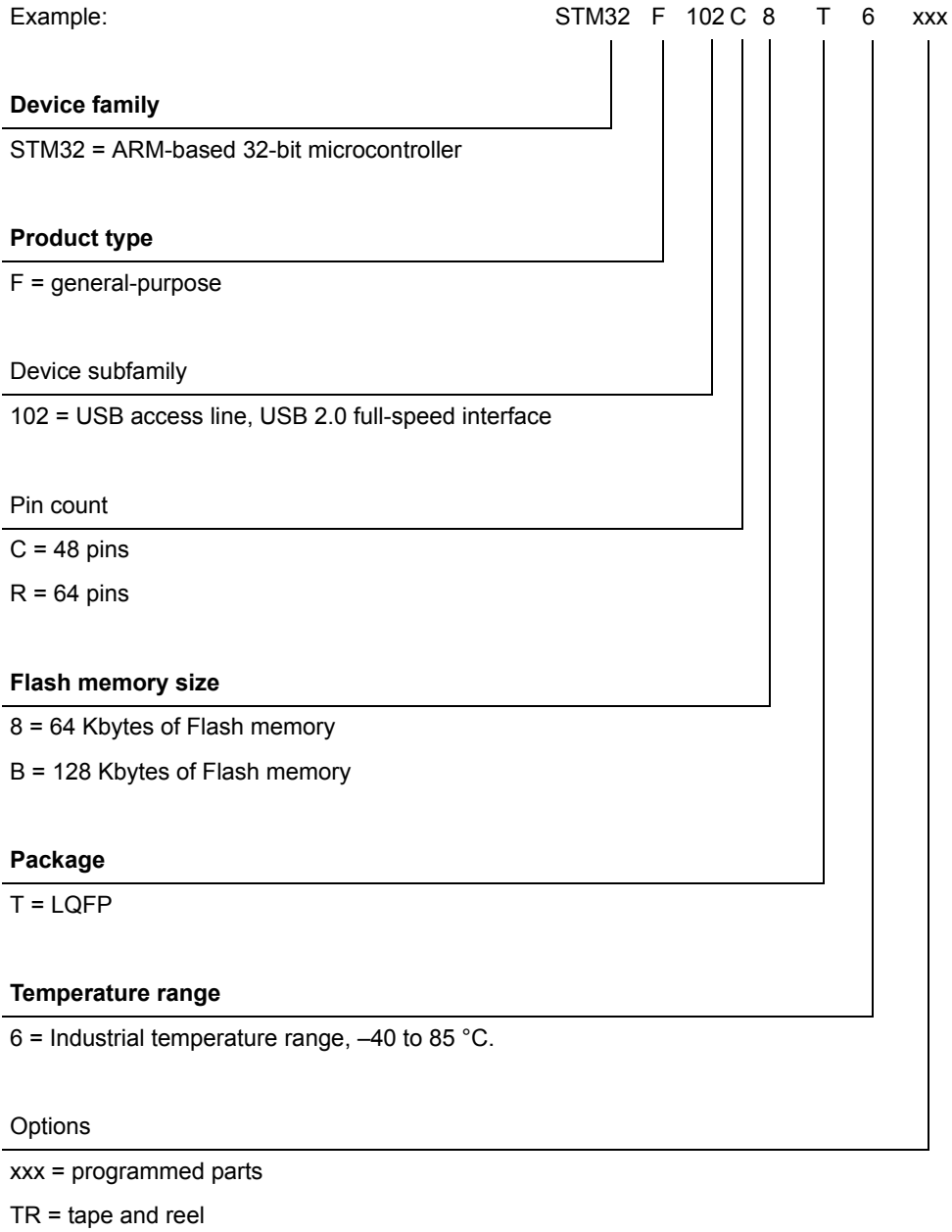
This is within the junction temperature range of the STM32F102xx (−40 <  $T_J$  < 105 °C).

Figure 40. LQFP64  $P_D$  max vs.  $T_A$



# 7 Ordering information scheme

**Table 53. Ordering information scheme**



## 8 Revision history

**Table 54. Document revision history**

Date	Revision	Changes
23-Sep-2008	1	Initial release.
23-Apr-2009	2	<p>I/O information clarified <i>on page 1</i>. <i>Figure 1: STM32F102T8 medium-density USB access line block diagram</i> and <i>Figure 5: Memory map</i> modified.</p> <p>In <i>Table 4: Medium-density STM32F102xx pin definitions</i>: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column.</p> <p>P<sub>D</sub> value added for LQFP64 package in <i>Table 8: General operating conditions</i>.</p> <p>Note modified in <i>Table 13: Maximum current consumption in Run mode, code with data processing running from Flash</i> and <i>Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM</i>. <i>Figure 13</i>, <i>Figure 14</i> and <i>Figure 15</i> show typical curves.</p> <p><i>Figure 31: ADC accuracy characteristics</i> modified.</p> <p><i>Figure 33: Power supply and reference decoupling</i> modified.</p> <p><i>Table 20: High-speed external user clock characteristics</i> and <i>Table 21: Low-speed external user clock characteristics</i> modified.</p> <p>ACC<sub>HSI</sub> max values modified in <i>Table 24: HSI oscillator characteristics</i>.</p> <p>Small text changes.</p>
22-Sep-2009	3	<p><i>Note 5</i>. updated in <i>Table 4: Medium-density STM32F102xx pin definitions</i>.</p> <p>V<sub>RERINT</sub> and T<sub>Coeff</sub> added to <i>Table 12: Embedded internal reference voltage</i>. Typical I<sub>DD_VBAT</sub> value added in <i>Table 16: Typical and maximum current consumptions in Stop and Standby modes</i>. <i>Figure 12: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values</i> added.</p> <p>f<sub>HSE_ext</sub> min modified in <i>Table 20: High-speed external user clock characteristics</i>.</p> <p>C<sub>L1</sub> and C<sub>L2</sub> replaced by C in <i>Table 22: HSE 4-16 MHz oscillator characteristics</i> and <i>Table 23: LSE oscillator characteristics (f<sub>LSE</sub> = 32.768 kHz)</i>, notes modified and moved below the tables. <i>Table 24: HSI oscillator characteristics</i> modified. Conditions removed from <i>Table 26: Low-power mode wakeup timings</i>.</p> <p><i>Note 1</i>. modified below <i>Figure 18: Typical application with an 8 MHz crystal</i>.</p> <p><i>Figure 25: Recommended NRST pin protection</i> modified.</p> <p>IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in <i>Section 5.3.10: EMC characteristics on page 48</i>.</p> <p>Jitter added to <i>Table 27: PLL characteristics</i>.</p> <p><i>Table 43: SPI characteristics</i> modified.</p> <p>C<sub>ADC</sub> and R<sub>AIN</sub> parameters modified in <i>Table 47: ADC characteristics</i>.</p> <p>R<sub>AIN</sub> max values modified in <i>Table 48: RAIN max for f<sub>ADC</sub> = 12 MHz</i>.</p> <p>Small text changes.</p>

Table 54. Document revision history (continued)

Date	Revision	Changes
27-Sep-2012	4	<p><i>Figure 2: Clock tree</i>: added FLITFCLK and <i>Note 3.</i>, and modified <i>Note 1.</i>.  Updated <i>Note 2.</i> in <i>Table 41: I2C characteristics</i>.  Updated <i>Figure 25: Recommended NRST pin protection</i>.  Changed <math>t_{w(SCKH)}</math> to <math>t_{w(SCLH)}</math>, <math>t_{w(SCKL)}</math> to <math>t_{w(SCLL)}</math>, <math>t_{r(SCK)}</math> to <math>t_{r(SCL)}</math>, <math>t_{f(SCK)}</math> to <math>t_{f(SCL)}</math>, and <math>t_{su(STA:STO)}</math> to <math>t_{w(STO:STA)}</math> in <i>Figure 26: I2C bus AC waveforms and measurement circuit(1)</i>.  Changed note for <math>I_{lkg}</math> and <math>R_{PU}</math> and updated <i>Note 1.</i> content in <i>Table 36: I/O static characteristics</i>. Updated text related to CMOS and TTL compliance and added <i>Figure 20</i>, <i>Figure 21</i>, <i>Figure 22</i>, and <i>Figure 23</i>.  Updated <i>Section : Output driving current</i>.  In <i>Table 43: SPI characteristics</i>, removed note 1 related to SPI1 remapped characteristics.  Added <math>DuCy_{(HSI)}</math> in <i>Table 24: HSI oscillator characteristics</i>.  <i>Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)</i>: removed note 2 related to oscillator selection, updated <i>Note 2.</i>, and <math>t_{SU(LSE)}</math> specified for various ambient temperature values.  Updated <i>Note 2.</i> and <i>Note 3.</i> below <i>Figure 35: Recommended footprint (dimensions in mm)<sup>(1)(2)(3)</sup></i>.  <i>Table 37: Output voltage characteristics</i>: updated <math>V_{OL}</math> and <math>V_{OH}</math> conditions for TTL and CMOS outputs and added <i>Note 2.</i>  Replaced “TBD” by “-” for “max” specification of “Supply current in Standby mode” in <i>Table 16: Typical and maximum current consumptions in Stop and Standby modes</i>.  Removed “except for analog inputs” from paragraph “GPIOs (general-purpose inputs/outputs) in <i>Chapter 2.3: Overview</i>.  Updated <math>t_{w(HSE)}</math> min value in <i>Table 20: High-speed external user clock characteristics</i>.  Added <i>Note 2.</i> in <i>Table 5: Voltage characteristics</i>.  Updated <i>Note 3.</i>, <i>Note 4.</i> and <i>Note 5.</i> in <i>Table 6: Current characteristics</i>.  Updated <i>Note 1.</i> in <i>Table 38: I/O AC characteristics</i>.  Added <i>Chapter 5.3.12: I/O current injection characteristics</i>.  Updated <i>Note 2.</i> in <i>Table 41: I2C characteristics</i>.  Updated “Output driving current” paragraph in <i>Chapter 5.3.13: I/O port characteristics</i>.  Removed Note 4 and updated <i>Note 3.</i> in <i>Table 41: I2C characteristics</i>.  Updated <i>Figure 29: SPI timing diagram - master mode(1)</i> (SCK Output instead of Input).  Replaced every occurrence of USBDP or USBDM by USB_DP or USB_DM, respectively.</p>

Table 54. Document revision history (continued)

Date	Revision	Changes
02-Aug-2013	5	<p>Removed sentence in “Unless otherwise specified the parameters ...” in <i>I2C interface characteristics</i> section.</p> <p>Added <math>V_{IN}</math> in <i>Table 8: General operating conditions</i>.</p> <p>Added note 5 in <i>Table 23: HSI oscillator characteristics</i></p> <p>Modified charge device model in <i>Table 33: ESD absolute maximum ratings</i></p> <p>Updated ‘<math>V_{IL}</math>’ and ‘<math>V_{IH}</math>’ in <i>Table 34: I/O static characteristics</i></p> <p>Added notes to <i>Figure 20: Standard I/O input characteristics - CMOS port</i>, <i>Figure 21: Standard I/O input characteristics - TTL port</i>, <i>Figure 22: 5 V tolerant I/O input characteristics - CMOS port</i> and <i>Figure 23: 5 V tolerant I/O input characteristics - TTL port</i></p> <p>Updated <i>Figure 24: I/O AC characteristics definition</i></p> <p>Updated note 2. and 3. in <i>Table 39: I<sup>2</sup>C characteristics</i></p> <p>Updated <i>Figure 26: I2C bus AC waveforms and measurement circuit(1)</i></p> <p>Updated title of <i>Table 40: SCL frequency (<math>f_{PCLK1} = 36</math> MHz, <math>V_{DD\_I2C} = 3.3</math> V)</i></p> <p>Updated <i>Table 47: ADC characteristics</i></p> <p>Updated <i>Section 6.1: Package mechanical data</i></p>
03-Jun-2015	6	<p>Updated <i>Table 18: Peripheral current consumption</i> and <i>Table 39: I<sup>2</sup>C characteristics</i></p> <p>Updated <i>Section 6: Package characteristics</i></p> <p>Updated <i>Section 6.1: LQFP64 package information</i> with addition of <i>Device marking for LQFP64</i> and <i>Figure 36</i>.</p> <p>Updated <i>Section 6.2: LQFP48 package information</i> with addition of <i>Device marking for LQFP48</i> and <i>Figure 39</i>.</p> <p>Updated Disclaimer.</p>

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