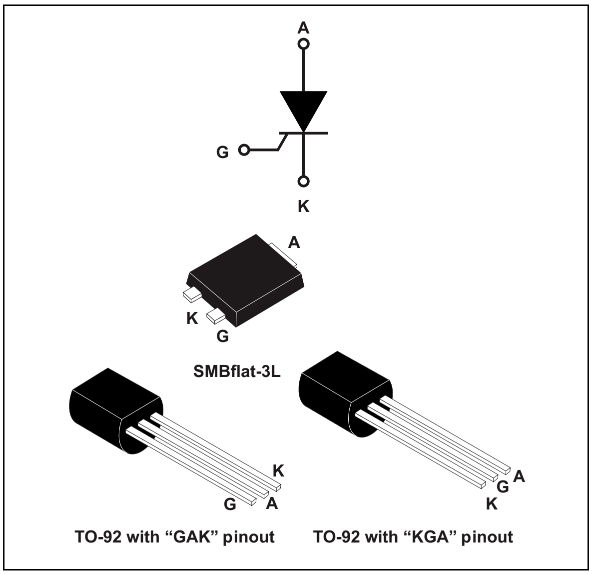
TS110-8

High surge voltage 1.25 A SCR for circuit breaker

Datasheet - production data



Features

- On-state rms current, 1.25 A
- Repetitive peak off-state voltage, 800 V
- Non-repetitive direct surge peak off-state voltage, 1250 V
- Non-repetitive reverse surge peak off-state voltage, 900 V
- Triggering gate current, 100 µA
- High off-state immunity: 200 V/µs
- ECOPACK®2 compliant component

Applications

- GFCI (Ground Fault Circuit Interrupter)
- AFCI (Arc Fault Circuit Interrupter)
- RCD (Residual Current Device)
- RCBO (Residual Current circuit Breaker with Overload protection)
- AFDD (Arc Fault Detection Device)

Description

Thanks to highly sensitive triggering levels, the TS110-8 series is suitable for circuit breaker applications where the available gate current is limited.

The 1250 V direct surge voltage capability of the TS110-8 enables high robustness of the whole circuit breaker. The low leakage current of the TS110-8 reduces power consumption over the entire lifetime of the circuit breaker. The high off-state immunity (200 V/µs) insures the non tripping of the breaker in case of electrical fast transient (EFT) on the mains.

The TS110-8 is available in through-hole TO-92 package with GAK and KGA pinout and in SMBflat-3L package.

Table 1. Device summary

Symbol	Value	Unit
$I_{T(RMS)}$	1.25	A
V_{DRM}, V_{RRM}	800	V
V_{DSm}, V_{RSM}	1250, 900	V
I_{GT}	100	µA
T_j	125	°C

1 Characteristics

Table 2. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	On-state rms current (180° conduction angle)	TO-92	T_l = 53 °C	1.25	A
		SMBflat-3L	T_c = 109 °C		
$IT_{(AV)}$	Average on-state current (180° conduction angle)	TO-92	T_l = 53 °C	0.8	A
		SMBflat-3L	T_c = 109 °C		
I_{TSM}	Non repetitive surge peak on-state current	t_p = 8.3 ms	$T_{j\ initial}$ = 25 °C	21	A
		t_p = 10 ms		20	
	1st step: one surge every 5 seconds, 25 surges 2nd step: one surge every 5 seconds, 25 surges	t_p = 10 ms	T_{amb} = 90 °C	25 times 12 A 25 times 16 A	
I^2t	I^2t Value for fusing	t_p = 10 ms, 25 °C		2	A^2s
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns	F = 50 Hz, 125 °C		100	A/µs
	Non repetitive critical current rate of rise at break-over, see *Figure 17*, $V_D > V_{DSm}$			200	
V_{DRM}, V_{RRM}	Repetitive peak off-state AC voltage, R_{GK} = 220 Ω		T_j = 125 °C	800	V
V_{DSm}	Non-repetitive direct surge peak off-state voltage, R_{GK} = 220 Ω	t_p = 10 ms	T_j = 25 °C	1250	V
V_{RSM}	Non-repetitive reverse surge peak off-state voltage, R_{GK} = 220 Ω	t_p = 10 ms	T_j = 25 °C	900	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125 °C	1.2	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	0.2	W
T_{stg}	Storage junction temperature range			- 40 to + 150	°C
T_j	Operating junction temperature range			- 40 to + 125	

Table 3. Electrical characteristics

Symbol	Test conditions			Value	Unit
I_{GT}	V_D = 12 V, R_L = 140Ω	T_j = 25 °C	Min.	1	µA
			Max.	100	
V_{GT}			Max.	0.8	V
V_{GD}	$V_D = V_{DRM}$, R_L = 33 kΩ, R_{GK} = 220 Ω	T_j = 125 °C	Min.	0.1	V
V_{RG}	I_{RG} = 2 mA	T_j = 25 °C	Min.	7.5	V
I_H	I_T = 50 mA, R_{GK} = 220 Ω	T_j = 25 °C	Max.	12	mA
I_L	I_G = 5 mA, R_{GK} = 220 Ω	T_j = 25 °C	Max.	12	mA
dV/dt	V_D = 67% V_{DRM}, R_{GK} = 220 Ω	T_j = 125 °C	Min.	200	V/µs

Table 4. Static electrical characteristics

Symbol	Test conditions			Value	Unit
V_{TM}	I_{TM} = 2.5 A, t_p = 380 µs	T_j = 25 °C	Max.	1.6	V
V_{T0}	Threshold voltage	T_j = 125 °C	Max.	0.95	V
R_D	Dynamic resistance	T_j = 125 °C	Max.	220	mΩ
I_{DRM} I_{RRM}	$V_D = V_{DRM} / V_{RRM}$, R_{GK} = 220 Ω	T_j = 25 °C	Max.	1	µA
		T_j = 125 °C		100	µA

Table 5. Thermal resistance

Symbol	Parameter			Value	Unit
$R_{th(j-l)}$	Junction to leads (DC)		TO-92	65	°C/W
$R_{th(j-a)}$	Junction to ambient (DC)		TO-92	160	
		S = 5 cm^2	SMBflat-3L	75	
$R_{th(j-c)}$	Junction to case (DC)		SMBflat-3L	14	

Figure 1. Maximum average power dissipation versus average on-state current

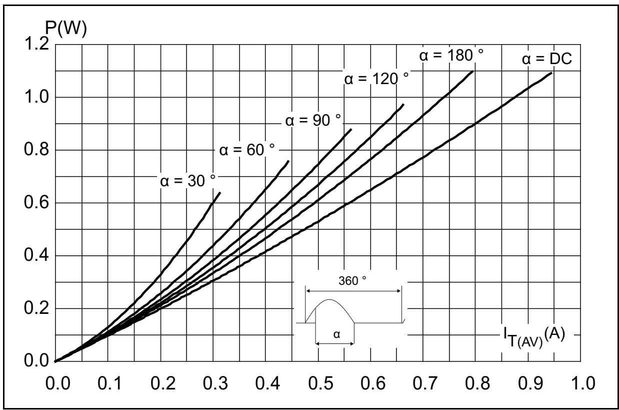


Figure 2. Average and DC on-state current versus lead temperature (TO-92)

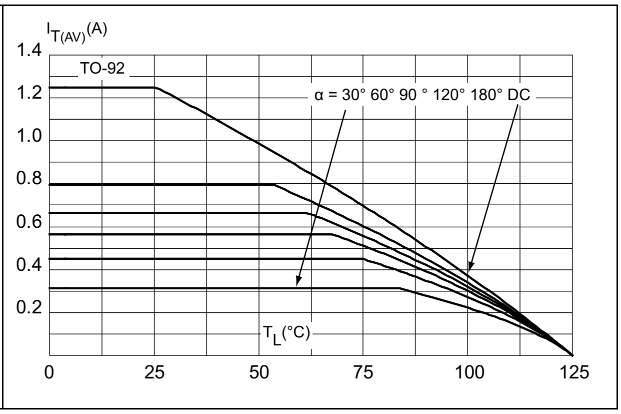


Figure 3. Average and DC on-state current versus case temperature (SMBflat-3L)

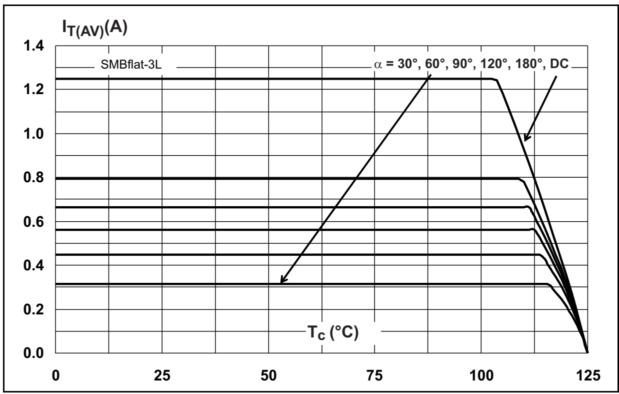


Figure 4. Average and DC on-state current versus ambient temperature

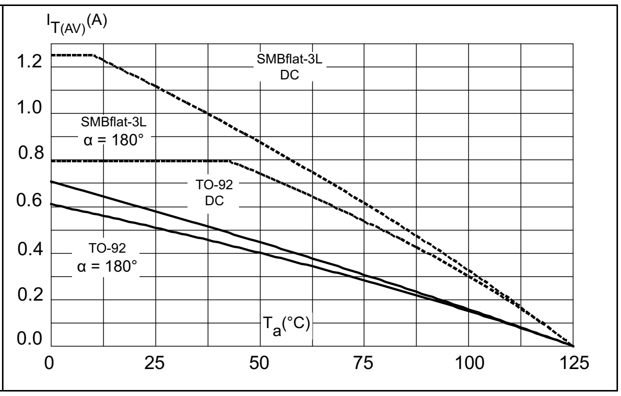


Figure 5. Relative variation of thermal impedance junction to ambient versus pulse duration

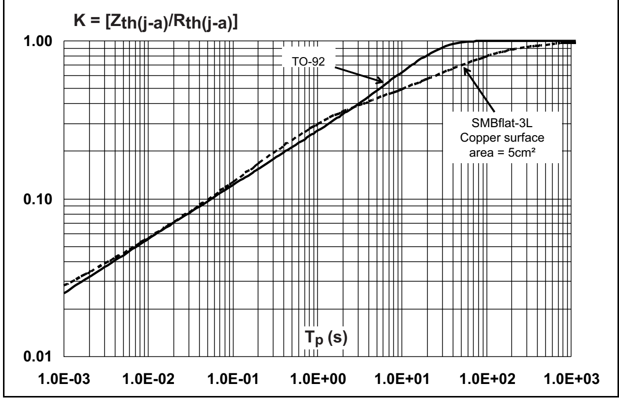


Figure 6. Typical thermal resistance junction to ambient versus copper surface under anode (epoxy FR4, Cu_{th} = 35 µm)

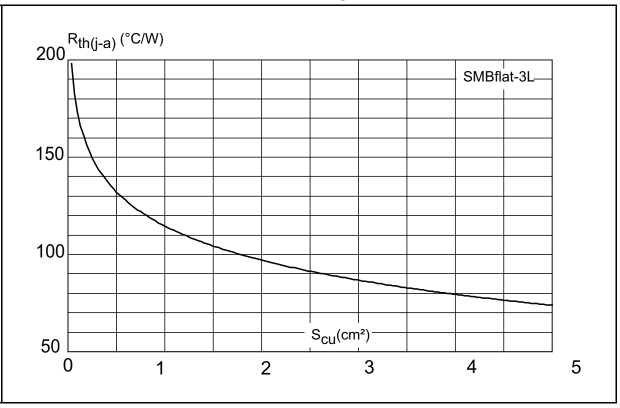


Figure 7. Relative variation of gate trigger current and trigger voltage versus junction temperature (typical values)

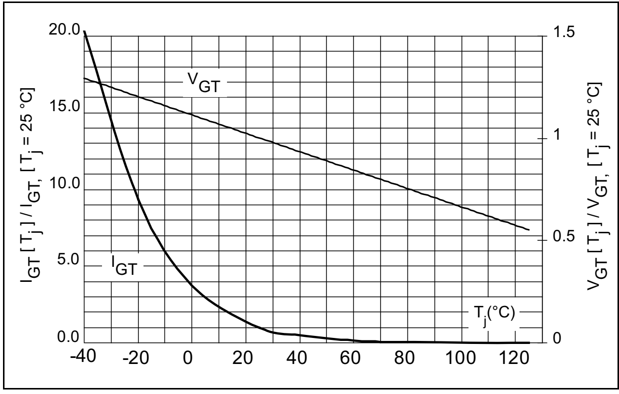


Figure 8. Relative variation of latching and holding current versus junction temperature (typical values)

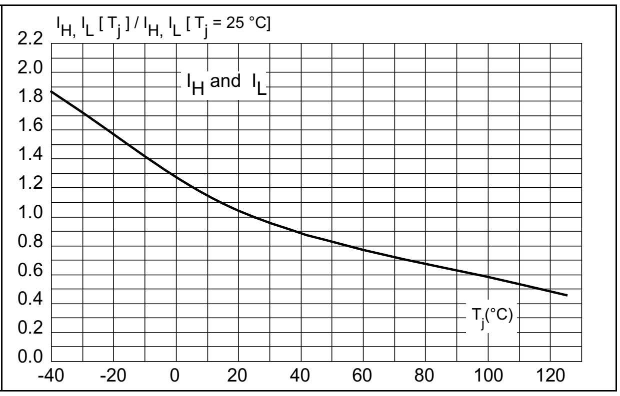


Figure 9. Relative variation of holding current versus gate-cathode resistance (typical values)

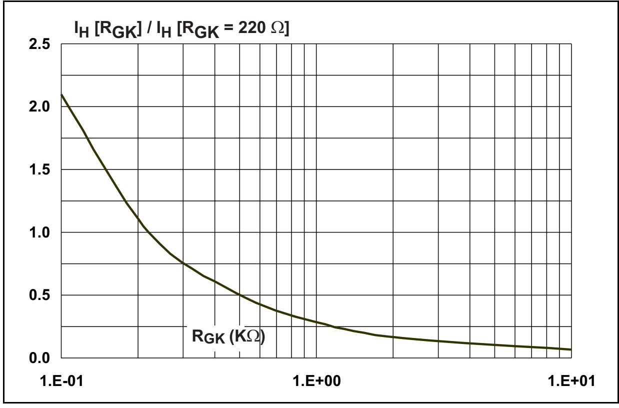
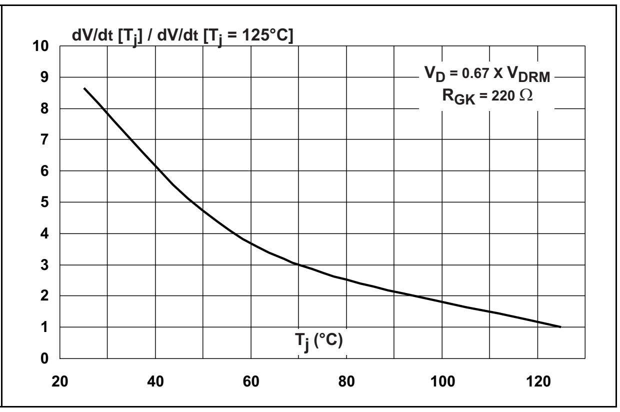


Figure 10. Relative variation of dV/dt immunity versus junction temperature (typical values)



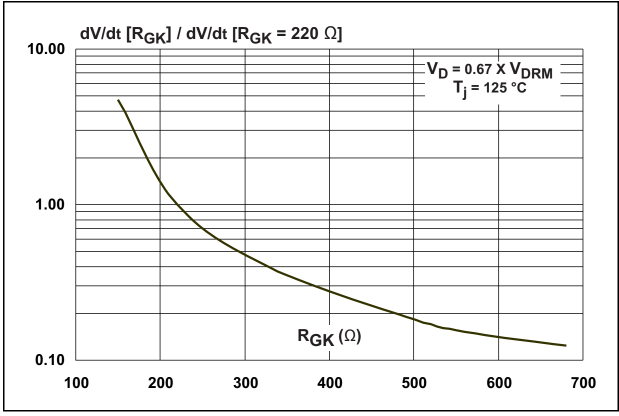


Figure 11. Relative variation of dV/dt immunity versus gate-cathode resistance (typical values)

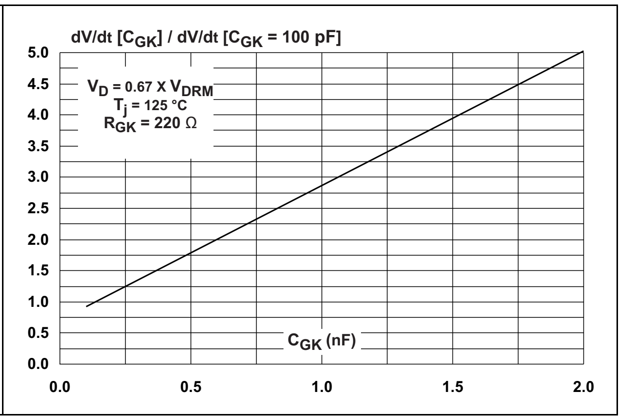


Figure 12. Relative variation of dV/dt immunity versus gate-cathode capacitor (typical values)

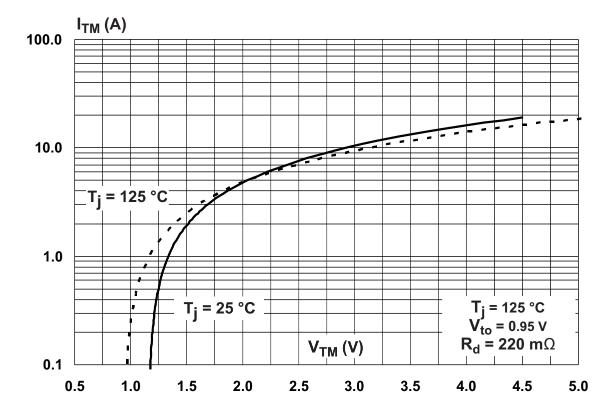


Figure 13. On-state characteristics (maximum values)

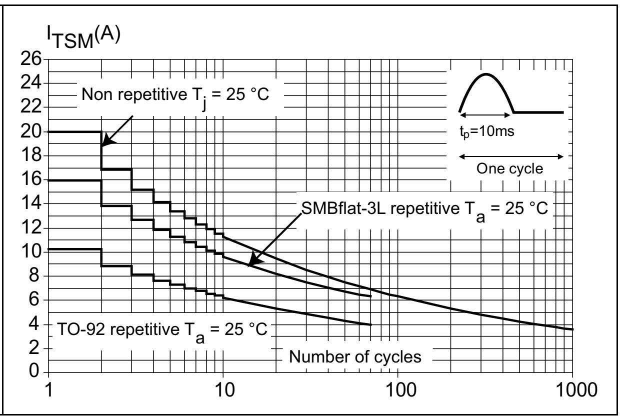


Figure 14. Surge peak on-state current versus number of cycles

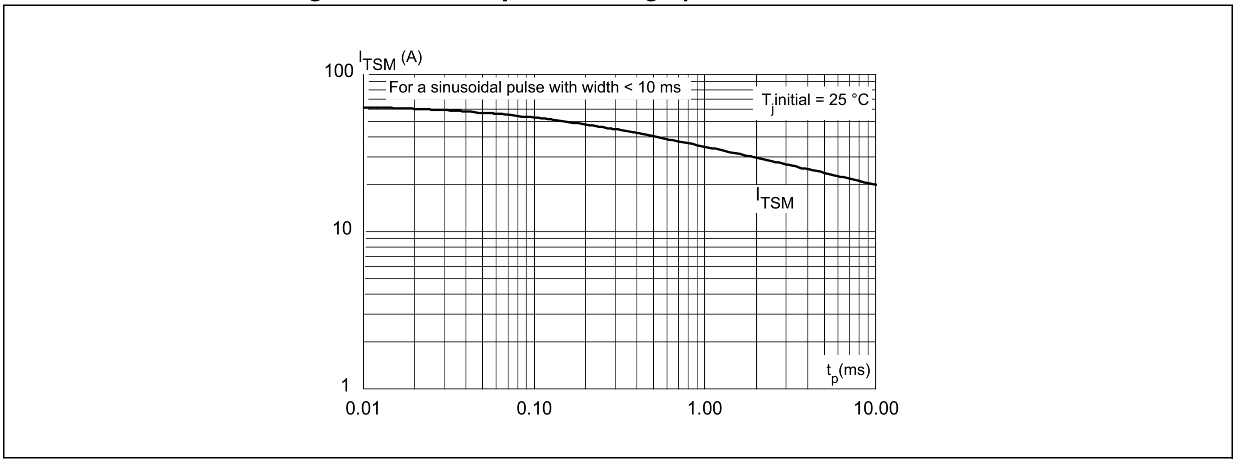


Figure 15. Non repetitive surge peak on-state current

2 AC line transient voltage ruggedness

In comparison with standard SCRs, the TS110-8 is self-protected against over-voltage. The TS110-8 switch can safely withstand AC line direct surge voltages by switching to the on state (for less than 10 ms on 50 Hz mains) to dissipate energy shocks through the load. The load limits the current through the TS110-8. The self-protection against over-voltage is based on an overvoltage crowbar technology. This safety feature works even with high turn-on current ramp up.

Figure 16 represents the TS110-8 in a test environment. It is used to stress the TS110-8 switch according to the IEC 61000-4-5 standard conditions. The TS110-8 folds back safely to the on state as shown in *Figure 17*.

The TS110-8 recovers its blocking voltage capability after the direct surge and the next zero current crossing. Such a non repetitive test can be done at least 10 times.

Figure 16. Overvoltage ruggedness test circuit for IEC 61000-4-5 standards

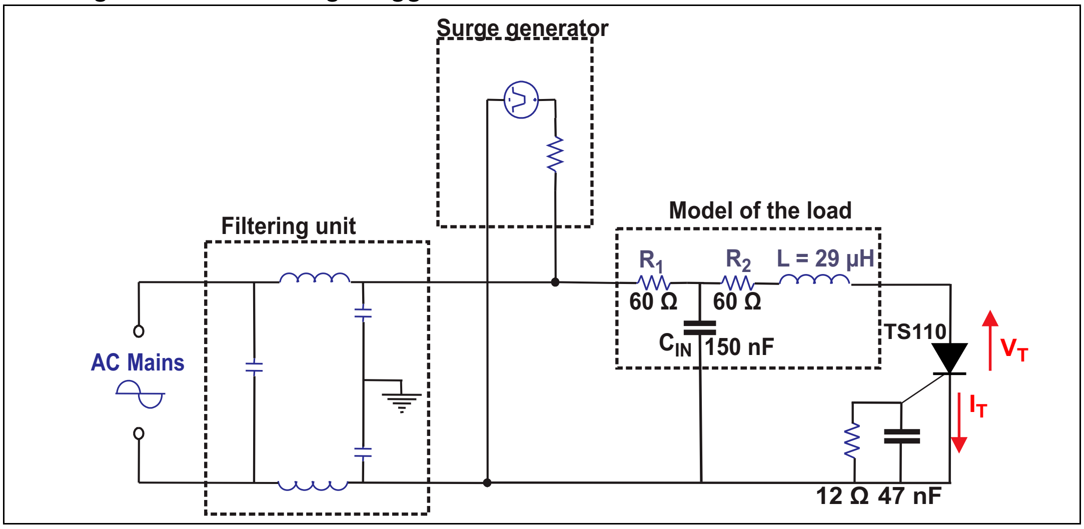
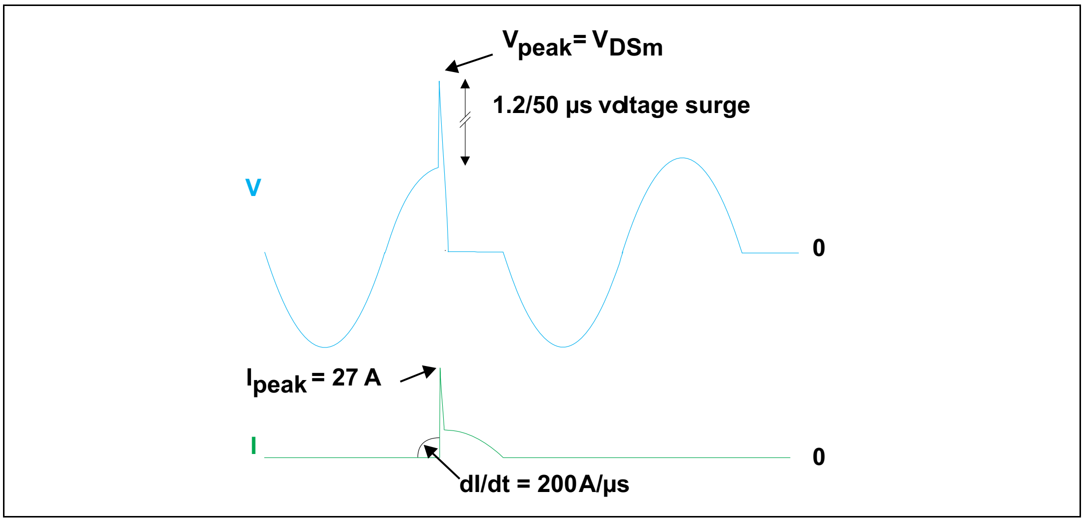


Figure 17. Typical current and voltage waveforms across the TS110-8 during IEC 61000-4-5 standard test



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 18. TO-92 dimensions (definitions)

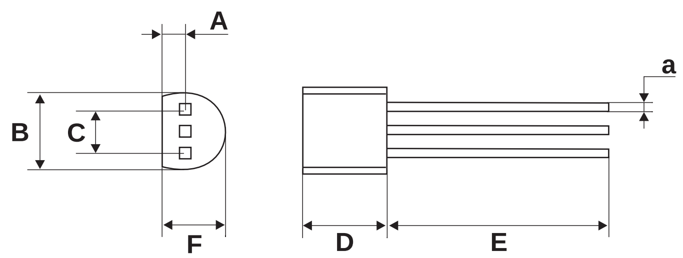


Table 6. TO-92 dimensions (values)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		1.35			0.053	
B			4.70			0.185
C		2.54			0.100	
D	4.40			0.173		
E	12.70			0.500		
F			3.70			0.146
a			0.5			0.019

For ammopack packing information, please contact your sales representative.

Figure 19. SMBflat-3L dimensions (definitions)

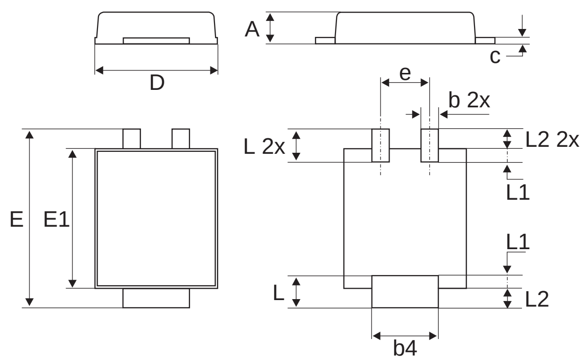
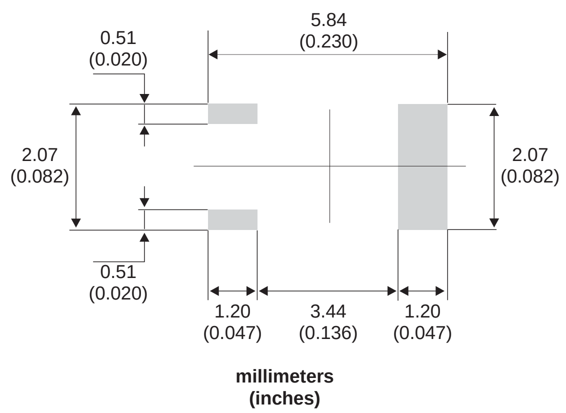


Table 7. SMBflat-3L dimensions (values)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.10	0.035		0.043
b	0.35		0.65	0.014		0.026
b4	1.95		2.20	0.07		0.087
c	0.15		0.40	0.006		0.016
D	3.30		3.95	0.130		0.156
E	5.10		5.60	0.201		0.220
E1	4.05		4.60	0.156		0.181
L	0.75		1.50	0.030		0.059
L1		0.40			0.016	
L2		0.60			0.024	
e		1.60			0.063	

Figure 20. SMBflat-3L footprint dimensions



4 Ordering information

Figure 21. Ordering information scheme

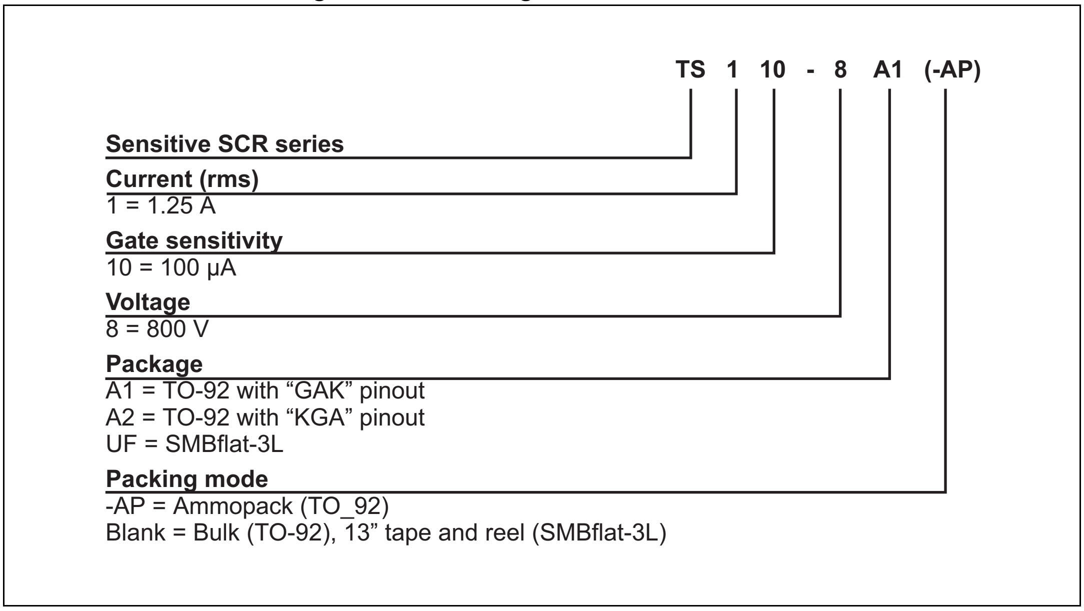


Table 8. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TS110-8A1	TS110-8	T0-92	200 mg	2500	Bulk
TS110-8A1-AP	TS110-8			2000	Ammopack
TS110-8A2	TS110-8	T0-92	200 mg	2500	Bulk
TS110-8A2-AP	TS110-8			2000	Ammopack
TS110-8UF	TS110-8	SMBflat-3L	47 mg	5000	Tape and reel 13”

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Oct-2014	1	Initial release.