DRV2510-Q1 3-A Automotive Haptic Driver for Solenoids and Voice Coils with Integrated Diagnostics

1 Features

- Wide Operating Voltage (4.5 V - 18 V)
- Integrated Load-Dump Protection (40 V)
- High Current Drive (3 A Peak)
- Low $R_{DS(on)}$, Full H-Bridge Output
- Integrated Diagnostics
- Integrated Fault Protection
  - 40-V Load Dump Protection per ISO-7637-2
  - Short-Circuit Protection
  - Over-temperature Protection
  - Over-Voltage and Under-Voltage Protection
  - Fault Reporting
- Analog Input
- I^2C Communication
- Dedicated Interrupt Pin
- Qualified According to AEC-Q100 Grade 2
- –40ºC to 125ºC Ambient Temperature Range
- ISO9000: 2002 TS16949 Certified

2 Applications

- Electromagnetic Actuator Driver
  - Voice Coil
  - Solenoid
- Mechanical Button Replacement
- Automotive Haptic Applications
  - Infotainment
  - Center-Console
  - Steering Wheel
  - Door-Panel
  - Seats

3 Description

The DRV2510-Q1 device is a high current haptic driver specifically designed for inductive loads, such as solenoids and voice coils.

The output stage consists of a full H-bridge capable of delivering 3 A of peak current.

The DRV2510-Q1 device provides protection functions such as undervoltage lockout, over-current protection and over-temperature protection.

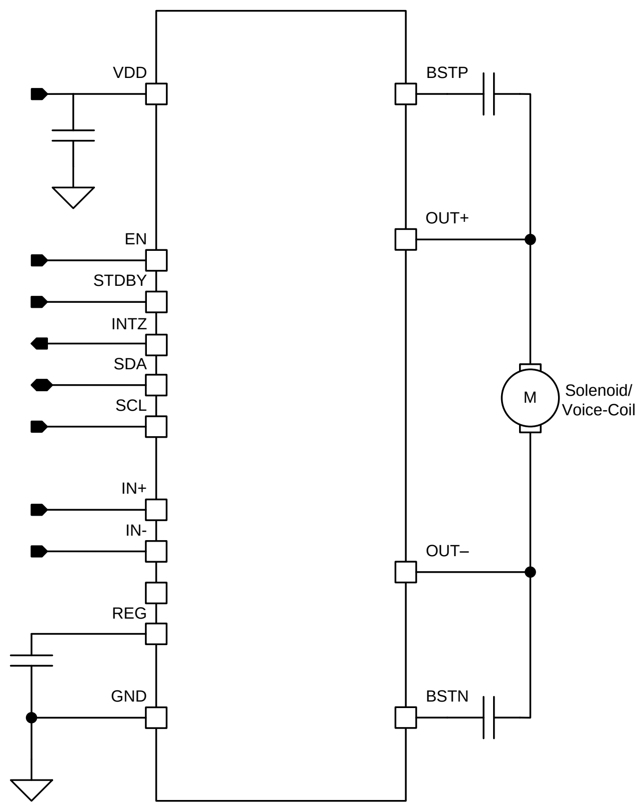
The DRV2510-Q1 device is automotive qualified. The integrated load-dump protection reduces external voltage clamp cost and size, and the onboard load diagnostics report the status of the actuator through the digital interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV2510-Q1	HTSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2016) to Revision B **Page**

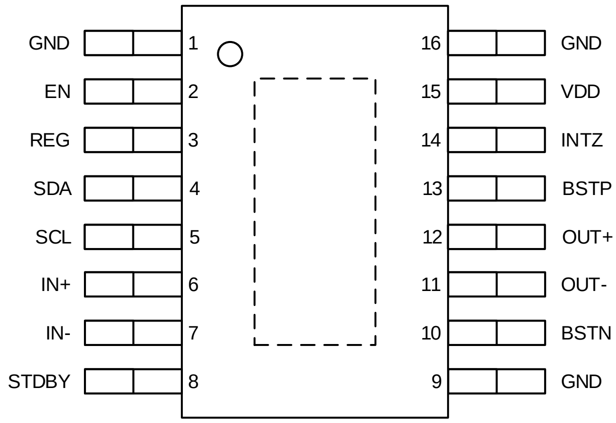
- Changed Feature From: Wide Operating Voltage (5 V – 18 V) To: Wide Operating Voltage (4.5 V – 18 V) 1
- Changed Feature From: Automotive Qualified (Q100) To: Qualified According to AEC-Q100 Grade 2 1
- Added Feature: ISO9000: 2002 TS16949 Certified 1
- Changed the VDD MIN value From: 5 V to: 4.5 V in the *Recommended Operating Conditions* 4
- Changed From: operates from 5 V – 18 V To: operates from 4.5 V – 18 V in the *Power Supply Recommendations* 22

Changes from Original (June 2016) to Revision A **Page**

- Released as Production Data. 1

5 Pin Configuration and Functions

TWP
HTSSOP 16-Pin With Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 9, 16	P	Ground.
EN	2	I	Device enable pin.
REG	3	P	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the MODE resistor divider.
SDA	4	I	I^2C data.
SCL	5	I	I^2C clock.
IN+	6	I	Positive differential input.
IN-	7	I	Negative differential input.
STDBY	8	I	Standby pin.
BSTN	10	P	Boot strap for negative output, connect to 220 nF X5R, or better ceramic cap to OUT-.
OUT-	11	O	Negative output.
OUT+	12	O	Positive output.
BSTP	13	P	Boot strap for positive output, connect to 220 nF X5R, or better ceramic cap to OUT+.
INTZ	14	O	General fault reporting. Open drain. INTZ = High, normal operation INTZ = Low, fault condition
VDD	15	P	Power supply.
Thermal Pad		G	Connect to GND for best system performance. If not connected to GND, leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	VDD DC supply voltage range	–0.3	30	V
	VDD pulsed supply voltage range. t < 400 ms exposure	–1	40	
	VDD supply voltage ramp rate		15	V/ms
Input voltage, V_I	SCL, SDA, EN	–0.3	5	V
	IN+, IN-, STDBY	–0.3	6.5	
Current	DC current on VDD, GND, OUT+, OUT-	–4	4	A
	Maximum current in all input pins	–1	1	mA
	Maximum sink current for open-drain pins		7	
Operating free-air temperature, T_A		–40	125	°C
Storage temperature range, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage. VDD.	4.5		18	V
V_{IH}	High-level input voltage. SDA, SCL, STDBY, EN.	2.1			V
V_{IL}	Low-level input voltage. SDA, SCL, STDBY, EN			0.7	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.4			V
I_{IH}	High-level input current. SDA, SCL, STDBY, EN			50	µA
R_L	Minimum load Impedance		1.5		Ω
C_B	Load capacitance for each bus line (SDA/SCL)			400	pF

6.4 Thermal Information

THERMAL METRIC[1]		DRV2510-Q1	UNIT
		PWP (HTSSOP)	
		{16} PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, AVCC = VDD = 12 V, R_L = 5 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\mid V_{OS} \mid$	Output offset voltage (measured differentially)	V_I = 0 V, Gain = 20 dB	–25		25	mV
I_{VDD}	Quiescent supply current	No load or filter		16		mA
$I_{VDD(SD)}$	Quiescent supply current in shutdown mode	No load or filter		5	20	µA
$I_{VDD(STDBY)}$	Quiescent supply current in standby mode	No load or filter		7		mA
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	T_J = 25°C		180		mΩ
G	Gain	$P_{(o)}$ = 1 W	19	20	21	dB
			25	26	27	
			31	32	33	dB
			35	36	37	
V_{REG}	Regulator voltage		6.4	6.9	7.4	V
V_O	Output voltage (measured differentially)			20		V
PSRR	Power supply ripple rejection	VDD = 12 V + 1 Vrms at 1 kHz		75		dB
V_{ICMIN}	Input common-mode min			0.3		V
V_{ICMAX}	Input common-mode max			4.4		
CMRR	Common-mode rejection ratio	f = 1 kHz, 100 mVrms referenced to GND. Gain = 20 dB		63		dB
f_{OSC}	Oscillator frequency (with PWM duty cycle < 96%)			400		kHz
				500		
	Output resistance in shutdown			10		MΩ
	Resistance to detect a short from OUT pin(s) to VDD or GND				200	Ω
	Open-circuit detection threshold		75	95	120	Ω
	Short-circuit detection threshold		0.9	1.2	1.5	Ω
	Power-on threshold			4.1		V
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C
	Over-current trip point			3.5		A
	Over-voltage trip point			21		V
	Over-voltage hysteresis			0.6		V
	Under-voltage trip point			4		V
	Under-voltage hysteresis			0.25		V

6.6 Timing Requirements

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Frequency at the SCL pin with no wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high	0.6			µs
$t_{w(L)}$	Pulse duration, SCL low	1.3			µs
$t_{su(1)}$	Setup time, SDA to SCL	100			ns
$t_{h(1)}$	Hold time, SCL to SDA	300			ns
$t_{(BUF)}$	Bus free time between stop and start condition	1.3			µs
$t_{su(2)}$	Setup time, SCL to start condition	0.6			µs
$t_{h(2)}$	Hold time, start condition to SCL	0.6			µs
$t_{su(3)}$	Setup time, SCL to stop condition	0.6			µs

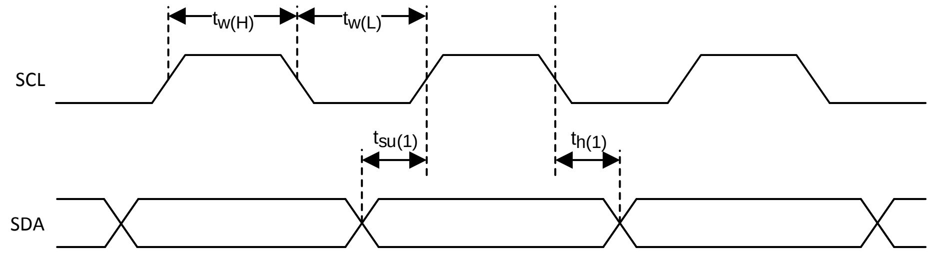


Figure 1. SCL and SDA Timing

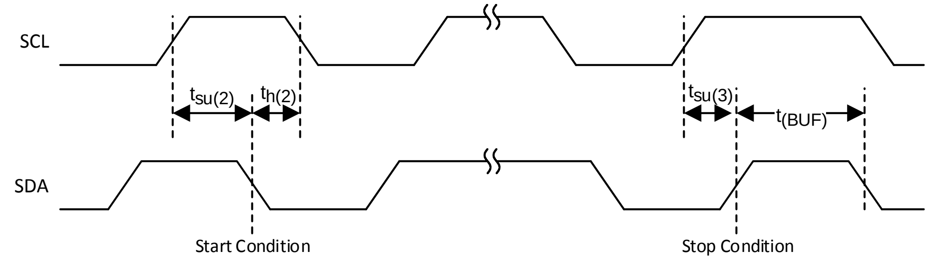


Figure 2. Timing for Start and Stop Conditions

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{on\text{-}sd}$	Turn-on time from shutdown to waveform	EN = Low to High, STBY = Low		229		ms
$t_{OFF\text{-}sd}$	Turn-off time	EN = High to Low		47		µs
$t_{on\text{-}stdby}$	Turn-on time from standby to waveform	EN = High, STBY = High to Low		32		µs

6.8 Typical Characteristics

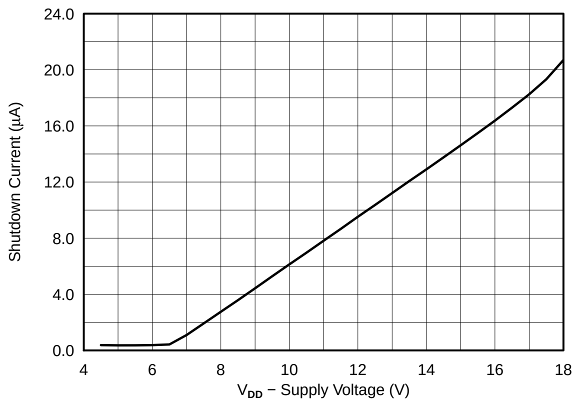


Figure 3. Shutdown Current vs VDD Voltage

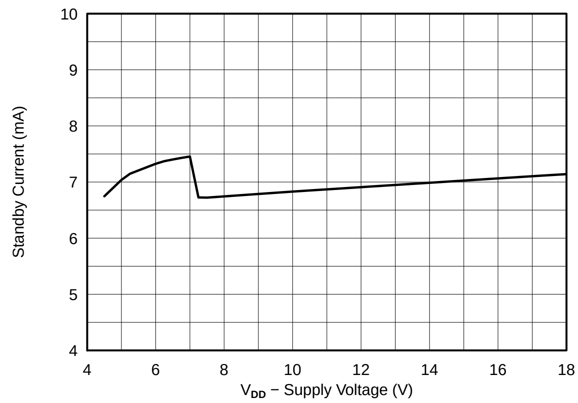


Figure 4. Standby Current vs VDD Voltage

7 Detailed Description

7.1 Overview

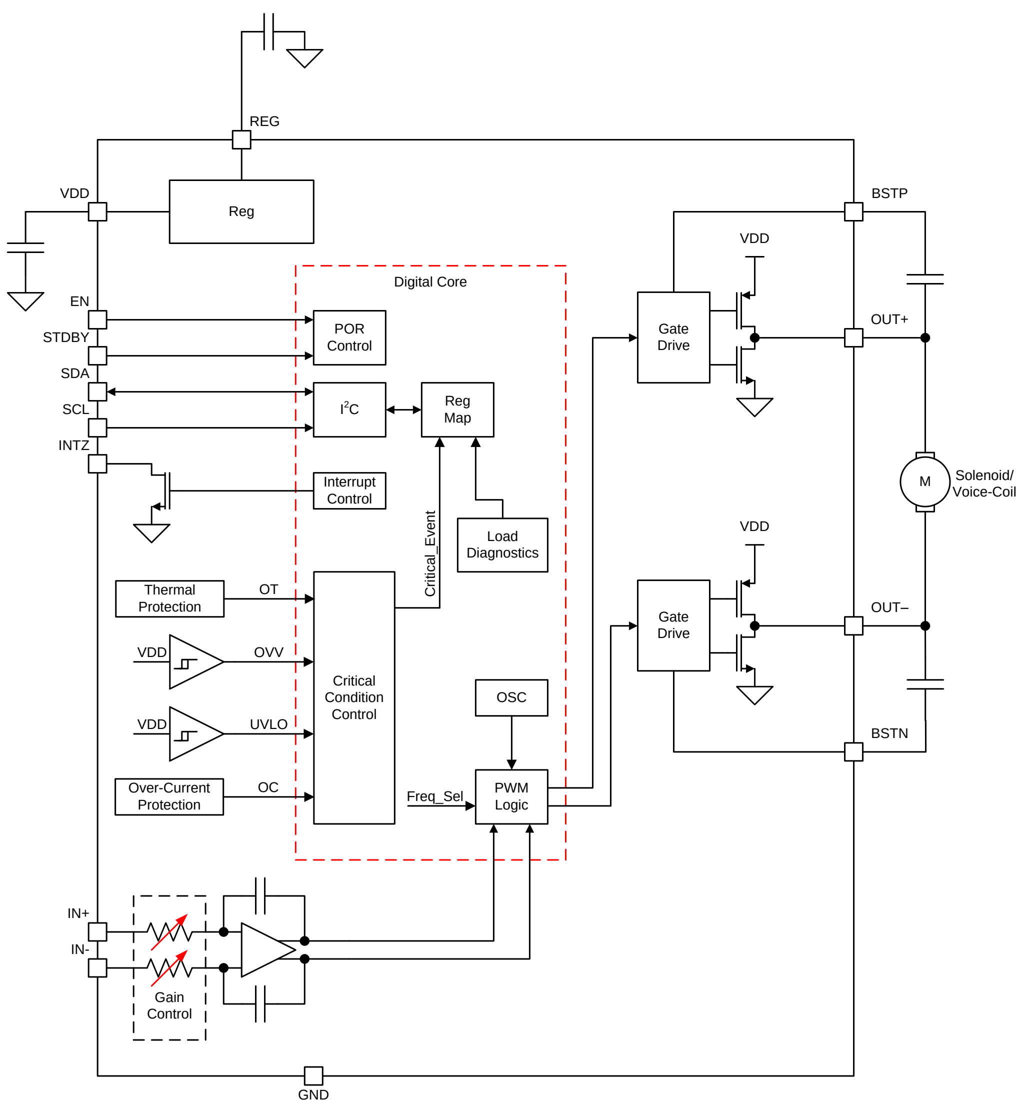
The DRV2510-Q1 device is a high current haptic driver specifically designed for inductive loads, such as solenoids and voice coils.

The output stage consists of a full H-bridge capable of delivering 3 A of peak current.

The design uses an ultra-efficient switching output technology developed by Texas Instruments, but with features added for the automotive industry. The DRV2510-Q1 device provides protection functions such as undervoltage lockout, over-current protection and over-temperature protection. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system.

The DRV2510-Q1 device is automotive qualified. The integrated load-dump protection reduces external voltage clamp cost and size, and the onboard load diagnostics report the status of the actuator through the digital interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input and Configurable Pre-amplifier

The DRV2510-Q1 device features a differential input stage that cancels common-mode noise that appears on the inputs. The DRV2510-Q1 device also features four gain settings that are configurable via I^2C. Please see the Programming Sections for register locations.

Table 1. Gain Configuration Table

GAIN	INPUT IMPEDANCE
20 dB	60 kΩ
26 dB	30 kΩ
32 dB	15 kΩ
36 dB	9 kΩ

7.3.2 Pulse-Width Modulator (PWM)

The DRV2510-Q1 device features BD modulation scheme with high bandwidth, low noise, low distortion, and excellent stability.

The BD modulation scheme allows for smaller ripple currents through the load. Each output switches from 0 V to the supply voltage. With no input, the OUT+ and OUT- pins are in phase with each other so that there is little or no current in the load. For positive differential inputs, the duty cycle of OUT+ is greater than 50% and the duty cycle of OUT- is lower than 50% for a positive differential output voltage. The opposite is true for negative differential inputs. The voltage accross the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces the I^2R losses in the load.

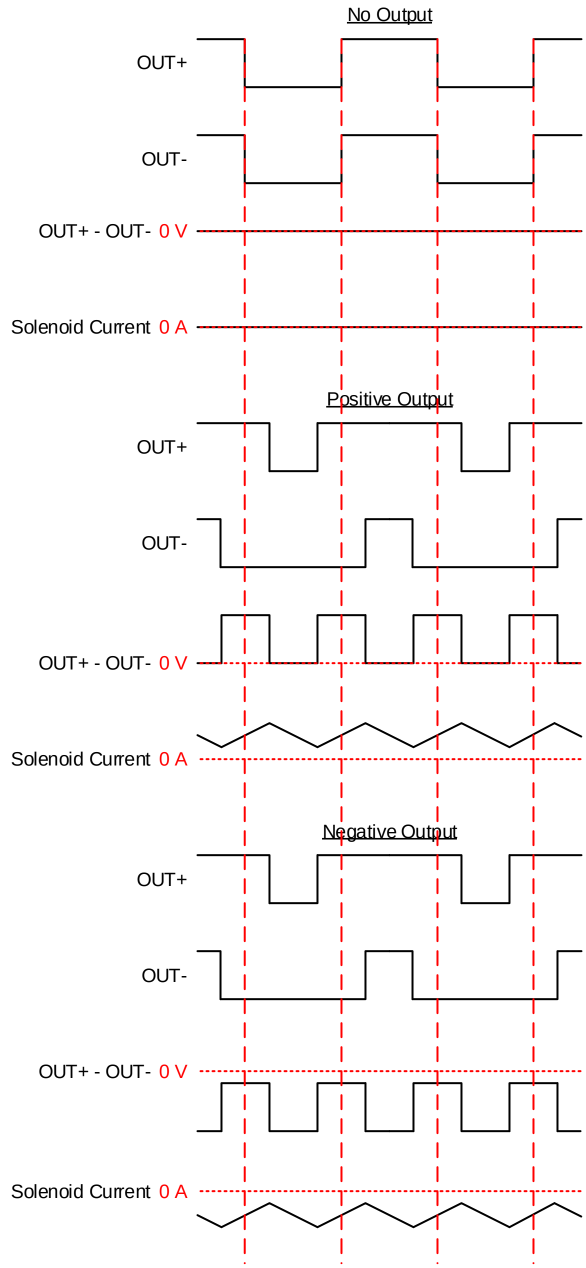


Figure 5. BD Mode Modulation

7.3.3 Designed for low EMI

The DRV2510-Q1 device design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that causes EMI. Follow the recommended design requirements in the *Design Requirements* section.

7.3.4 Device Protection Systems

The DRV2510-Q1 device features a complete set of protection circuits carefully designed to protect the device against permanent failures due to shorts, over-temperature, over-voltage, and under-voltage scenarios. The INTZ pin signals if an error is detected.

Additionally, the DRV2510-Q1 device is not damaged by adjacent pin to pin shorts.

Table 2. Fault Reporting Table

FAULT	TRIGGERING CONDITION	INTZ	ACTION
Over-current	Output short or short to VDD or GND	pulled low	output in high impedance. I^2 updated.
Over-temperature	T_j > 150 ºC	pulled low	output in high impedance. Recovery is automatic once the temperature returns to a safe level.
Under-voltage	VDD < 4 V	pulled low	output in high impedance. I^2 reset.
Over-voltage	VDD > 21 V	pulled low	output in high impedance. I^2 updated.

7.3.4.1 Diagnostics

The device incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to VDD
- Short across load
- Open load

The device reports the presence of any of the short or open conditions to the system via I^2C register read.

1. **Load Diagnostics**—The load diagnostic function runs on de-assertion of EN or when the device is in a fault state (dc detect, overcurrent, overvoltage, undervoltage, and overtemperature). During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to VDD, open load, or shorted load. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning. The load diagnostic test takes approximately 229 ms to run. Note that the *check* phase repeats up to five times if a fault is present or a large capacitor to GND is present on the output. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state, and the device checks the load continuously until removal of the fault condition. After detection of a normal output condition, the output starts. The load diagnostics run after every other overvoltage (OV) event. The load diagnostic for open load only has I^2C reporting. All other faults have I^2C and INTZ pin assertion.

   The device performs load diagnostic tests as shown in Figure 6.
   Figure 7 illustrates how the diagnostics determine the load based on output conditions.

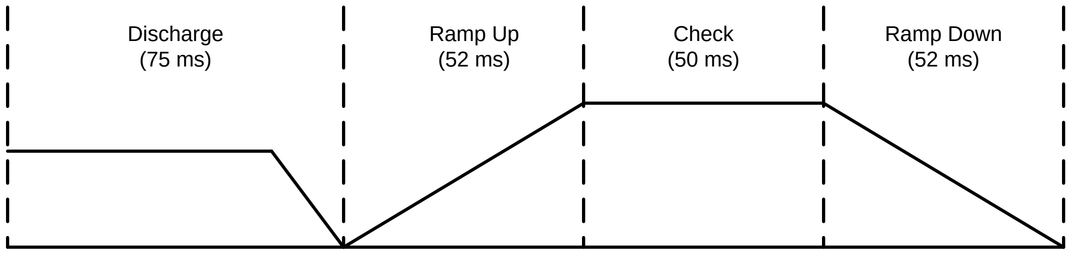


Figure 6. Load Diagnostics Sequence of Events

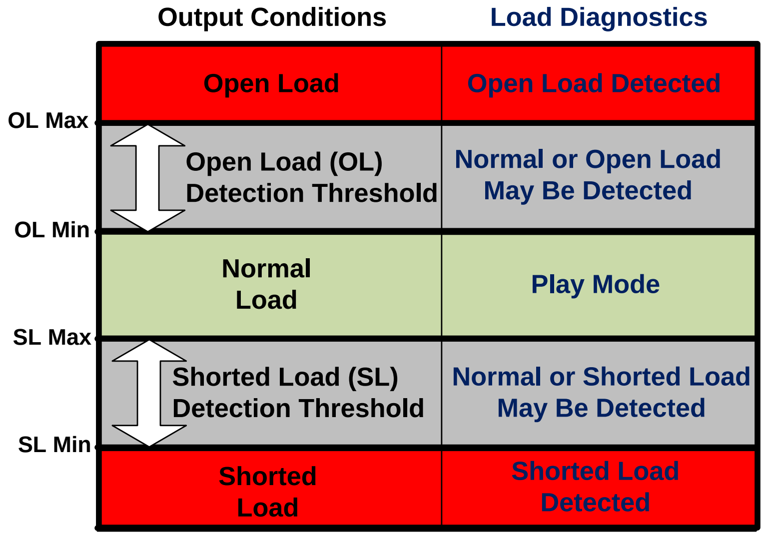


Figure 7. Load Diagnostic Reporting Thresholds

2. **Faults During Load Diagnostics**—If the device detects a fault (overtemperature, overvoltage, undervoltage) during the load diagnostics test, the device exits the load diagnostics, which may result in a small transient on the output.

7.4 Device Functional Modes

The DRV2510-Q1 device has multiple power states to optimize power consumption.

7.4.1 Operation in Shutdown Mode

The NRST pin of the DRV2510-Q1 device puts the device in a shutdown mode. When NRST is asserted (logic low), all internal blocks of the device are off to achieve ultra low power. I^2C is not operational in this mode and the output is in Hi-Z state.

7.4.2 Operation in Standby Mode

The STDBY pin of the DRV2510-Q1 device puts the device in a standby mode. When STDBY is asserted (logic high), some internal blocks of the device are off to achieve low power while preserving the ability to wake up quickly to achieve low latency waveform playback.

7.4.3 Operation in Active Mode

The DRV2510-Q1 device is in active mode when it has a valid supply, and it is not in either shutdown or standby modes. In this mode the DRV2510-Q1 device is fully on and reproducing at the output the input times the gain.

7.5 Programming

7.5.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 8 shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When the acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. Figure 8 shows a generic data-transfer sequence.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Pull-up resistors between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2510-Q1 supply voltage, V_{DD}.

NOTE

The DRV2510-Q1 slave address is 0x6C (7-bit), or 1101100 in binary.

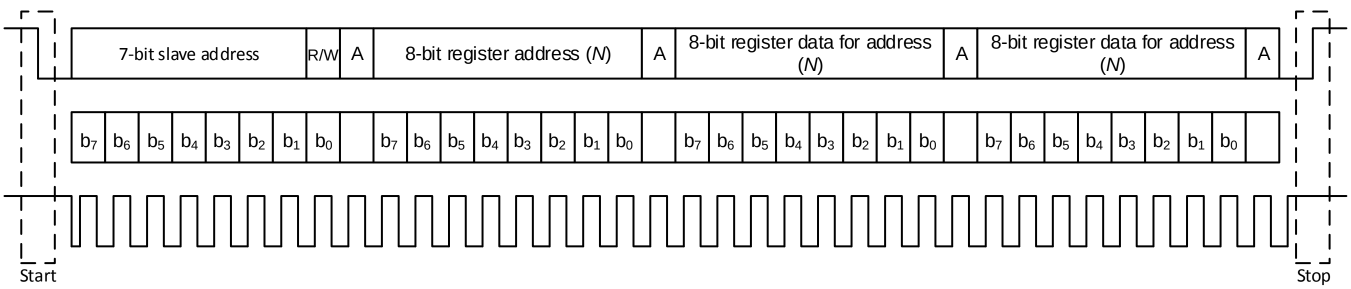


Figure 8. Typical I²C Sequence

The DRV2510-Q1 device operates as an I²C-slave 1.8-V logic thresholds, but can operate up to the V_{DD} voltage. The device address is 0x5A (7-bit), or 1011010 in binary which is equivalent to 0xB4 (8-bit) for writing and 0xB5 (8-bit) for reading.

7.5.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte R/W operations for all registers.

During multiple-byte read operations, the DRV2510-Q1 device responds with data one byte at a time and begins at the signed register. The device responds as long as the master device continues to respond with acknowledges.

The DRV2510-Q1 supports sequential I²C addressing. For write transactions, a sequential I²C write transaction has taken place if a register is issued followed by data for that register as well as the remaining registers that follow. For I²C sequential-write transactions, the register issued then serves as the starting point and the amount of data transmitted subsequently before a stop or start is transmitted determines how many registers are written.

Programming (continued)

7.5.3 Single-Byte Write

As shown in Figure 9, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read-write bit. The read-write bit determines the direction of the data transfer. For a write-data transfer, the read-write bit must be set to 0. After receiving the correct I^2C device address and the read-write bit, the DRV2510-Q1 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the DRV2510-Q1 internal-memory address that is accessed. After receiving the register byte, the device responds again with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

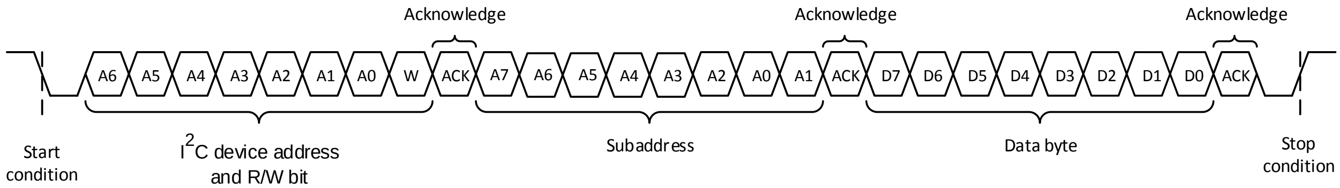


Figure 9. Single-Byte Write Transfer

7.5.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2510-Q1 device as shown in Figure 10. After receiving each data byte, the DRV2510-Q1 device responds with an acknowledge bit.

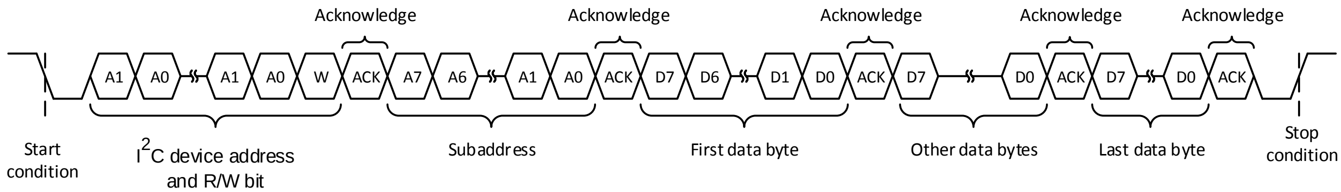


Figure 10. Multiple-Byte Write Transfer

7.5.5 Single-Byte Read

Figure 11 shows that a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read-write bit. For the data-read transfer, both a write followed by a read actually occur. Initially, a write occurs to transfer the address byte of the internal memory address to be read. As a result, the read-write bit is set to 0.

After receiving the DRV2510-Q1 address and the read-write bit, the DRV2510-Q1 device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the DRV2510-Q1 address and the read-write bit again. On this occasion, the read-write bit is set to 1, indicating a read transfer. Next, the DRV2510-Q1 device transmits the data byte from the memory address that is read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer. See the note in the *General I^2C Operation* section.

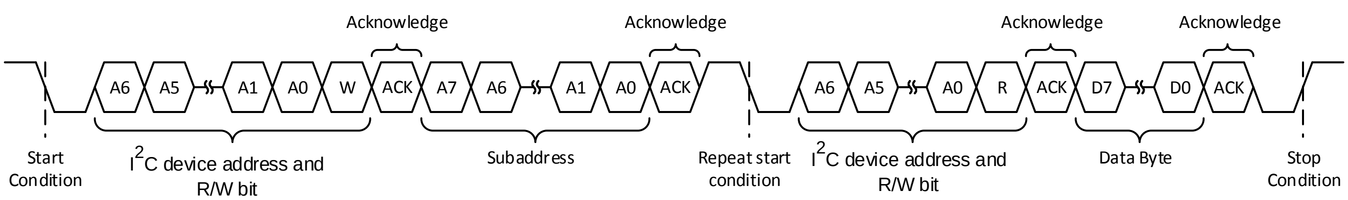


Figure 11. Single-Byte Read Transfer

Programming (continued)

7.5.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2510-Q1 device to the master device as shown in Figure 12. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

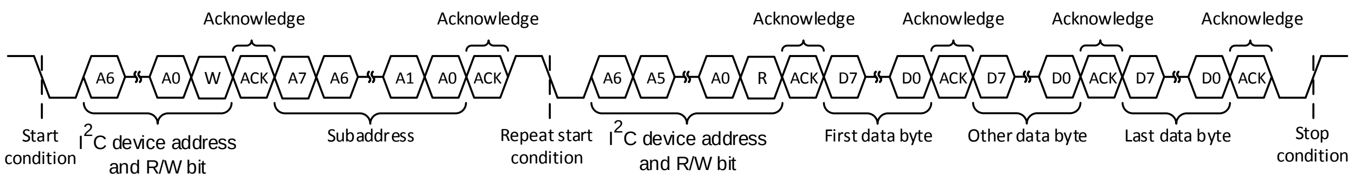


Figure 12. Multiple-Byte Read Transfer

7.6 Register Map

Table 3. Register Map Overview

REG NO.	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	0x00	Reserved					LOAD_DIAG	Reserved	
0x01	0x00	OVER_TEMP	Reserved	OVER_VOLT	UNDER_VOLT	OVER_CURR	Reserved		
0x02	0x00	DEV_ACTIVE	STDBY	DIAG_ACTIVE	FAULT	LOAD_SHORT	LOAD_OPEN	LOAD_SHORT_GND	LOAD_SHORT_VDD
0x03	0x00	GAIN[1:0]		Reserved					FREQ_SEL

7.6.1 Address: 0x00

Figure 13. 0x00

7	6	5	4	3	2	1	0
Reserved					LOAD_DIAG[0]	Reserved	
					RO-0		

Table 4. Address: 0x00

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7-3	Reserved				
2	LOAD_DIAG	RO	0	Shows the status of the load diagnostics.	
				0	An open or short has not been detected.
				1	An open or short was detected.
1-0	Reserved				

7.6.2 Address: 0x01

Figure 14. 0x01

7	6	5	4	3	2	1	0
OVER_TEMP[0]	Reserved	OVER_VOLT[0]	UNDER_VOLT[0]	OVER_CURR[0]	Reserved		
RO-0		RO-0	RO-0	RO-0			

Table 5. Address: 0x01

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7	OVER_TEMP	RO	0	Shows the current statuts of the thermal protection	
				0	Temperature is below the over-temperature threshold.
				1	Temperature is above the over-temperature threshold.
6	Reserved				
5	OVER_VOLT	RO	0	Shows the status of the over-voltage protection.	
				0	VDD voltage is below the over-voltage threshold.
				1	VDD voltage is above the over-voltage threshold.
4	UNDER_VOLT	RO	0	Shows the status of the under-voltage protection.	
				0	VDD voltage is above the under-voltage threshold.
				1	VDD voltage is below the under-voltage threshold.
3	OVER_CURR	RO	0	Shows the status of the over-current protection.	
				0	An over-current event has not occured.
				1	Device shutdown due to over-current.
2-0	Reserved				

7.6.3 Address: 0x02

Figure 15. 0x02

7	6	5	4	3	2	1	0
DEV_ACTIVE [0]	STDBY[0]	DIAG_ACTIVE [0]	FAULT[0]	LOAD_SHORT [0]	LOAD_OPEN [0]	LOAD_SHORT _GND[0]	LOAD_SHORT _VDD[0]
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0

Table 6. Address: 0x02

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7	DEV_ACTIVE	RO	0	Shows the device status (active or shutdown).	
				0	Device is shutdown.
				1	Device is active.
6	STDBY	RO	0	Shows the device standby status.	
				0	Device is not on standby.
				1	Device is on standby.
5	DIAG_ACTIVE	RO	0	Shows the status of the diagnositcs engine.	
				0	Not performing load diagnostics.
				1	Performing load diagnostics.
4	FAULT	RO	0	Shows if a fault has occured on the system. Either over-voltage, under-voltage, over-current, over-temperature.	
				0	No fault has occured.
				1	A fault has occured.
3	LOAD_SHORT	RO	0	Shows whether the output is shorted.	
				0	OUT+ is not shorted to OUT-.
				1	OUT+ is shorted to OUT-.
2	LOAD_OPEN	RO	0	Shows whether the output has a proper load connected.	
				0	A proper load is connected between OUT+ and OUT-.
				1	There is an open connection between OUT+ and OUT-.
1	LOAD_SHORT_GND	RO	0	Shows whether the output is shorted to GND.	
				0	Output is not shorted to GND.
				1	Either OUT+ or OUT- is shorted to GND.
0	LOAD_SHORT_VDD	RO	0	Shows whether the output is shorted to VDD.	
				0	Output is not shorted to VDD.
				1	Either OUT+ or OUT- is shorted to VDD.

7.6.4 Address: 0x03

Figure 16. 0x03

7	6	5	4	3	2	1	0
GAIN[1:0]		Reserved					FREQ_SEL[0]
R/W-0	R/W-0						R/W-0

Table 7. Address: 0x03

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7-6	GAIN[1:0]	R/W	0	Sets the gain of the driver.	
				0	20 dB.
				1	26 dB.
				2	32 dB.
				3	36 dB.
5-1	Reserved				
0	FREQ_SEL	R/W	0	Sets the output frequency.	
				0	400 kHz.
				1	500 kHz.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV2510-Q1 device is a high-efficiency driver for inductive loads, such as solenoids and voice-coils. The typical use of the device is on haptic applications where short, strong waveforms are desired to create a haptic event that will be coming from the application processor.

8.2 Typical Applications

8.2.1 Single-Ended Source

To use the DRV2510-Q1 with a single-ended source, apply either a voltage divider to bias INB to 3 V, tie to GND or use a 0.1-µF cap from INB to GND to have the device self bias. Apply the single-ended signal to the INA pin.

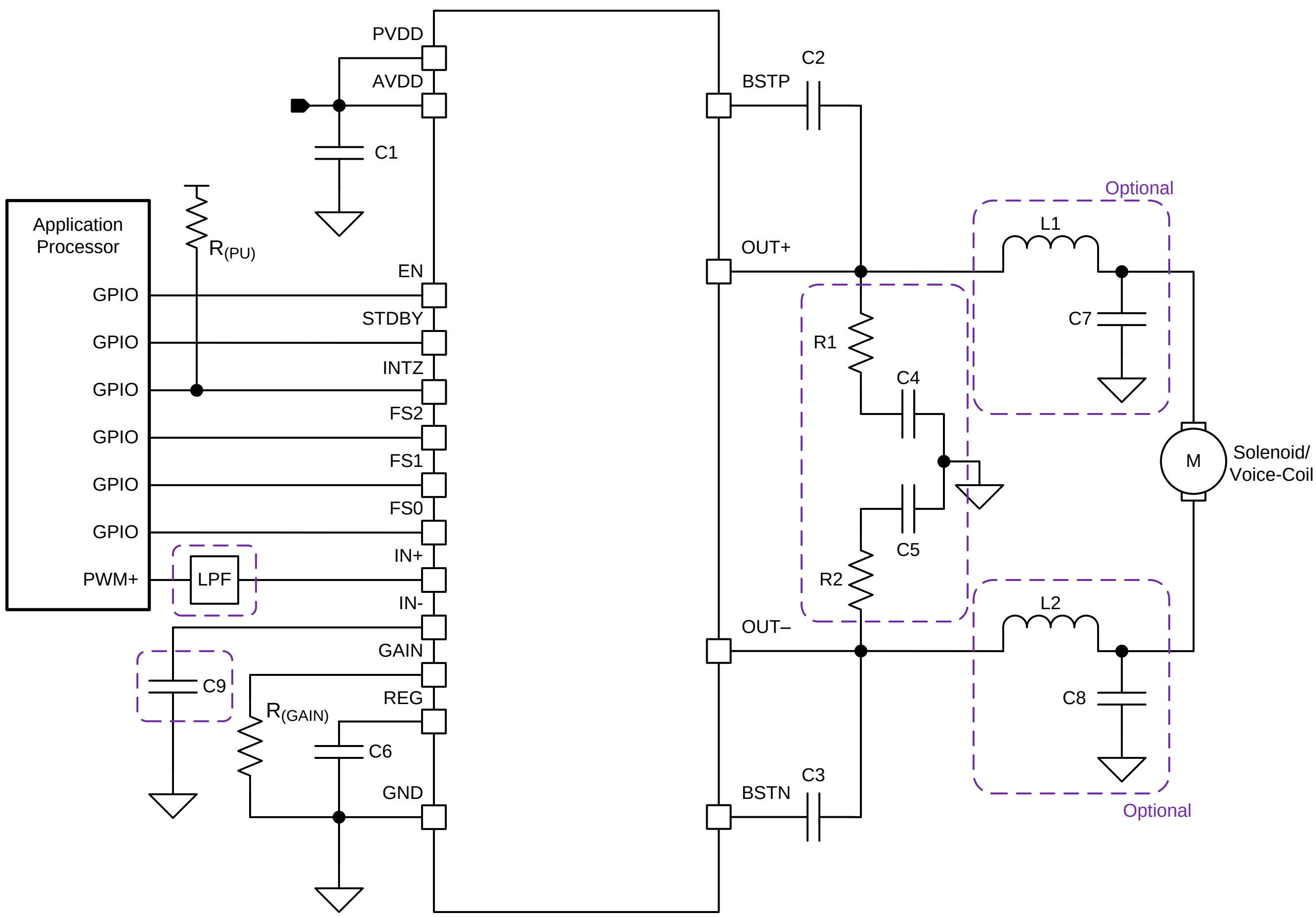


Figure 17. Typical Application Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

For most applications the following component values found in Table 8 below can be used.

Table 8. Component Requirements Table

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
C1	Supply capacitor	Capacitance	22 µF, 10 µF, and 0.1 µF
C2/C3	Boost capacitor	Capacitance	0.22 µF
C4/C5	Output snubber capacitor	Capacitance	470 pF
C6	Regulator capacitor	Capacitance	1 µF
C9	Input decoupling capacitor	Capacitance	0.1 µF
R1/R2	Output snubber resistor	Resistance	3.3 Ω
$R_{(PU)}$	Pull-up resistor	Resistance	100 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Optional Components

Note that in the diagrams, there are a few optional external components. These optional external components may be needed in the application to meet EMI/EMC standards and specifications by filters necessary frequency spectrums.

8.2.1.2.2 Capacitor Selection

A bulk bypass capacitor should be mounted between VBAT and GND. The capacitance needs to be >22 uF with a X5R or better rating on the power pins to GND. Also include two ceramic capacitors in the ranges of 220 pF to 1 uF and 100 nF to 1 uF. The bootstrap capacitors, BSTA and BSTB, should be 220-nF ceramic capacitors of quality X5R or better rated for at least the maximum rating of the pin.

8.2.1.2.3 Solenoid Selection

The DRV2510-Q1 solenoid driver can accommodate a variety of solenoids. Solenoids should have an equivalent resistance of 1.6 Ω or greater. Solenoids with lower resistances are prone to driving high currents. A maximum peak current of 3-A should not be exceeded.

8.2.1.2.4 Output Filter Considerations

The output filter is optional and is mainly for limiting peak currents. A second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See Equation 2, Equation 3, and Equation 4 for example filter design.

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \quad (1)$$

$$L_x = \frac{\sqrt{2} \times R_L}{2\omega_o} \quad (2)$$

$$2 \times C_F = \frac{\sqrt{2}}{2 \times \frac{R_L}{2} \times \omega_0} \quad (3)$$

$$\omega_0 = 2\pi \times f \quad (4)$$

8.2.1.3 Application Curves

These application curves were taken using an HA200 solenoid with a 100-g mass, and the acceleration was measured using the DRV-AAC16-EVM accelerometer. The following scales apply to the graphs:

- Output Differential Voltage scale is shown on the plots at 5-V/div
- Acceleration scale is 5.85-G/div
- Current scale is 2-A/div

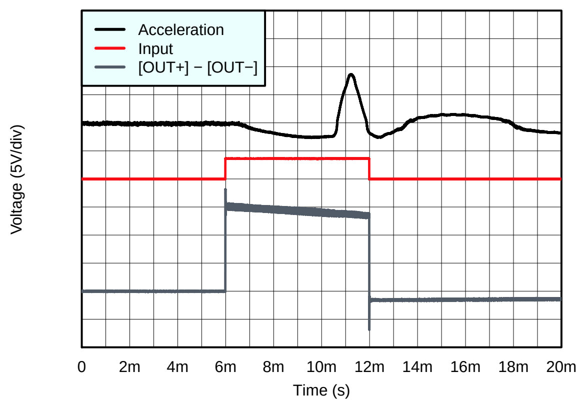


Figure 18. Voltage and Acceleration vs Time (Input Square Wave)

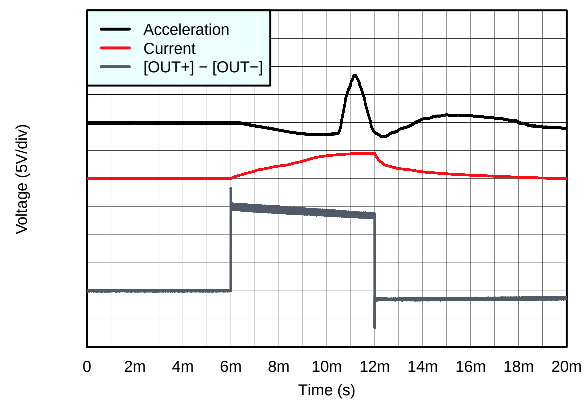


Figure 19. Voltage and Acceleration vs Time (Square Wave)

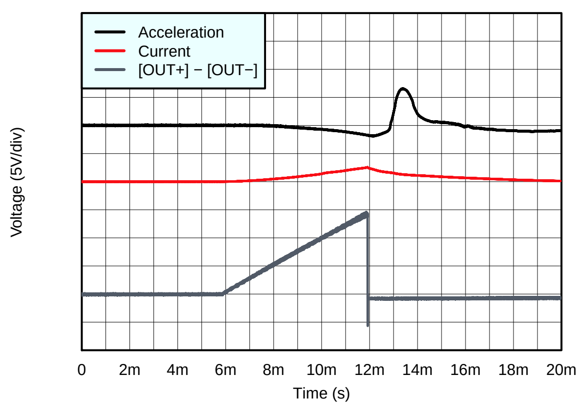


Figure 20. Voltage and Acceleration vs Time (Ramp Wave)

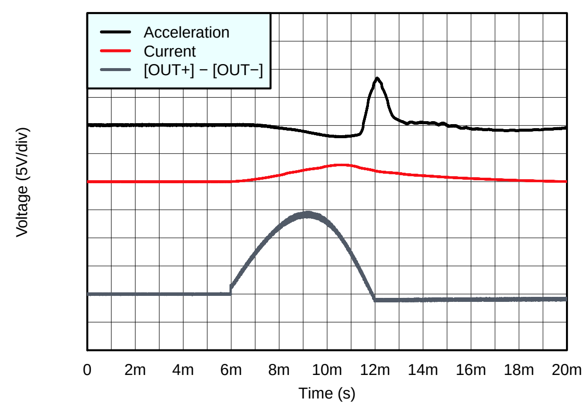


Figure 21. Voltage and Acceleration vs Time (1/2 Sine Wave)

8.2.1.4 Differential Input Diagram

To use the DRV2510-Q1 with a differential input source, apply both inputs differentially from a control source (GPIO, DAC, etc...).

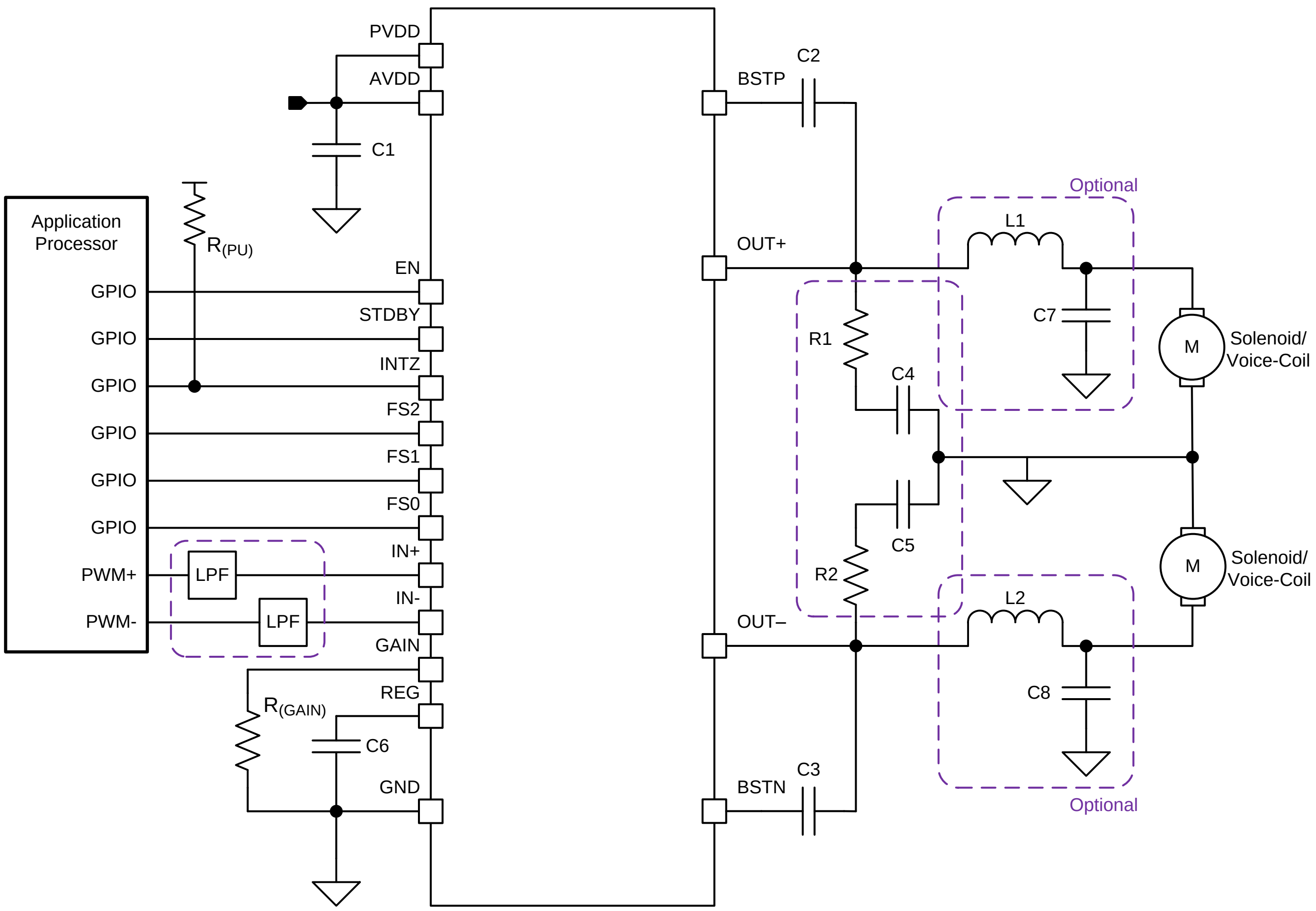


Figure 22. Typical Application Schematic

9 Power Supply Recommendations

The DRV2510-Q1 device operates from 4.5 V - 18 V and this supply should be able to handle high surge currents in order to meet the high currrent draws for haptics effects. Additionally the DRV2510-Q1 should have 22-µF, 10-µF and 0.1-µF ceramic capacitors near the VDD pin for additional decoupling from trace routing.

10 Layout

10.1 Layout Guidelines

The EVM layout optimizes for thermal dissipation and EMC performance. The DRV2510-Q1 device has a thermal pad down, and good thermal conduction and dissipation require adequate copper area. Layout also affects EMC performance. It is best practice to use the same/similiar layout as shown below in the DRV2510Q1EVM.

10.2 Layout Example

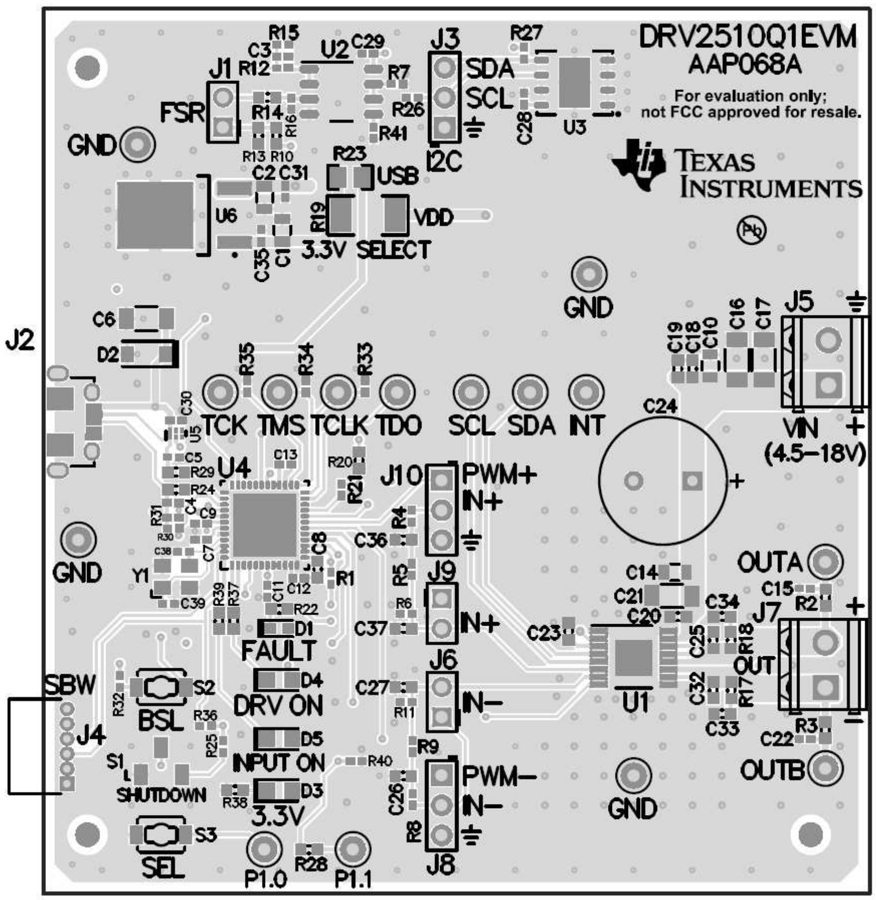


Figure 23. DRV2510-Q1 EVM

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

E2E is a trademark of Texas Instruments.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV2510QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV2510	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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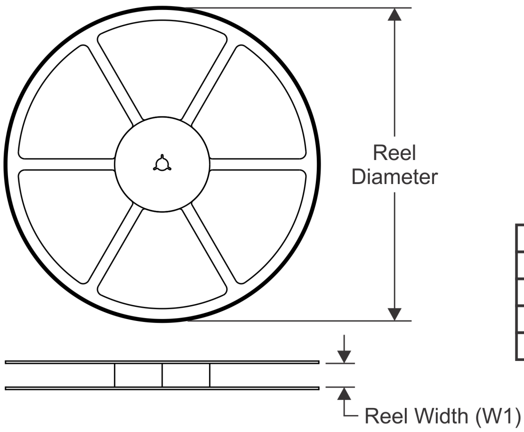
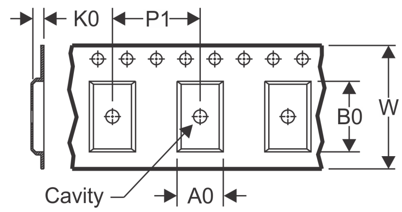
TAPE AND REEL INFORMATION

REEL DIMENSIONS

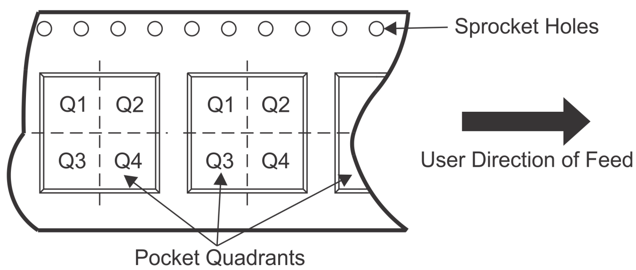


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

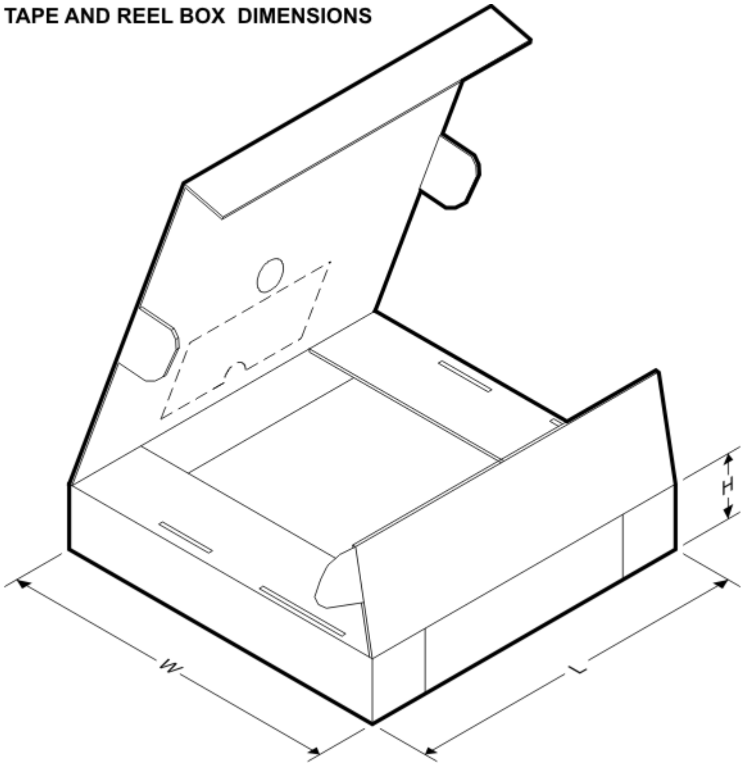
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2510QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

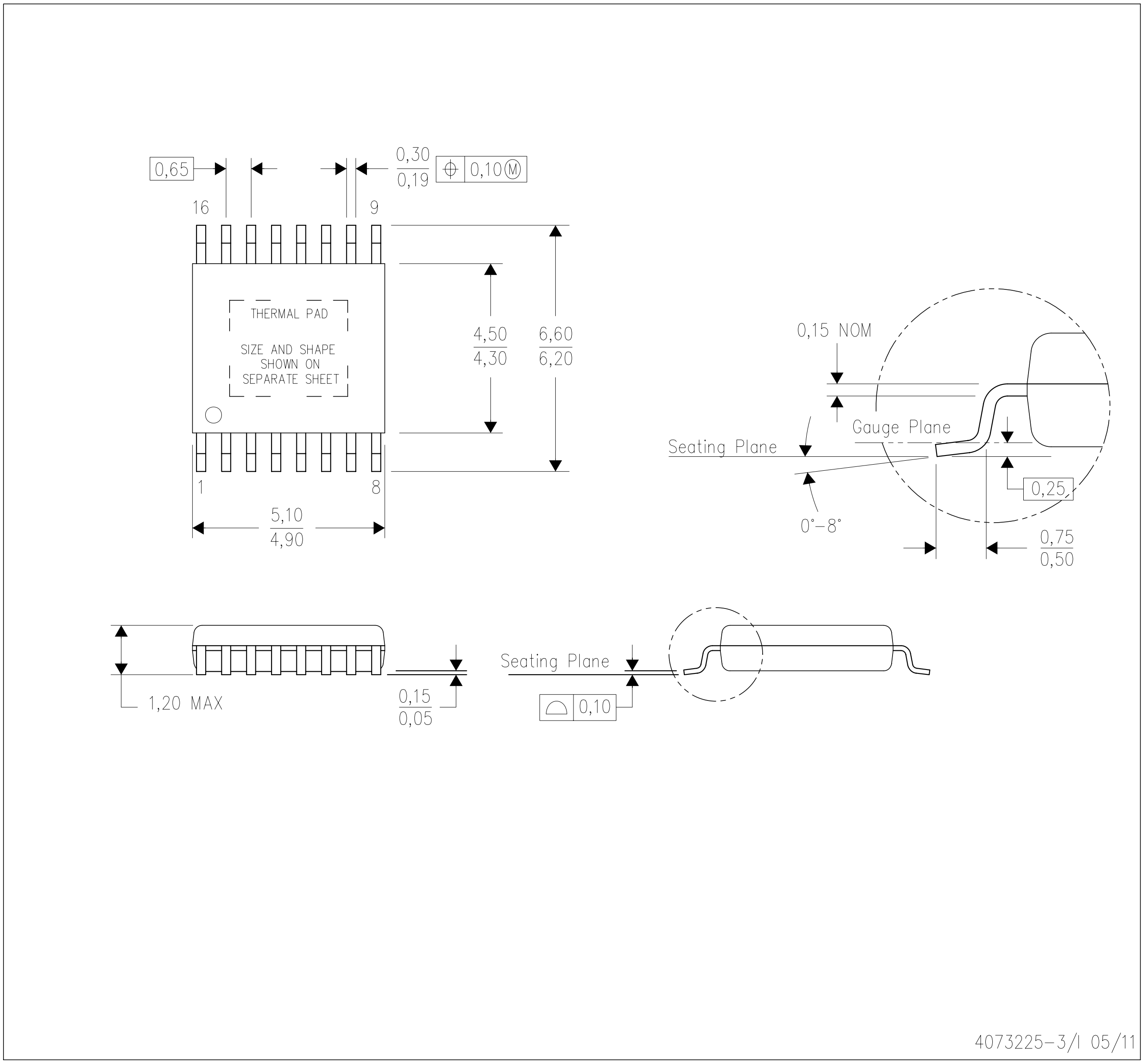
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2510QPWPRQ1	HTSSOP	PWP	16	2000	367.0	367.0	38.0

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

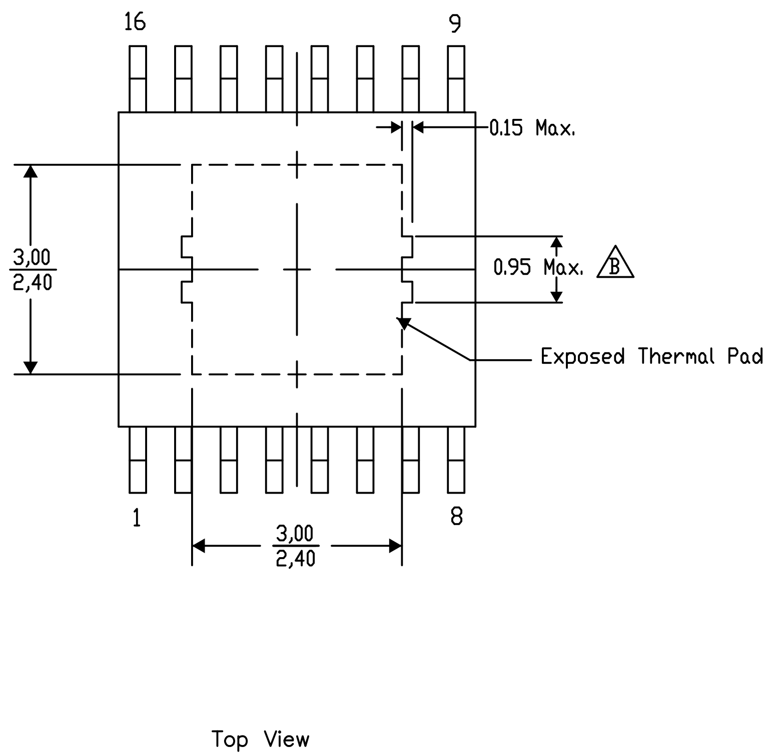
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

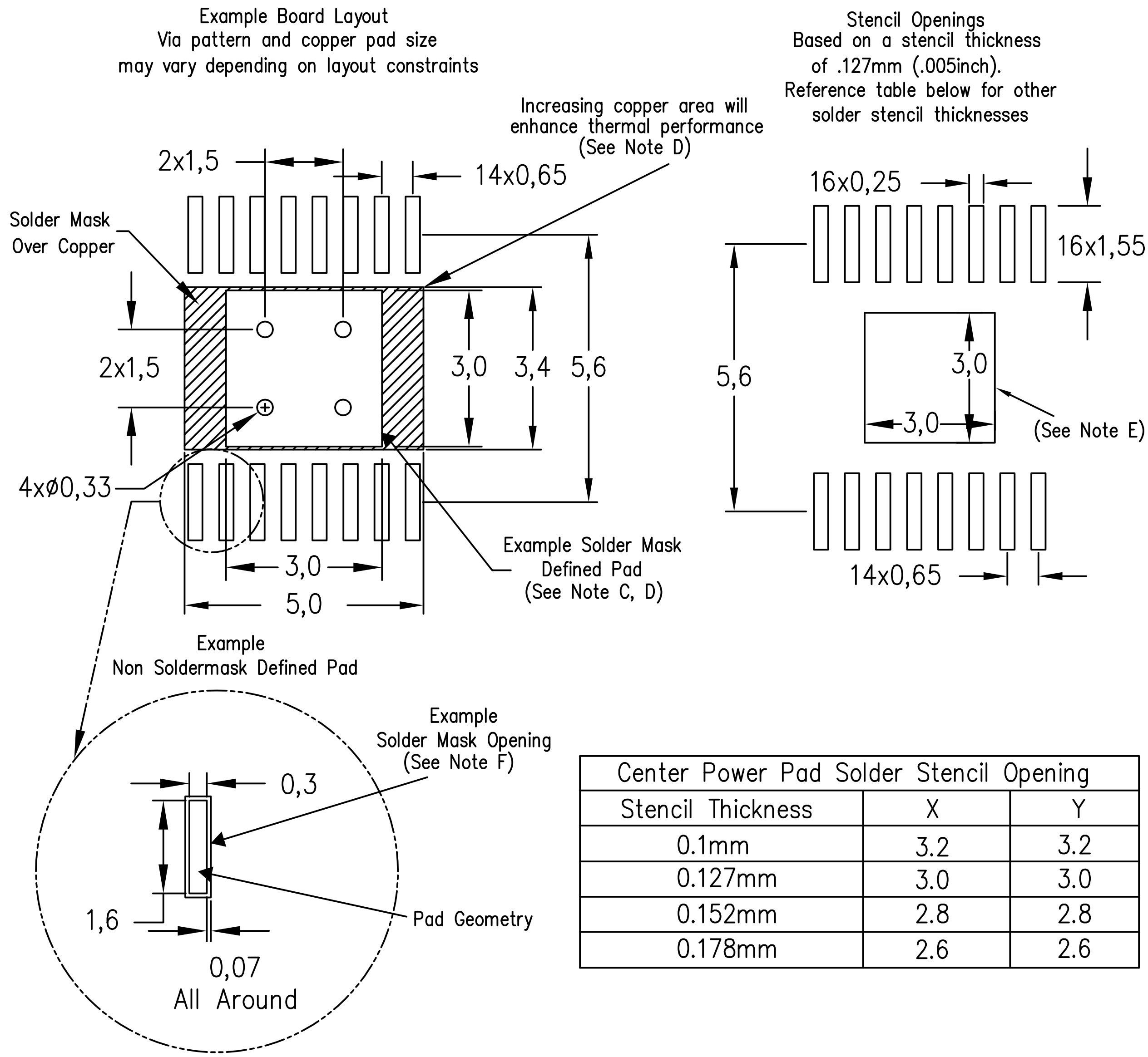
4206332-8/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	3.2
0.127mm	3.0	3.0
0.152mm	2.8	2.8
0.178mm	2.6	2.6

4207609-5/W 09/15

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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