TPS22918-Q1, 5.5-V, 2-A, 52-mΩ On-Resistance Load Switch

1 Features

- AEC-Q100 Qualified
- Integrated Single-Channel Load Switch
- Qualified for Automotive Applications:
  - Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature Range
- Input Voltage Range: 1 V to 5.5 V
- Low On-Resistance (R_{ON})
  - R_{ON} = 52 mΩ (typical) at V_{IN} = 5 V
  - R_{ON} = 53 mΩ (typical) at V_{IN} = 3.3 V
- 2-A Maximum Continuous Switch Current
- Low Quiescent Current
  - 8.3 µA (typical) at V_{IN} = 3.3 V
- Low-Control Input-Threshold Enables Use of 1 V or Higher GPIO
- Configurable Quick-Output Discharge (QOD)
- Configurable Rise Time With CT Pin
- Small SOT23-6 Package (DBV)
  - 2.9 mm × 2.8 mm, 0.95-mm Pitch, 1.45-mm Height (with leads)
- ESD Performance Tested per AEC Q100
  - ±2-kV HBM and ±750-V CDM

2 Applications

- Automotive Electronics
- Infotainment
- Cluster
- ADAS (Advanced Driver Assistance Systems)

3 Description

The TPS22918-Q1 is a single-channel load switch with both configurable rise time and configurable quick-output discharge. The device contains an N-channel MOSFET that can operate over an input voltage range of 1 V to 5.5 V and can support a maximum continuous current of 2 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

The configurable rise time of the device reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The TPS22918-Q1 features a configurable quick output discharge (QOD) pin, which controls the fall time of the device to allow design flexibility for power down and sequencing.

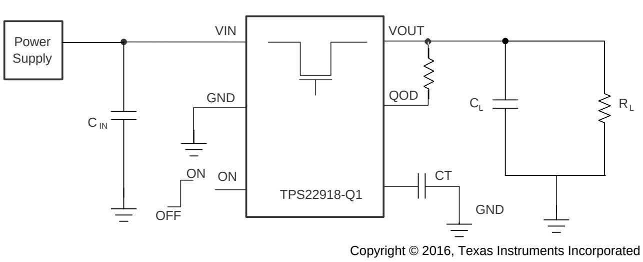
The TPS22918-Q1 is available in a small, leaded SOT-23 package (DBV) which allows to visually inspect solder joints. The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Device Information(1)

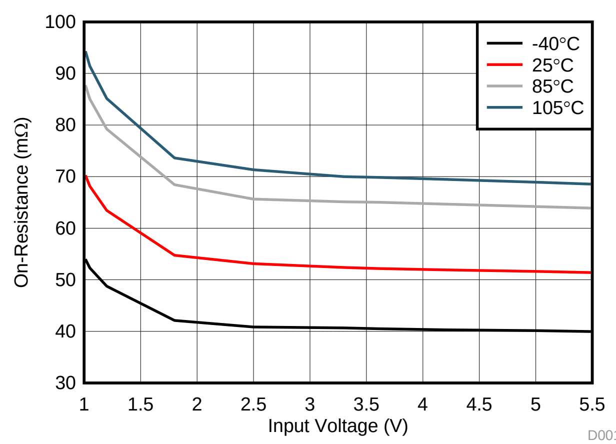
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22918-Q1	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



On-Resistance vs Input Voltage Typical Values



I_{OUT} = –200 mA

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (July 2016) to Revision A	Page
• Changed device status from *Product Preview* to *Production Data*	1

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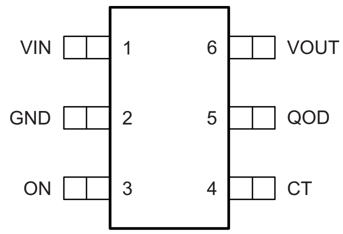
5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information
2	GND	—	Device ground
3	ON	I	Active high switch control input. Do not leave floating
4	CT	O	Switch slew rate control. Can be left floating. See the *Feature Description* section for more information
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin disconnected See the *Quick Output Discharge (QOD)* section for more information
6	VOUT	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current, T_A = 70°C (3)		2	A
I_{MAX}	Maximum continuous switch current, T_A = 85°C (3)		1.5	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		2.5	A
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Assumes 12-K power-on hours at 100% duty cycle. This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI's semiconductor products.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		1	5.5	V
V_{ON}	ON voltage		0	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{IN} = 1 V to 5.5 V	1	5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{IN} = 1 V to 5.5 V	0	0.5	V
T_A	Operating free-air temperature (1)		–40	105	°C
C_{IN}	Input Capacitor		1 (2)		µF

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(MAX)}$], the maximum power dissipation of the device in the application [$P_{D(MAX)}$], and the junction-to-ambient thermal resistance of the part-package in the application (θ_{JA}), as given by the following equation: $T_{A(MAX)} = T_{J(MAX)} – (\theta_{JA} \times P_{D(MAX)})$.
(2) See the *Application and Implementation* section.

6.4 Thermal Information

THERMAL METRIC (1)		TPS22918-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the following operating ambient temperature –40°C ≤ T_A ≤ +105°C (full). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$	Quiescent current	V_{ON} = 5 V, I_{OUT} = 0 A	V_{IN} = 5.5 V	–40°C to +105°C		9.2	16	µA
			V_{IN} = 5 V			8.7	16	
			V_{IN} = 3.3 V			8.3	15	
			V_{IN} = 1.8 V			10.2	17	
			V_{IN} = 1.2 V			9.3	16	
			V_{IN} = 1 V			8.9	15	
$I_{SD, VIN}$	Shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 5.5 V	–40°C to +105°C		0.5	5	µA
			V_{IN} = 5 V	–40°C to +105°C		0.5	4.5	
			V_{IN} = 3.3 V	–40°C to +105°C		0.5	3.5	
			V_{IN} = 1.8 V	–40°C to +105°C		0.5	2.5	
			V_{IN} = 1.2 V	–40°C to +105°C		0.4	2	
			V_{IN} = 1 V	–40°C to +105°C		0.4	2	
I_{ON}	ON pin input leakage current	V_{IN} = 5.5 V, I_{OUT} = 0 A		–40°C to +105°C			0.1	µA
R_{ON}	On-Resistance	V_{IN} = 5.5 V, I_{OUT} = –200 mA		25°C		51	59	mΩ
				–40°C to +105°C			78	
		V_{IN} = 5 V, I_{OUT} = –200 mA		25°C		52	59	
				–40°C to +105°C			79	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA		25°C		52	59	
				–40°C to +105°C			79	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA		25°C		53	59	
				–40°C to +105°C			80	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA		25°C		53	61	
				–40°C to +105°C			80	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA		25°C		55	65	
				–40°C to +105°C			88	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA		25°C		64	77	
				–40°C to +105°C			104	
		V_{IN} = 1 V, I_{OUT} = –200 mA		25°C		71	85	
				–40°C to +105°C			116	
V_{HYS}	ON pin hysteresis	V_{IN} = 1 V to 5.5 V		–40°C to +105°C		107		mV
R_{PD}	Output pull down resistance	V_{IN} = 5 V, V_{ON} = 0 V		25°C		24		Ω
				–40°C to +105°C			30	
		V_{IN} = 3.3 V, V_{ON} = 0 V		25°C		25		
				–40°C to +105°C			35	
		V_{IN} = 1.8 V, V_{ON} = 0 V		25°C		45		
				–40°C to +105°C			60	

6.6 Switching Characteristics

See timing test circuit in Figure 21 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the ON pin is asserted high. Test Conditions: V_{ON} = 5 V, T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = 5 V						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		1950		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2540		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		690		µs
V_{IN} = 3.3 V						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		1430		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		1680		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		590		µs
V_{IN} = 1.8 V						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		965		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		960		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		480		µs
V_{IN} = 1 V						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		725		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		3		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		560		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF, CT = 1000 pF		430		µs

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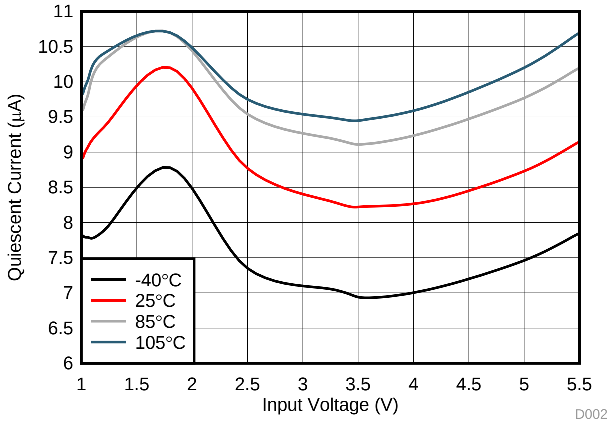
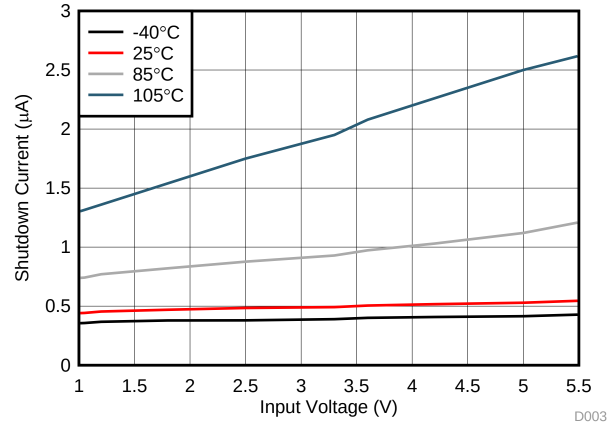
6.7 Typical DC Characteristics



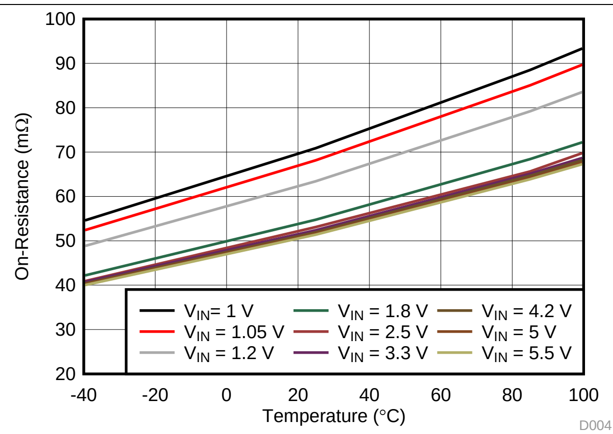
V_{ON} = 5 V I_{OUT} = 0 A

Figure 1. Quiescent Current vs Input Voltage



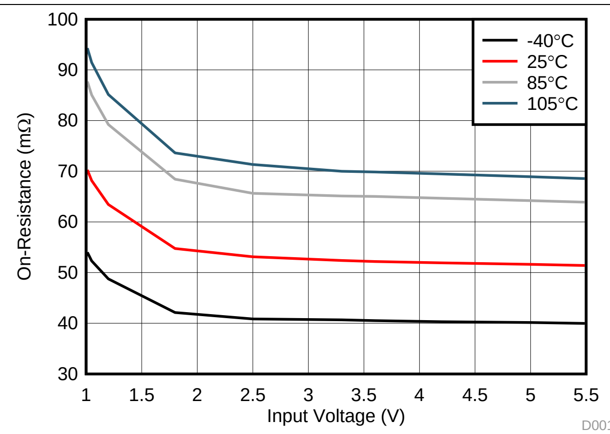
V_{ON} = 0 V I_{OUT} = 0 A

Figure 2. Shutdown Current vs Input Voltage



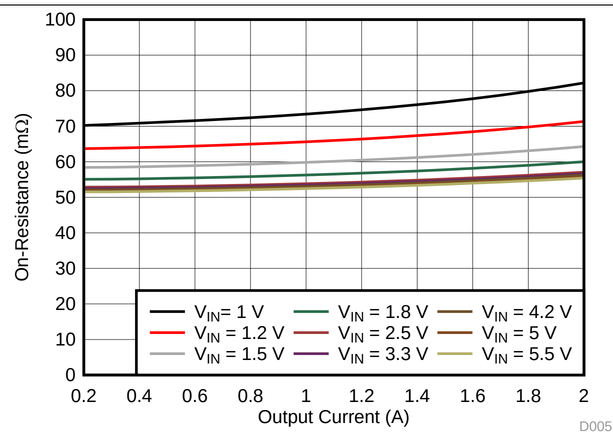
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 3. On-Resistance vs Temperature



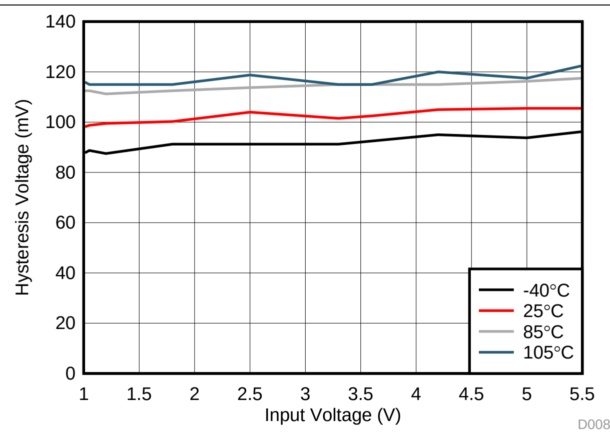
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 4. On-Resistance vs Input Voltage



V_{ON} = 5 V T_A = 25°C

Figure 5. On-Resistance vs Output Current



I_{OUT} = 0 A

Figure 6. Hysteresis Voltage vs Input Voltage

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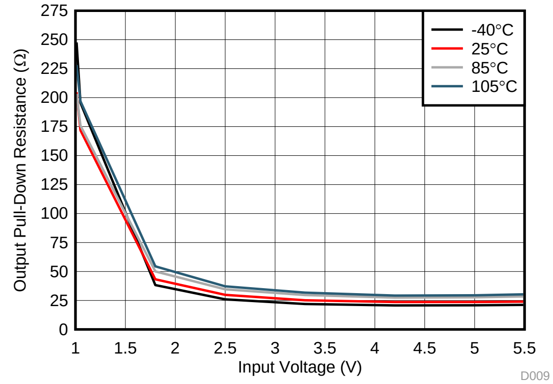
Typical DC Characteristics (continued)



$V_{IN} = V_{OUT}$ $V_{ON} = 0$ V

Figure 7. Output Pull-Down Resistance vs Input Voltage

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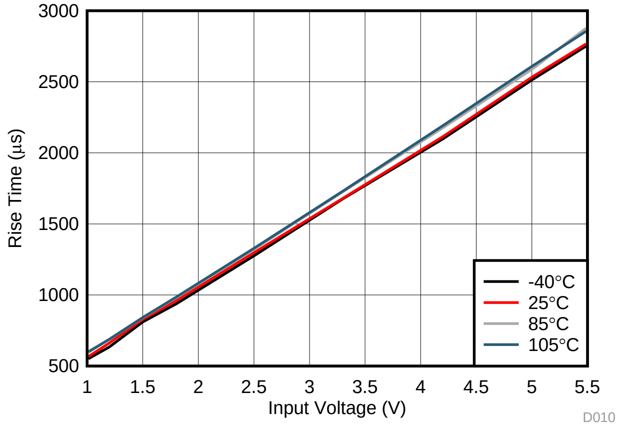
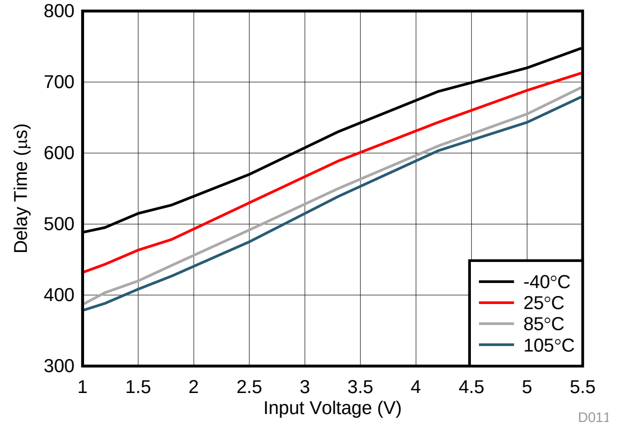
6.8 Typical AC Characteristics



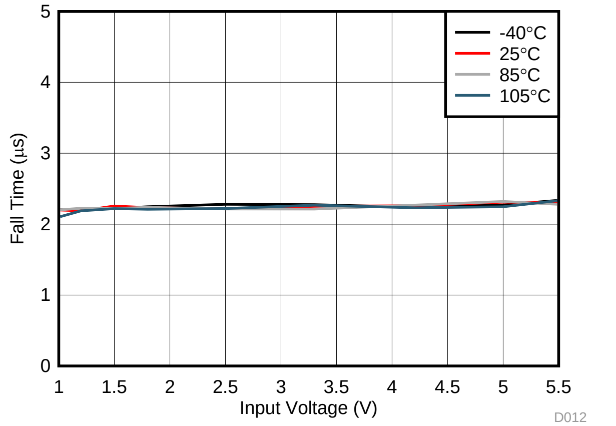
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 1000 pF

Figure 8. Rise Time vs Input Voltage



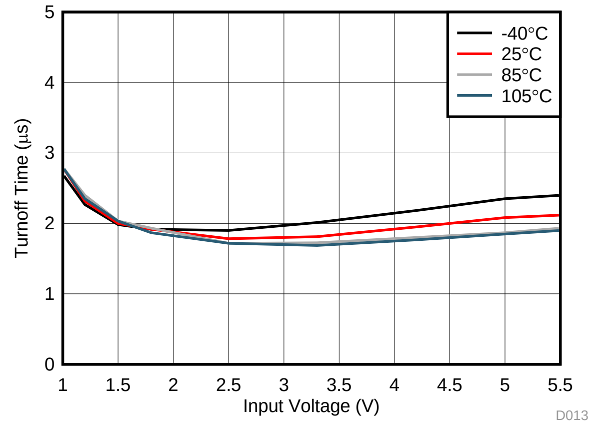
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 9. Delay Time vs Input Voltage



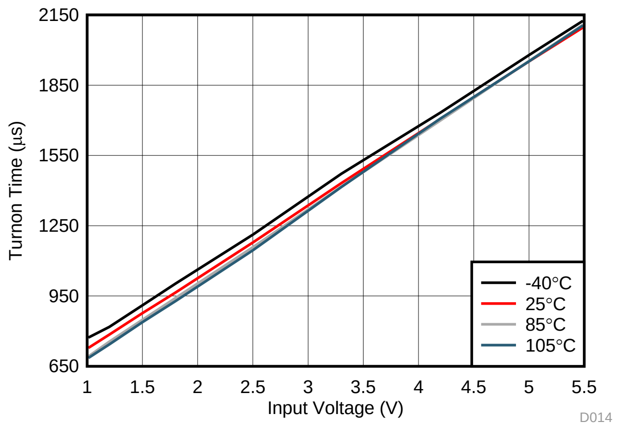
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF QOD = Open

Figure 10. Fall Time vs Input Voltage



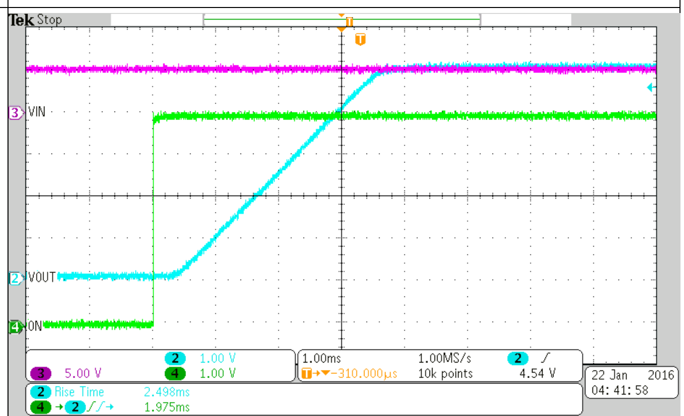
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 11. Turnoff Time vs Input Voltage



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF CT =1000 pF

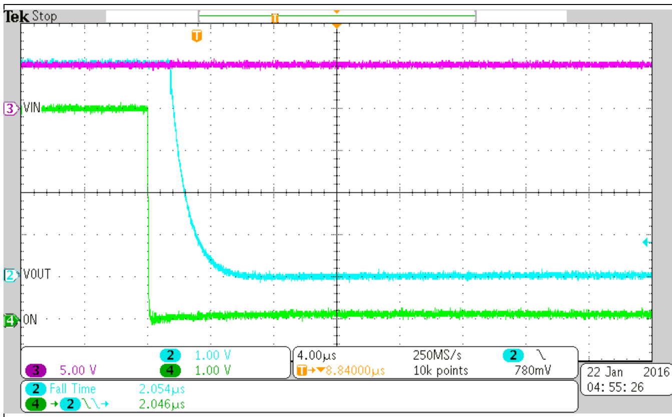
Figure 12. Turnon Time vs Input Voltage



V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 1000 pF

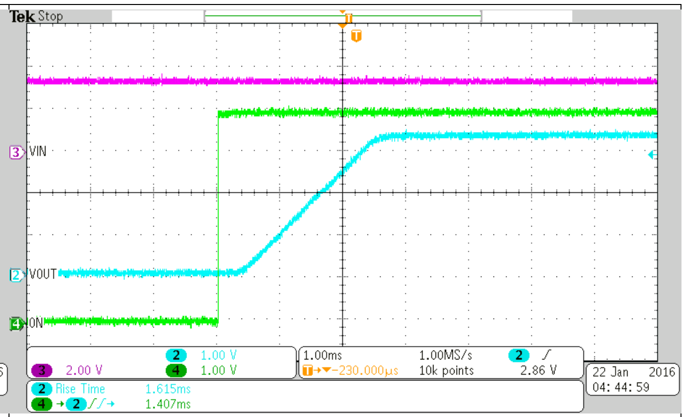
Figure 13. Rise Time (t_R) at V_{IN} = 5 V

Typical AC Characteristics (continued)



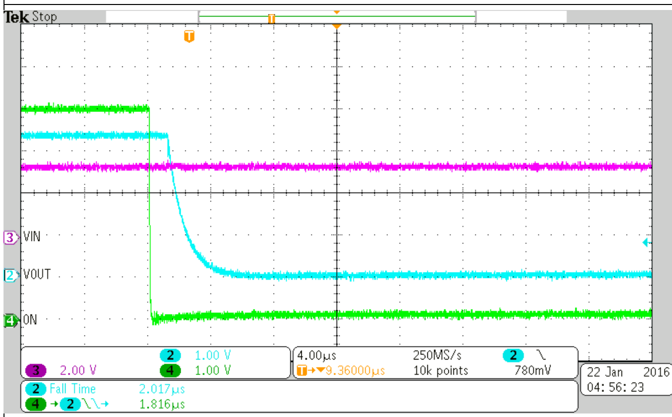
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω QOD = Open

Figure 14. Fall Time (t_F) at V_{IN} = 5 V



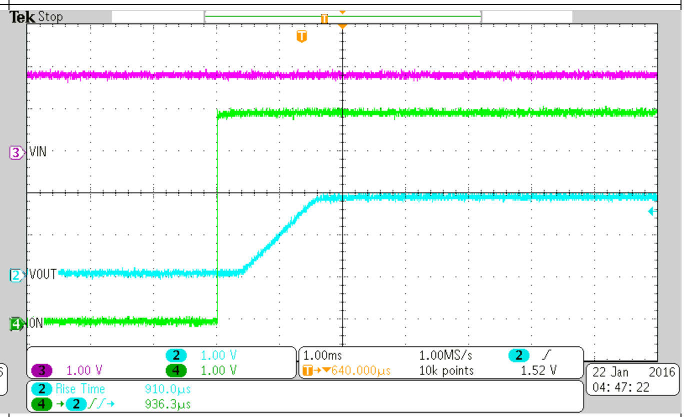
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 1000 pF

Figure 15. Rise Time (t_R) at V_{IN} = 3.3 V



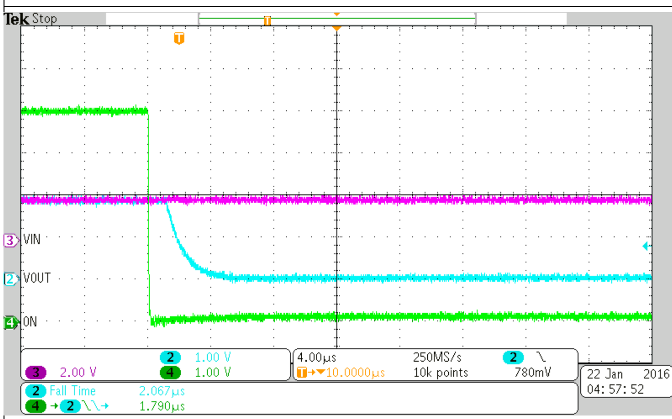
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω QOD = Open

Figure 16. Fall Time (t_F) at V_{IN} = 3.3 V



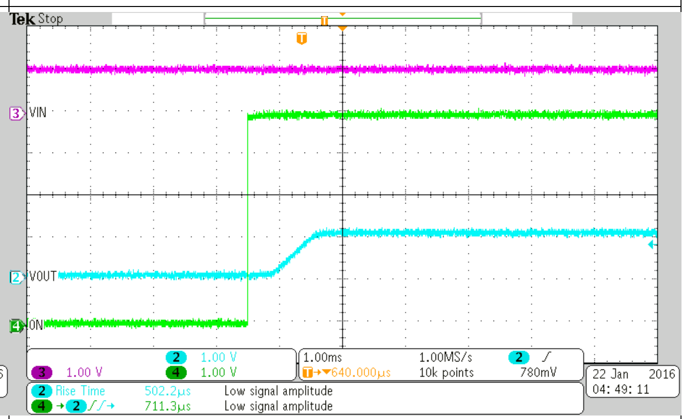
V_{IN} = 1.8 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 1000 pF

Figure 17. Rise Time (t_R) at V_{IN} = 1.8 V



V_{IN} = 1.8 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω QOD = Open

Figure 18. Fall Time (t_F) at V_{IN} = 1.8 V



V_{IN} = 1.0 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 1000 pF

Figure 19. Rise Time (t_R) at V_{IN} = 1 V

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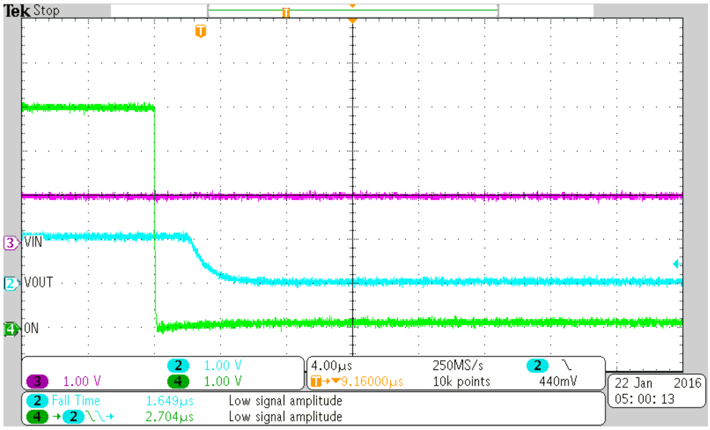
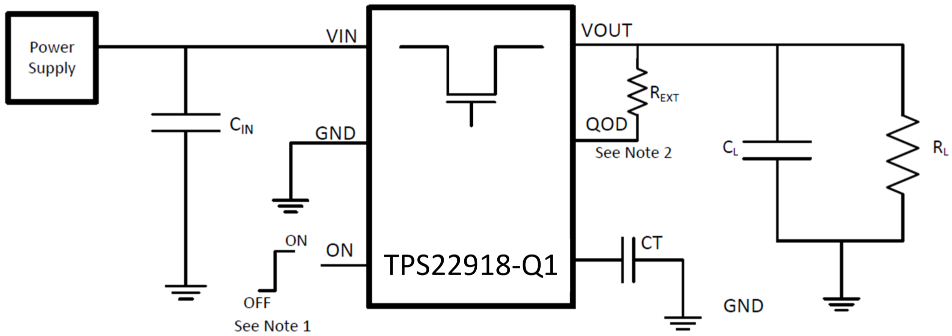
Typical AC Characteristics (continued)



V_{IN} = 1.0 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω   QOD = Open

Figure 20. Fall Time (t_F) at V_{IN} = 1 V

7 Parameter Measurement Information



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(1) Rise and fall times of the control signal is 100 ns.

(2) Turnoff times and fall times are dependent on the time constant at the load. For TPS22918-Q1, the internal pull-down resistance R_{PD} is enabled when the switch is disabled. The time constant is (R_{QOD} || R_L) × C_L where R_{QOD} equals R_{PD} + R_{EXT}.

Figure 21. Test Circuit

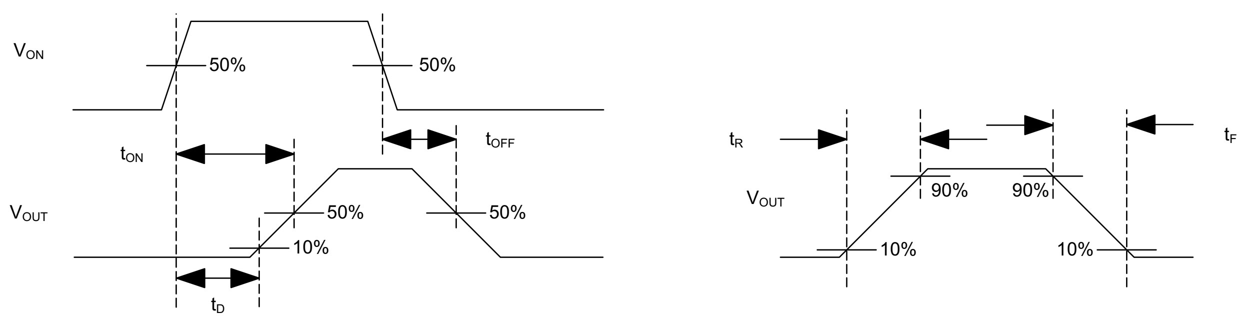


Figure 22. Timing Waveforms

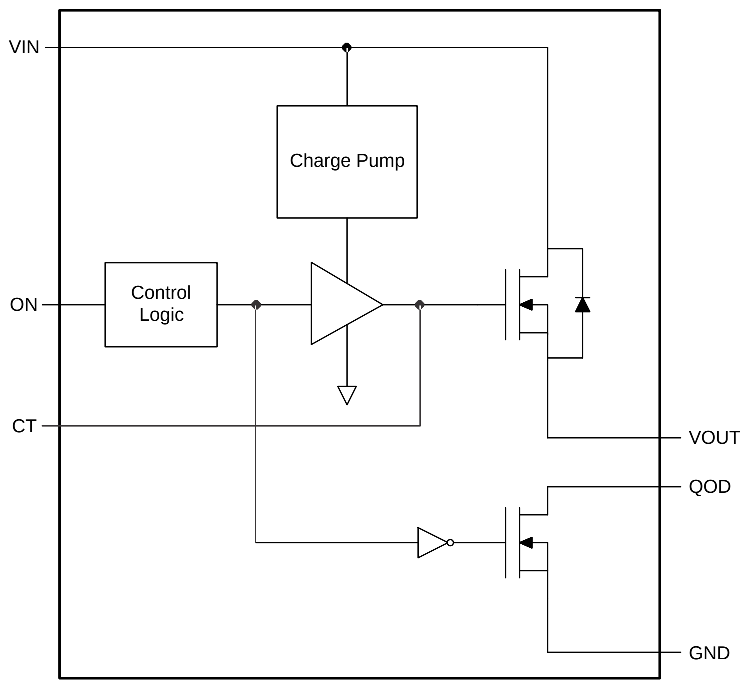
8 Detailed Description

8.1 Overview

The TPS22918-Q1 is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows to configure the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

8.3.2 Quick Output Discharge (QOD)

The TPS22918-Q1 includes a QOD feature. The QOD pin can be configured in one of three valid ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance R_{PD}. The value of this resistance is listed in the *Electrical Characteristics* table.
- QOD pin connected to VOUT pin using an external resistor R_{EXT}. After the switch becomes disabled, the discharge rate is controlled by the value of the total resistance of the QOD. To adjust the total QOD

Feature Description (continued)

resistance, Equation 1 can be used.

$$R_{QOD} = R_{PD} + R_{EXT} \tag{1}$$

Where:
- R_{QOD} is the total output discharge resistance
- R_{PD} is the internal pulldown resistance
- R_{EXT} is the external resistance placed between the VOUT and QOD pin.

- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

The fall times of the device depend on many factors including the total resistance of the QOD, V_{IN}, and the output capacitance. When QOD is shorted to VOUT, the fall time changes over V_{IN} as the internal R_{PD} varies over V_{IN}. To calculate the approximate fall time of V_{OUT} for a given R_{QOD}, use Equation 2 and Table 1.

$$V_{CAP} = V_{IN} \times e^{-t/\tau} \tag{2}$$

Where:
- V_{CAP} is the voltage across the capacitor (V)
- t is the time since power supply removal (s)
- τ is the time constant equal to $R_{QOD} \times C_L$

The fall times' dependency on V_{IN} becomes minimal as the QOD value increases with additional external resistance. See Table 1 for QOD fall times.

Table 1. QOD Fall Times

V_{IN} (V)	FALL TIME (µs) 90% - 10%, C_{IN} = 1 µF, I_{OUT} = 0 A , V_{ON} = 0 V (1)					
	T_A = 25°C			T_A = 85°C		
	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF
5.5	42	190	1880	40	210	2150
5	43	200	1905	45	220	2200
3.3	47	230	2150	50	260	2515
2.5	58	300	2790	60	345	3290
1.8	75	430	4165	80	490	4950
1.2	135	955	9910	135	1035	10980
1	230	1830	19625	210	1800	19270

(1) Typical values with QOD shorted to VOUT

8.3.2.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN}. Past a certain V_{IN} level, the strength of the R_{PD} is reduced. If there is still remaining charge on the output capacitor, this results in longer fall times. For further information regarding this condition, see the *Shutdown Sequencing During Unexpected System Power Loss* section.

8.3.2.2 Internal QOD Considerations

Special considerations must be taken when using the internal R_{PD} by shorting the QOD pin to the VOUT pin. The internal R_{PD} is a pulldown resistance designed to quickly discharge a load after the switch has been disabled. Care must be used to ensure that excessive current does not flow through R_{PD} during discharge so that the maximum T_J of 150°C is not exceeded. When using only the internal R_{PD} to discharge a load, the total capacitive load must not exceed 200 µF. Otherwise, an external resistor, R_{EXT}, must be used to ensure the amount of current flowing through R_{PD} is properly limited and the maximum T_J is not exceeded. To ensure the device is not damaged, the remaining charge from C_L must decay naturally through the internal QOD resistance and must not be driven.

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8.3.3 Adjustable Rise Time (CT)

A capacitor to GND on the CT pin sets the slew rate for each channel. The capacitor to GND on the CT pin must be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate is shown in Equation 3.

$$SR = 0.55 \times CT + 30 \quad (3)$$

where

- SR is the slew rate (in µs/V)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constant 30 are µs/V. The units for the constant 0.55 are µs/(V × pF)

Equation 3 accounts for 10% to 90% measurement on V_{OUT} and does not apply for CT less than 100 pF. Use Table 2 to determine rise times for when CT is greater or equal to 100 pF.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 2 contains rise time values measured on a typical device.

Table 2. Rise Time Table

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 2.5 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2V	VIN = 1.0 V
0	135	95	75	60	50	45	40
220	650	455	350	260	220	185	160
470	1260	850	655	480	415	340	300
1000	2540	1680	1300	960	810	660	560
2200	5435	3580	2760	2020	1715	1390	1220
4700	12050	7980	6135	4485	3790	3120	2735
10000	26550	17505	13460	9790	8320	6815	5950

As the voltage across the capacitor approaches the capacitor rated voltage, the effective capacitance reduces. Depending on the dielectric material used, the voltage coefficient changes. See Table 3 for the recommended minimum voltage rating for the CT capacitor.

Table 3. Recommended CT Capacitor Voltage Rating

V_{IN} (V)	RECOMMENDED CT CAPACITOR VOLTAGE RATING (V)(1)
1 V to 1.2 V	10
1.2 V to 4 V	16
4 V to 5.5 V	20

(1) If using V_{IN} = 1.2 V or 4 V, it is recommended to use the higher voltage rating.

8.4 Device Functional Modes

Table 4 describes the connection of the VOUT pin depending on the state of the ON pin.

Table 4. VOUT Connection

ON	QOD Configuration	TPS22918-Q1
L	QOD pin connected to VOUT with R_{EXT}	GND (via R_{EXT} + R_{PD})
L	QOD pin tied to VOUT directly	GND (via R_{PD})
L	QOD pin left open	Open
H	Any valid QOD configuration	VIN

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com (See the *Device Support* section for more information).

9.2 Typical Application

This typical application demonstrates how the TPS22918-Q1 can be used to power downstream modules.

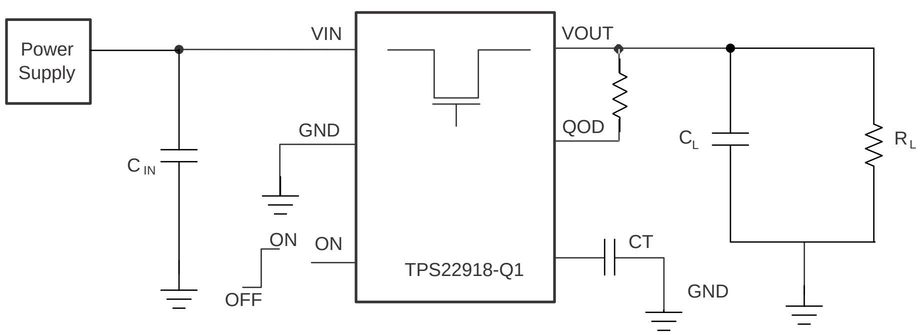

Figure 23. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the input parameters listed in Table 5.

Table 5. Design Parameter

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5 V
Load current	2 A
C_L	22 uF
t_F	4 ms
Maximum acceptable inrush current	400 mA

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9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between VIN and GND. A 1 µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.2.2.2 Output Capacitor (C_L) (Optional)

Becuase of the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.2.2.3 Shutdown Sequencing During Unexpected System Power Loss

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22918-Q1, adding a load switch to each power rail can be used to manage the power down sequencing in the event of an unexpected system power loss (battery removal). To determine the QOD values for each load switch, first confirm the power down order of the device this is wished to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down. Next, refer to Table 1 in the *Quick Output Discharge (QOD)* section to determine appropriate C_{OUT} and R_{QOD} values for each power rail's load switch so that the load switches' fall times correspond to the order in which they need to be powered down. In the above example, make sure this power rail's fall time to be 4 ms. Using Equation 2, to determine the appropriate R_{QOD} to achieve our desired fall time.

Because fall times are measured from 90% of V_{OUT} to 10% of V_{OUT}, Equation 2 becomes Equation 4.

$$.5\text{ V} = 4.5\text{ V} \times e^{-(4\text{ ms}) / (R \times (22\text{ µF}))} \tag{4}$$

$$R_{QOD} = 83.333\ \Omega \tag{5}$$

Refer to Figure 7, R_{PD} at V_{IN} = 5 V is approximately 25 Ω. Using Equation 1, the required external QOD resistance can be calculated as shown in Equation 6.

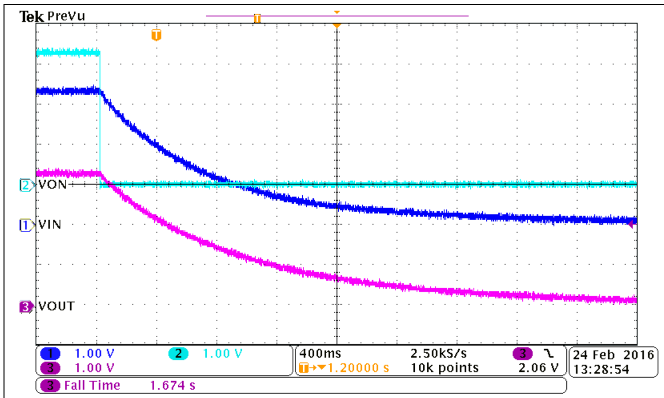
$$83.333\ \Omega = 25\ \Omega + R_{EXT} \tag{6}$$

$$R_{EXT} = 58.333\ \Omega \tag{7}$$

Figure 24 through Figure 29 are scope shots demonstrating an example of the QOD functionality when power is removed from the device (both ON and VIN are disconnected simultaneously). The input voltage is decaying in all scope shots below.

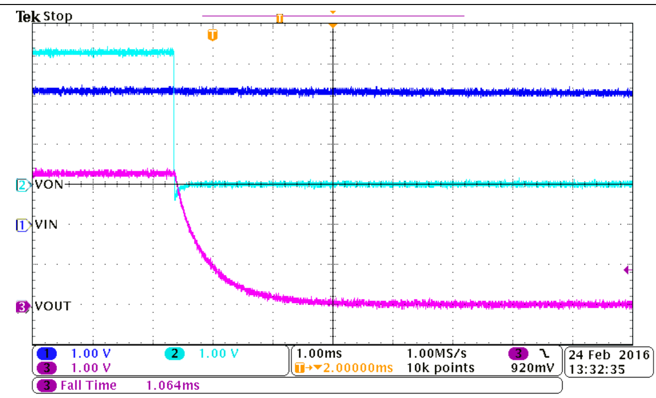
- Initial V_{IN} = 3.3 V
- QOD = Open, 500 Ω, or shorted to VOUT
- C_L = 1 µF, 10 µF
- V_{OUT} is left floating

NOTE: V_{IN} may appear constant in some figures. This is because the time scale of the scope shot is too small to show the decay of C_{IN}.



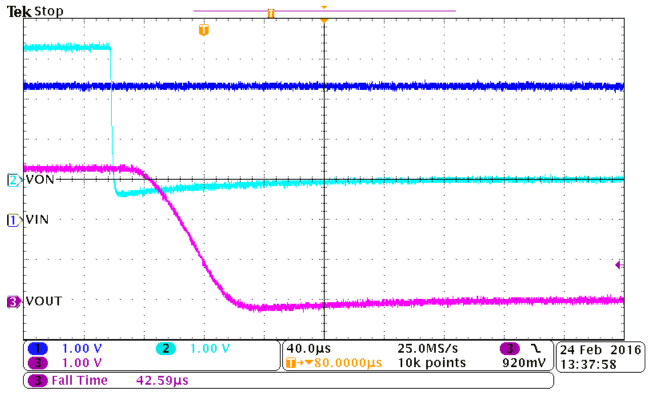
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 1 µF
QOD = Open

Figure 24. Fall Time (t_F) at V_{IN} = 3.3 V



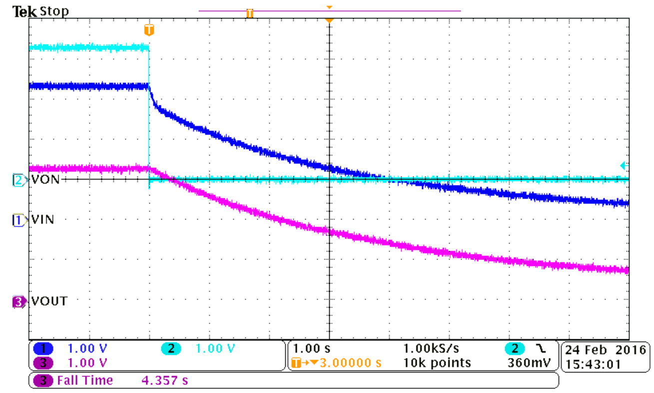
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 1 µF
QOD = 500 Ω

Figure 25. Fall Time (t_F) at V_{IN} = 3.3 V



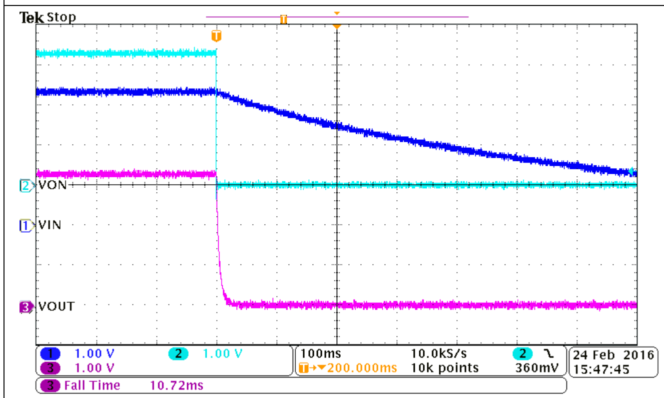
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 1 µF
QOD = V_{OUT}

Figure 26. Fall Time (t_F) at V_{IN} = 3.3 V



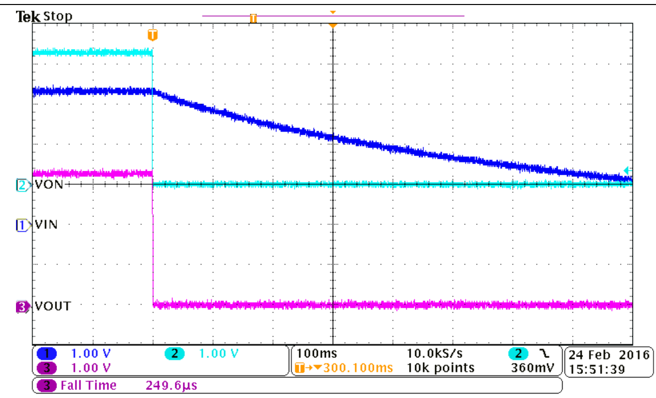
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 10 µF
QOD = Open

Figure 27. Fall Time (t_F) at V_{IN} = 3.3 V



V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 10 µF
QOD = 500 Ω

Figure 28. Fall Time (t_F) at V_{IN} = 3.3 V



V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 10 µF
QOD = VOUT

Figure 29. Fall Time (t_F) at V_{IN} = 3.3 V

9.2.2.4 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table. When the R_{ON} of the device is determined based upon the VIN conditions, use Equation 8 to calculate the VIN to VOUT voltage drop.

ΔV is the $I_{LOAD} \times R_{ON}$

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where

- ΔV is the voltage drop from VIN to VOUT
- I_{LOAD} is the load current
- R_{ON} is the On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated. (8)

9.2.2.5 Inrush Current

Use Equation 9 to determine how much inrush current is caused by the C_L capacitor.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the capacitance on VOUT
- dt is the output voltage rise time during the ramp up of VOUT when the device is enabled
- dV_{OUT} is the change in V_{OUT} during the ramp up of VOUT when the device is enabled (9)

The appropriate rise time can be calculated using the design requirements and the inrush current equation. As the rise time (measured from 10% to 90% of V_{OUT}) is calculated, this is accounted in the dV_{OUT} parameter (80% of V_{OUT} = 4 V) as shown in Equation 10.

$$400\ mA = 22\ \mu F \times 4\ V/dt \quad (10)$$

$$dt = 220\ \mu s \quad (11)$$

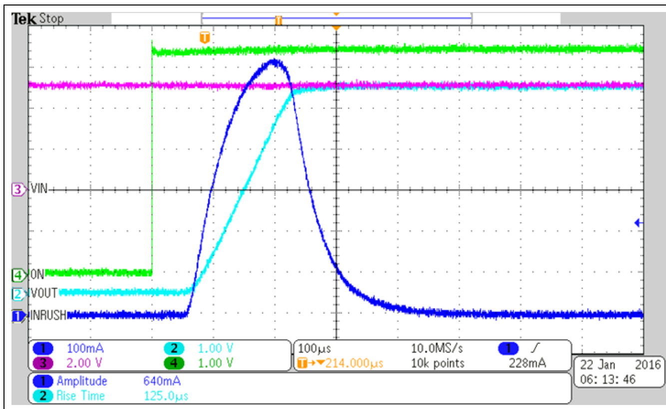
To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 220 µs. Refering to the Table 2 at V_{IN} = 5 V, CT = 220 µF provides a typical rise time of 650 µs. Adding this rise time and voltage into Equation 9, yields Equation 12.

$$I_{Inrush} = 22\ \mu F \times 4\ V / 650\ \mu s \quad (12)$$

$$I_{Inrush} = 135\ mA \quad (13)$$

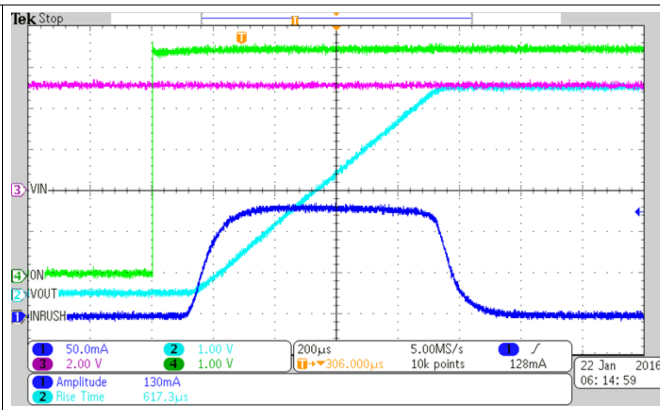
This inrush current can be seen in the *Application Curves* section. An appropriate C_L value must be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

9.2.3 Application Curves



V_{IN} = 5 V C_L = 22 µF CT = 0 µF

Figure 30. TPS22918-Q1 Inrush Current



V_{IN} = 5 V C_L = 22 µF CT = 220 µF

Figure 31. TPS22918-Q1 Inrush Current

10 Power Supply Recommendations

The TPS22918-Q1 is designed to operate from a VIN range of 1 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

- VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
- The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1 µF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The VOUT pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor must be placed as close to the device pins as possible.

11.2 Layout Example

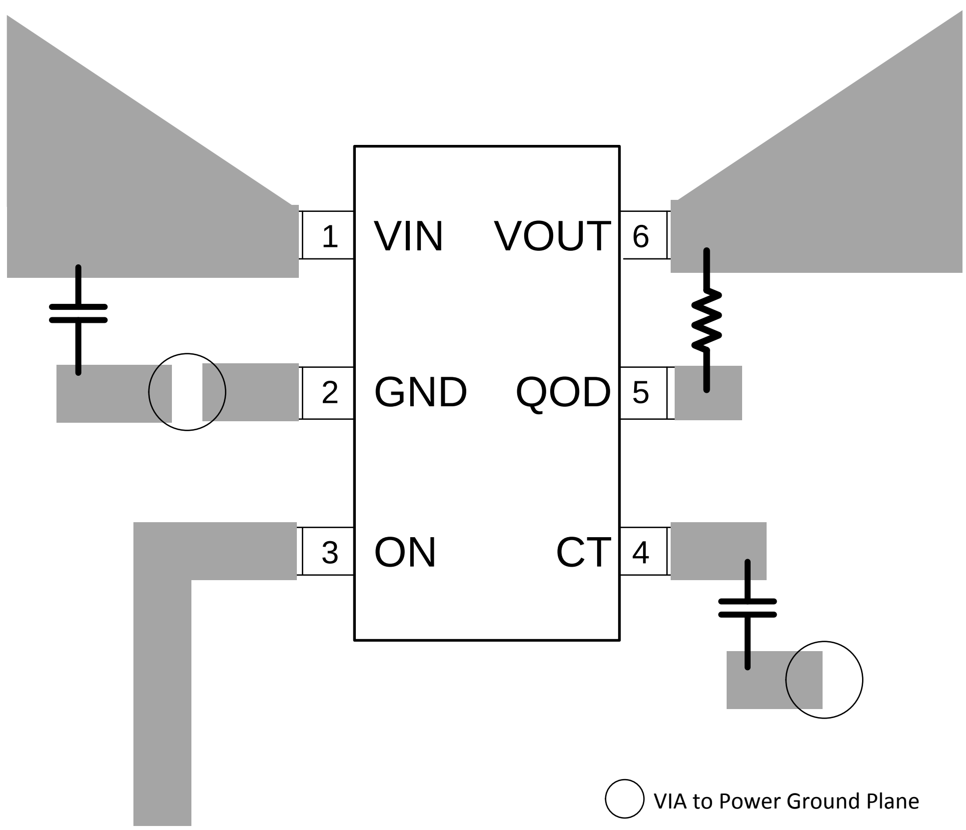


Figure 32. Recommended Board Layout

11.3 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

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Thermal Considerations (continued)

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 14.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (14)$$

Where:

$P_{D(MAX)}$ is the maximum allowable power dissipation
$T_{J(MAX)}$ is the maximum allowable junction temperature (150°C for the TPS22918-Q1)
T_A is the ambient temperature of the device
θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Developmental Support

For the TPS22918 PSpice Transient Model, see SLVMBI6.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *TPS22918 5.5-V, 2-A, 50-mΩ On-Resistance Load Switch Evaluation Module*, SLVUAP0
- *Quiescent Current vs Shutdown Current for Load Switch Power Consumption*, SLVA757
- *Fundamentals of On-Resistance in Load Switches*, SLVA771

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22918TDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	13NW	Samples
TPS22918TDBVTQ1	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	13NW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22918-Q1 :

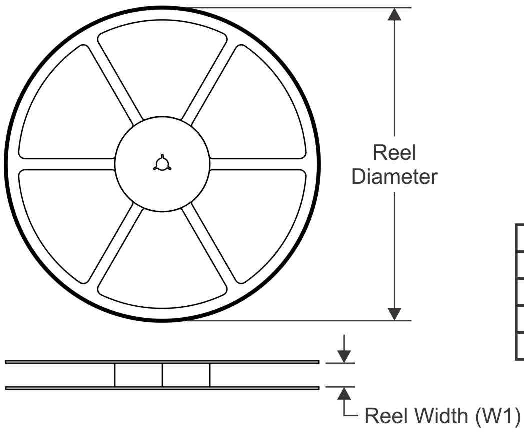
- Catalog: TPS22918

NOTE: Qualified Version Definitions:

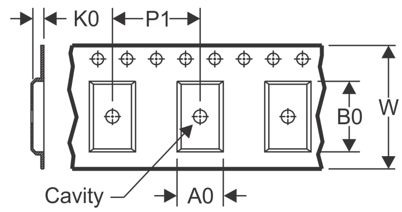
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

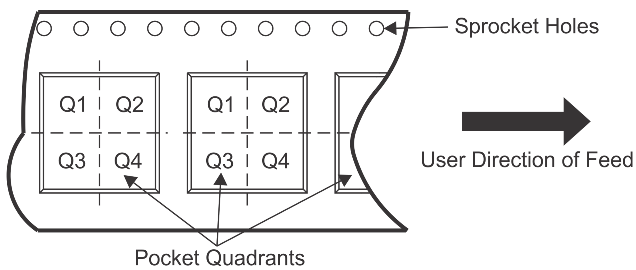


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

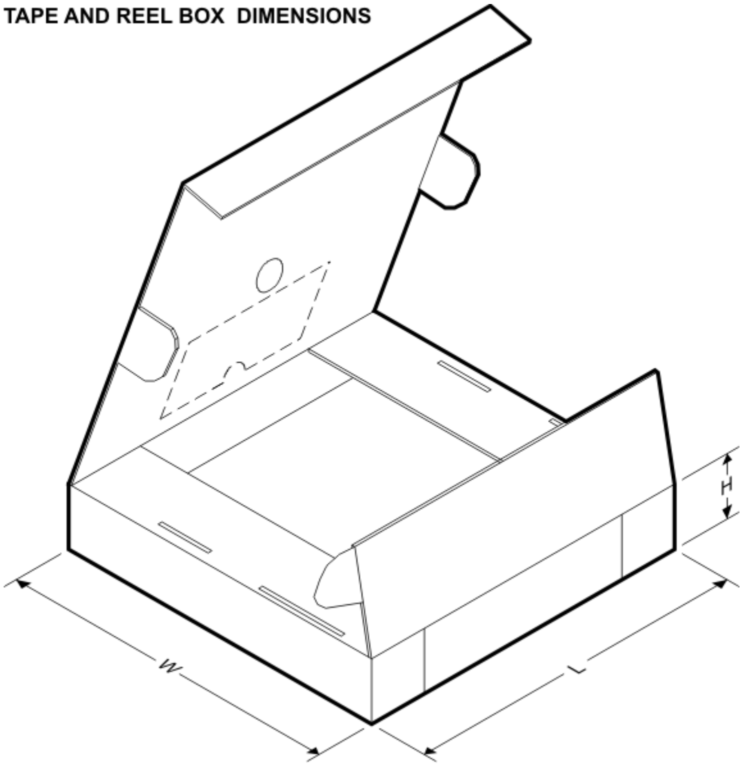
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22918TDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS22918TDBVTQ1	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

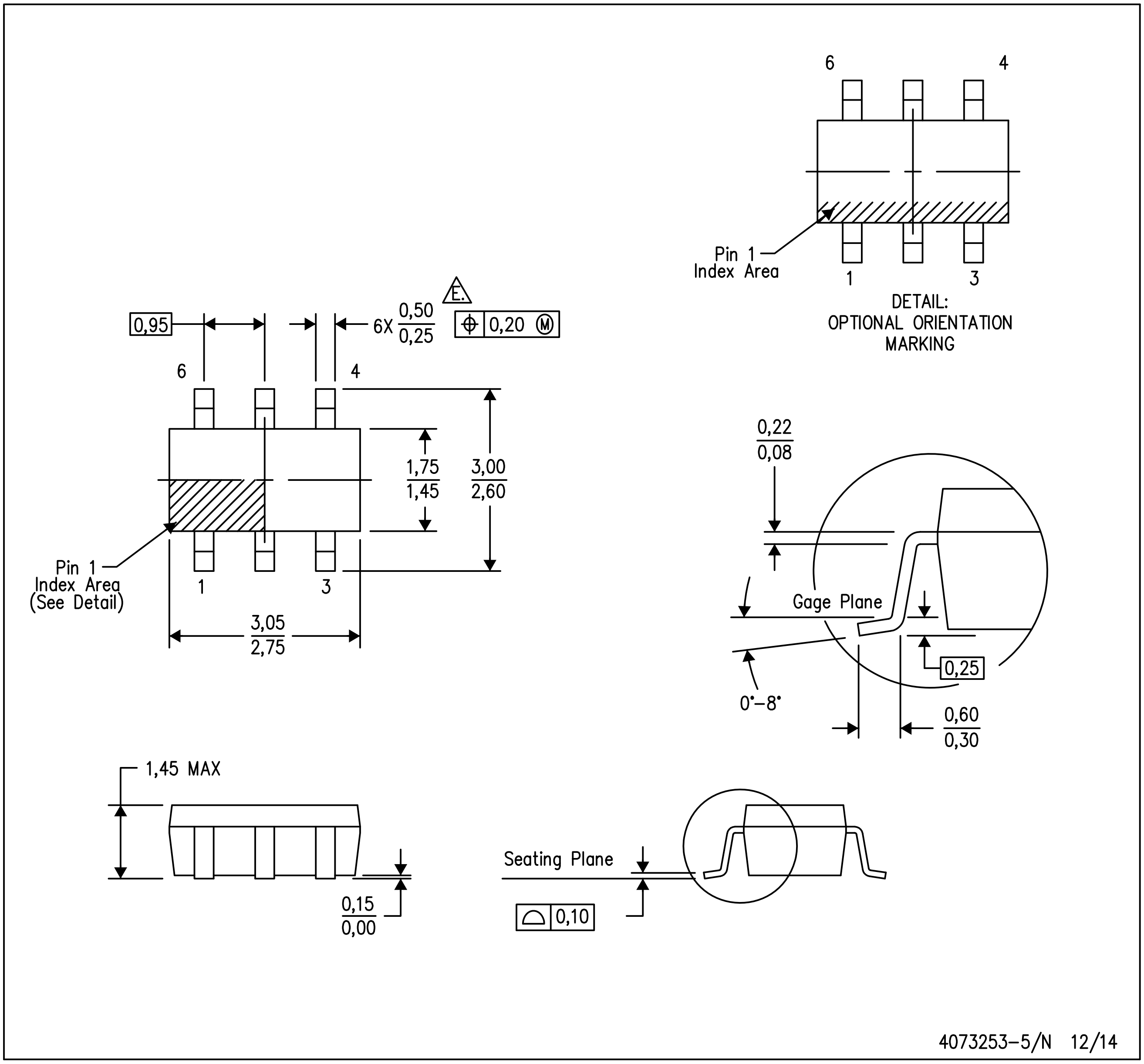
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

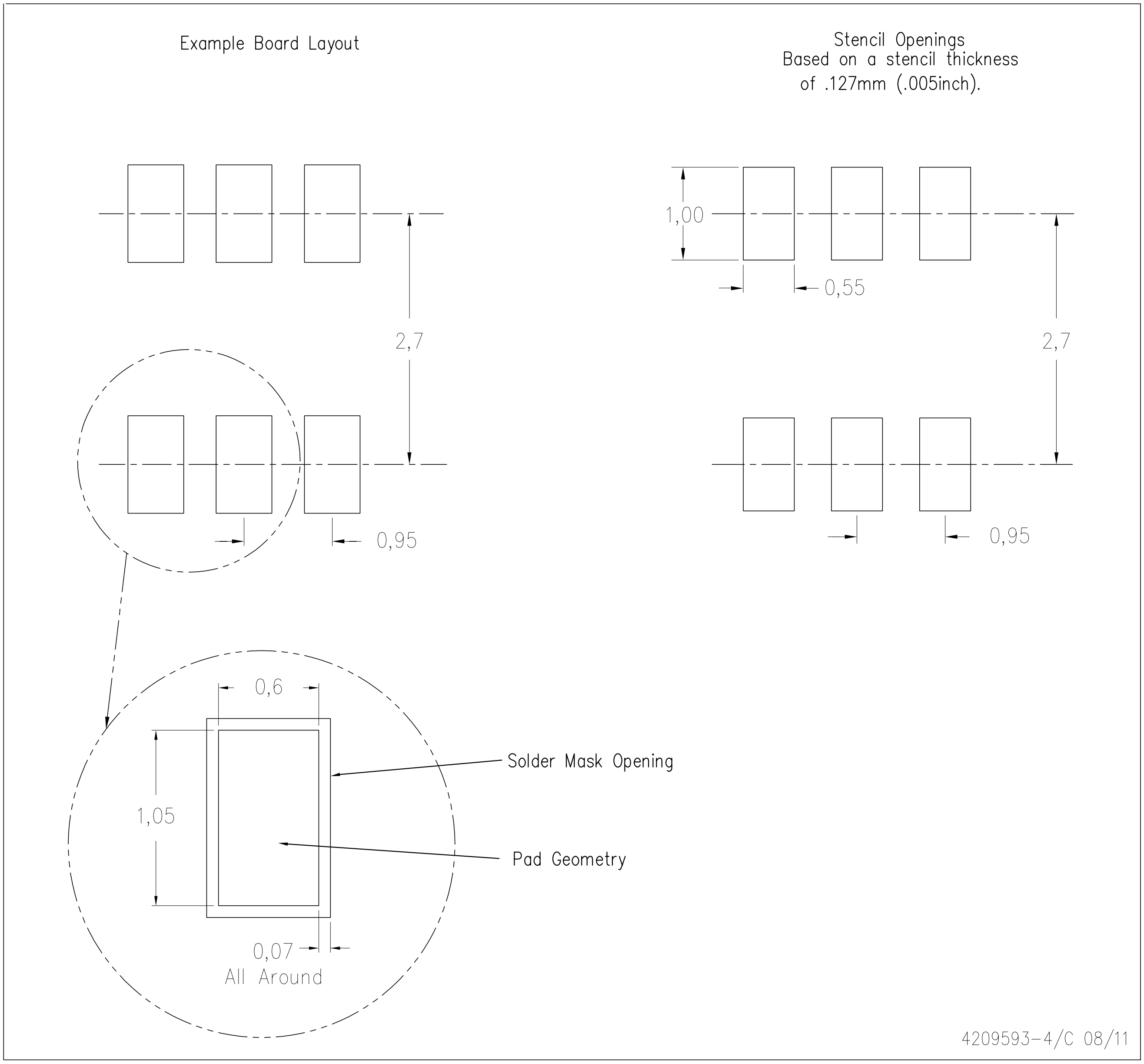
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22918TDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TPS22918TDBVTQ1	SOT-23	DBV	6	250	190.0	190.0	30.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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