# Low Voltage Dual SPDT Analog Switch with Negative Swing Audio Capability

## DESCRIPTION

The DG2750 is a dual SPDT low on-resistance switch designed to from a single 1.8 V to 5.5 V power supply. It is a bi-directional switch, and is capable of switching negative swing audio without the need for a coupling capacitor. With a single power supply, the audio signal can swing over the range from ((V+) - 5) to V+.

Guaranteed to operate with 1.4 V logic when V+ is in the range of 2.7 V to 5.5 V, the DG2750 will allow an easy interface with low voltage DSP or ASIC control logic.

The DG2750 is built on sub micron CMOS low voltage process technology, has very low quiescent current, and provides greater than 600 mA latch-up protection, as tested per JESD78.

The DG2750 is assembled in compact mQFN10, 1.4 mm x 1.8 mm x 0.55mm and ultra thin UTMQFN of 0.35 mm thickness.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The miniQFN-10 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL rating.

As a further sign of Vishay Siliconix's commitment, the DG2750 is fully RoHS-complaint and halogen-free.

## FEATURES

- Capable to switch negative swing audio without DC blocking capacitor
- Low signal distortion: THD+N < -98 dB
- Low on-resistance
- 1.4 V high logic
- Latch-up current > 600 mA (JESD78)
- ESD (HBM): 8 kV on I/O pins
- Reduced power consumption
- Reduce board space
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

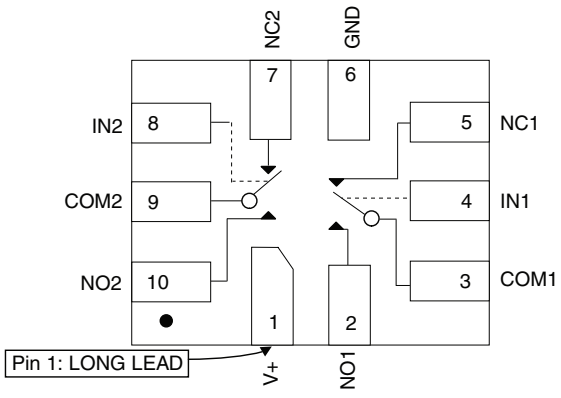
RoHS COMPLIANT

## APPLICATIONS

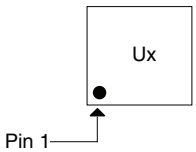
- Cellular phones
- Portable media players
- Computer and game machine
- Handheld healthcare and instruments

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**miniQFN-10L**




Top View




Device Marking: Ux for DG2750
x = Date/Lot Traceability Code

## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE | SIZE |
|---|---|---|---|
| DG2750DN-T1-E4 | -40 °C to 85 °C | miniQFN-10 | 1.4 mm x 1.8 mm x 0.55 mm |
| DG2750DN1-T1-GE4 | | UTMQFN-10 | 1.4 mm x 1.8 mm x 0.35 mm |

## TRUTH TABLE, DG2750

| IN1 (PIN 4) | IN2 (PIN 8) | FUNCTION |
|---|---|---|
| 0 | X | COM1 = NC1 |
| 1 | X | COM1 = NO1 |
| X | 0 | COM2 = NC2 |
| X | 1 | COM2 = NO2 |

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | LIMIT | UNIT |
|---|---|---|---|
| Reference to GND | V+, IN | -0.3 to 6 | V |
| | COM, NO, NC [a] | (V+) -5.5 or -2.5 whichever higher, (V+ + 0.3) | |
| Current (Any Terminal except COM, NO, NC, IN) | | 30 | mA |
| Continuous Current (COM, NO, NC, IN) | | ± 250 | |
| Peak Current (Pulsed at 1 ms, 10 % Duty Cycle) | | ± 500 | |
| Storage Temperature (D Suffix) | | -65 to 150 | °C |
| Power Dissipation (Packages) [b] | miniQFN-10 [c] | 208 | mW |
| ESD (Human Body Model) I/O to GND | | 8 | kV |
| Latch-up (per JESD78) | | 600 | mA |

**Notes**

a. Signals on COM, NO, NC, exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 2.6 mW/°C above 70 °C.

## SPECIFICATIONS (V+ = 2.7 V, ± 10 %)

| PARAMETER | SYMBOL | TEST CONDITIONS OTHERWISE UNLESS SPECIFIED | TEMP. [a] | LIMITS -40 °C to 85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN. [b] | TYP. [c] | MAX. [b] | |
| **Analog Switch** | | | | | | | |
| Analog Signal Range [d] | $V_{ANALOG}$ | | Full | -2.5 | - | V+ | V |
| On-Resistance | $R_{DS(on)}$ | V+ = 2.7 V, $V_S$ = ((V+) -4.5 V, -1 V, 0 V, 1 V, 2 V, V+), $I_S$ = 100 mA | Room | - | 0.45 | 1 | Ω |
| | | | Full | - | - | 1.3 | |
| On-Resistance Match | $\Delta R_{ON}$ | | Room | - | 0.1 | - | |
| On-Resistance Resistance Flatness | $R_{ON}$ Flatness | | Room | - | 0.3 | - | |
| Switch Off Leakage Current | $I_{NO/NC(off)}$ | V+ = 2.7 V, $V_{NC/NO}$ = -2.5 V or 2.5 V, $V_{COM}$ = 2.5 V or -2.5 V | Room | - | 50 | - | nA |
| | $I_{COM(off)}$ | | Full | -250 | - | 250 | |
| Channel On Leakage Current | $I_{COM(on)}$ | | Room | - | 50 | - | |
| | | | Full | -250 | - | 250 | |
| **Digital Control** | | | | | | | |
| Input Voltage High | $V_{INH}$ | V+ = 2.7 V to 4.3 V | Full | 1.4 | - | - | V |
| Input Voltage Low | $V_{INL}$ | | Full | - | - | 0.6 | |
| Input Capacitance | $C_{IN}$ | | Room | - | 6.5 | - | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | -1 | - | 1 | µA |

## SPECIFICATIONS (V+ = 2.7 V, ± 10 %)

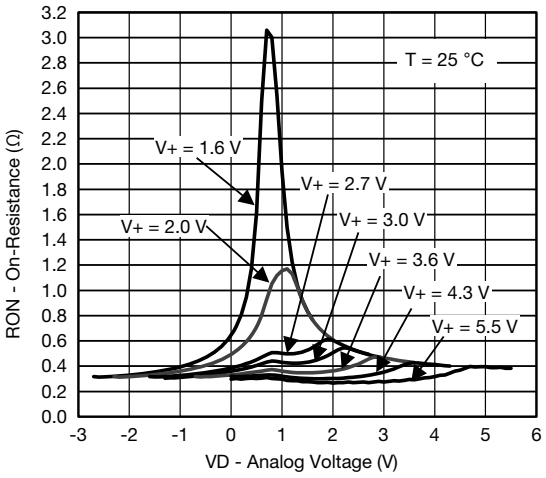
| PARAMETER | SYMBOL | TEST CONDITIONS OTHERWISE UNLESS SPECIFIED | TEMP. [a] | LIMITS -40 °C to 85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN.[b] | TYP. [c] | MAX. [b] | |
| **Dynamic Characteristics** | | | | | | | |
| Break-Before-Make Time [e, d] | $t_{BBM}$ | V+ = 3 V, $V_S$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room | 800 | 1160 | - | ns |
| | | | Full | 1000 | - | - | |
| Enable Turn-On Time [e, d] | $t_{ON(EN)}$ | | Room | - | 1200 | 2100 | |
| | | | Full | - | - | 2500 | |
| Enable Turn-Off Time [e, d] | $t_{OFF(EN)}$ | | Room | - | 33 | 130 | |
| | | | Full | - | - | 150 | |
| Charge Injection [d] | $Q_{INJ}$ | $C_L$ = 1 nF, $R_{GEN}$ = 0 Ω, $V_{GEN}$ = 0 V | Room | - | 4 | - | pC |
| Total Harmonic Distortion Plus Noise | THD+N | f = 20 Hz to 20 kHz, $V_{COM}$ = 0.5 $V_{P-P}$, $R_S$ = $R_L$ = 600 Ω; DC bias = 0 V | | - | < -98 | - | dB |
| Off-Isolation [d] | OIRR | V+ = 3 V, $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 300 kHz | | - | -54 | - | dB |
| Crosstalk [d] | $X_{TALK}$ | | | - | -60 | - | |
| Bandwidth [d] | BW | V+ = 3 V, $R_L$ = 50 Ω, -3 dB | | - | 49 | - | MHz |
| Channel-Off Capacitance [d] | $C_{NC/NO(off)}$ | V+ = 3 V, f = 1 MHz | | - | 36 | - | pF |
| Channel-On Capacitance [d] | $C_{COM/NC/NO(on)}$ | | | - | 106 | - | |
| Power Supply | | | | | | | |
| Power Supply Range | V+ | | | 1.8 | - | 5.5 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 V, or V+ | Full | - | - | 2 | µA |

**Notes**

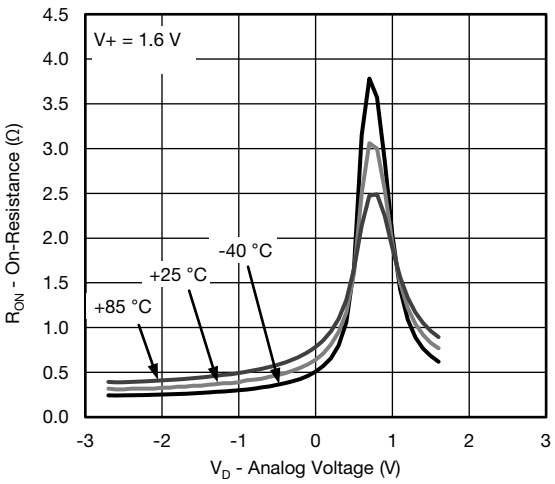
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.
f. Crosstalk measured between channels.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

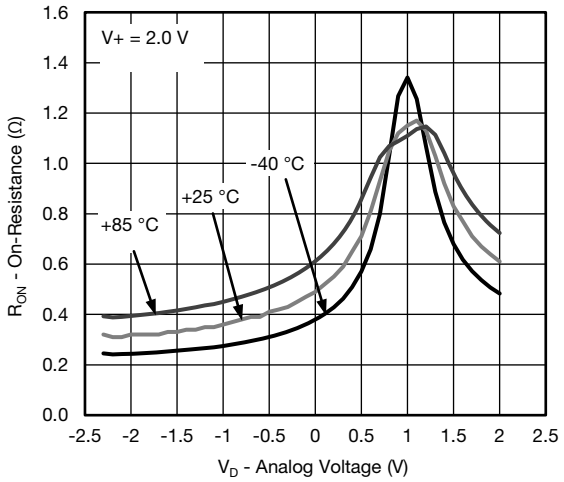



**On-Resistance vs. $V_D$ and Single Supply Voltage**

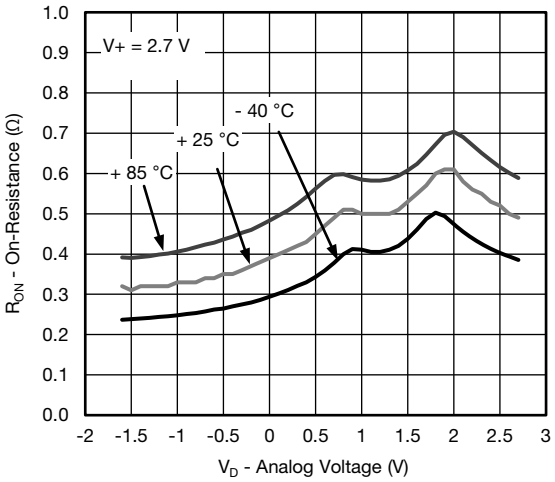



**On-Resistance vs. Analog Voltage and Temperature**

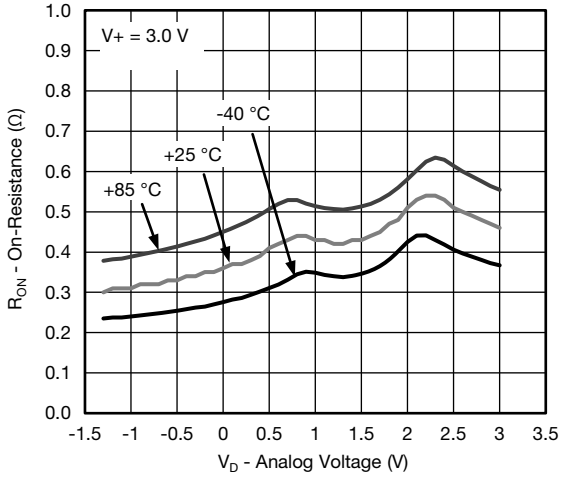
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



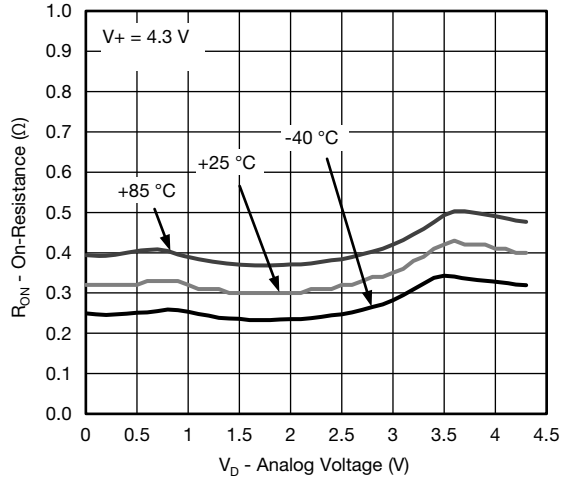

**On-Resistance vs. Analog Voltage and Temperature**



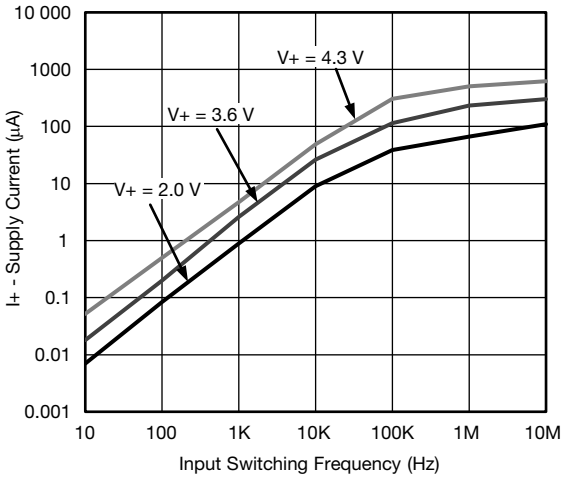

**On-Resistance vs. Analog Voltage and Temperature**



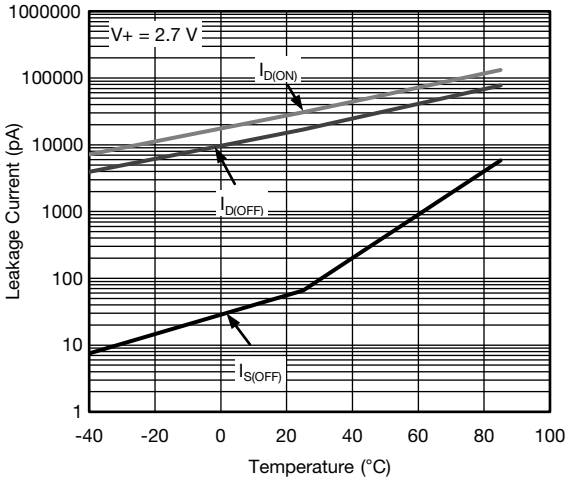

**On-Resistance vs. Analog Voltage and Temperature**




**On-Resistance vs. Analog Voltage and Temperature**

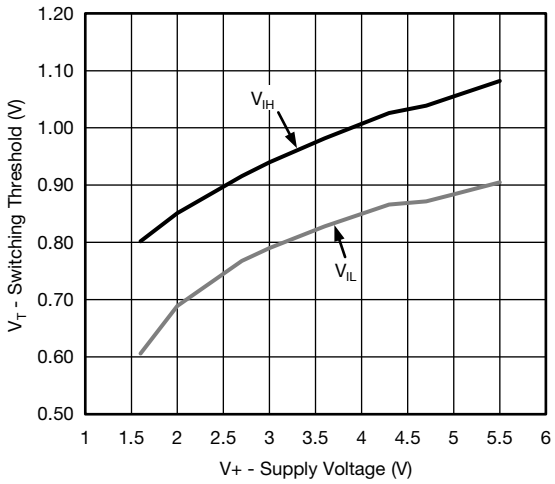



**Supply Current vs. Input Switching Frequency**

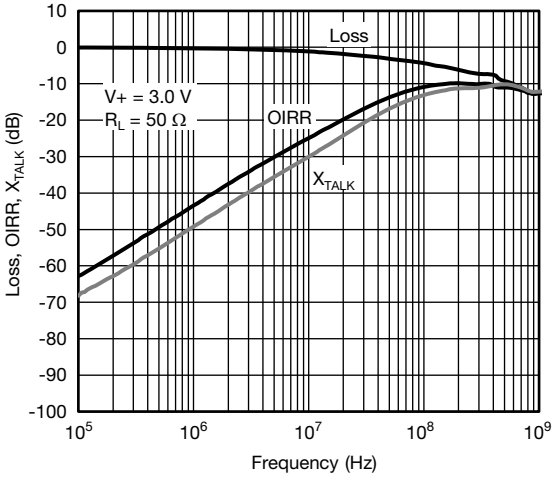



**Leakage Current vs. Temperature**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

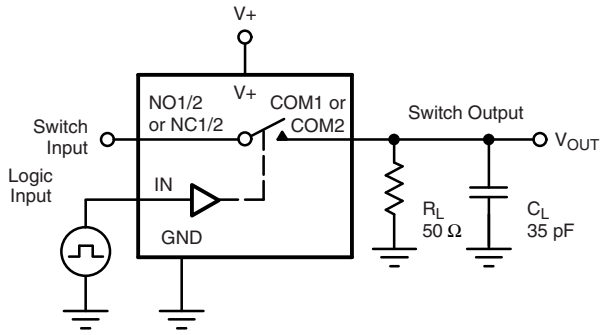



**Switching Threshold vs. Supply Voltage**



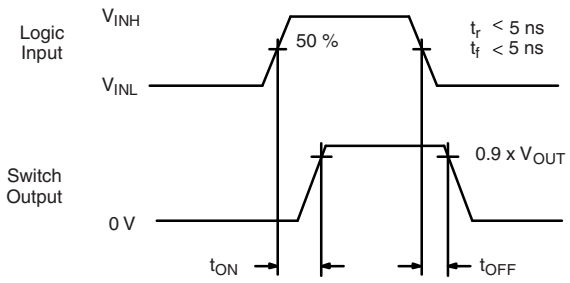

**Insertion Loss, Off-Isolation, Crosstalk vs. Frequency**

## TEST CIRCUITS



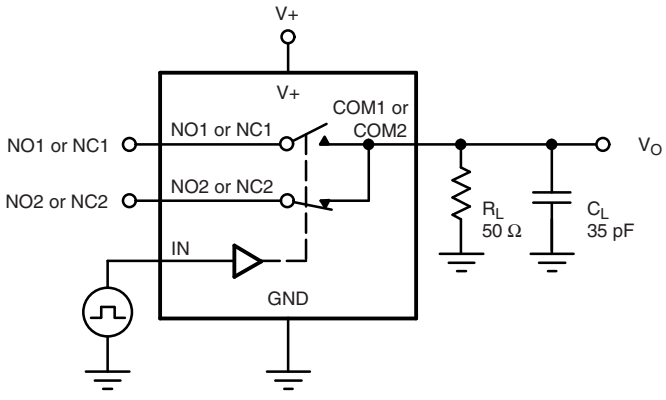

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

**Fig. 1 - Switching Time**




$C_L$ (includes fixture and stray capacitance)

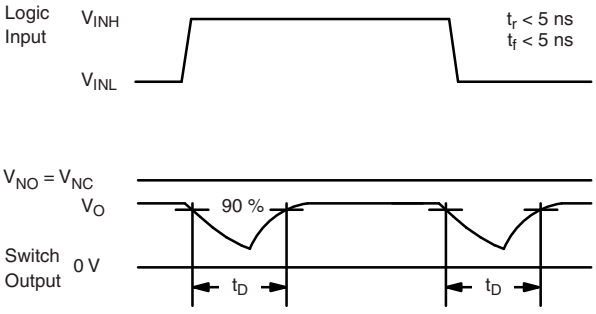
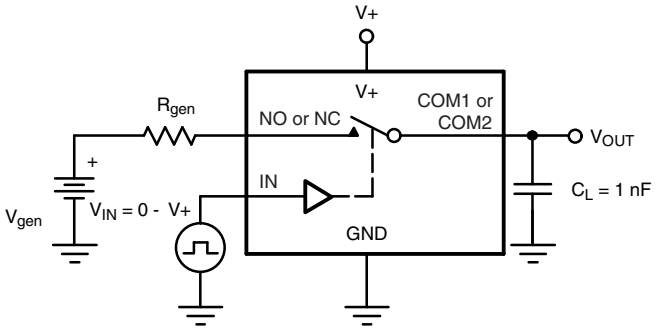
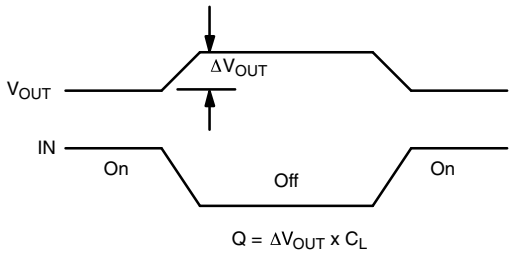



**Fig. 2 - Break-Before-Make Interval**

## TEST CIRCUITS




IN depends on switch configuration: input polarity determined by sense of switch.

**Fig. 3 - Charge Injection**

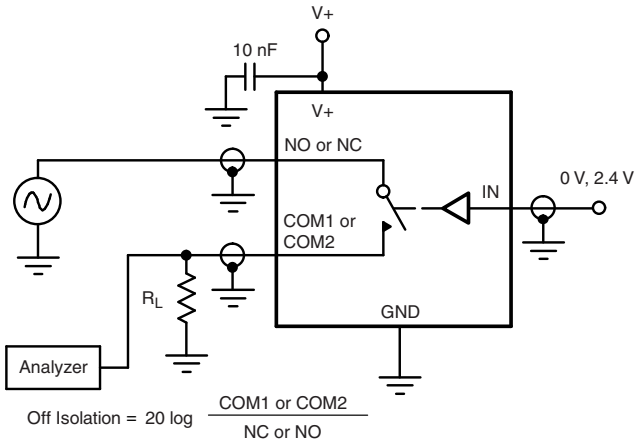



**Fig. 4 - Off-Isolation**

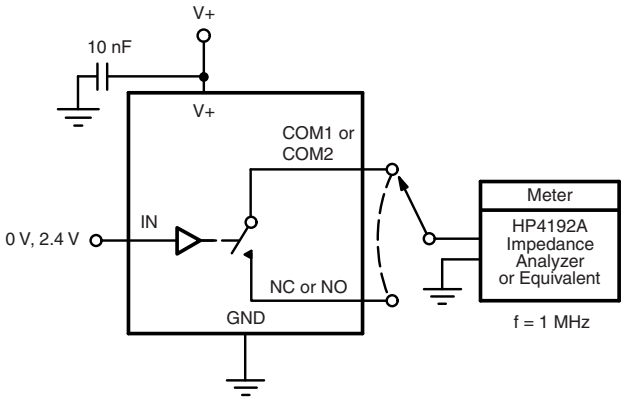
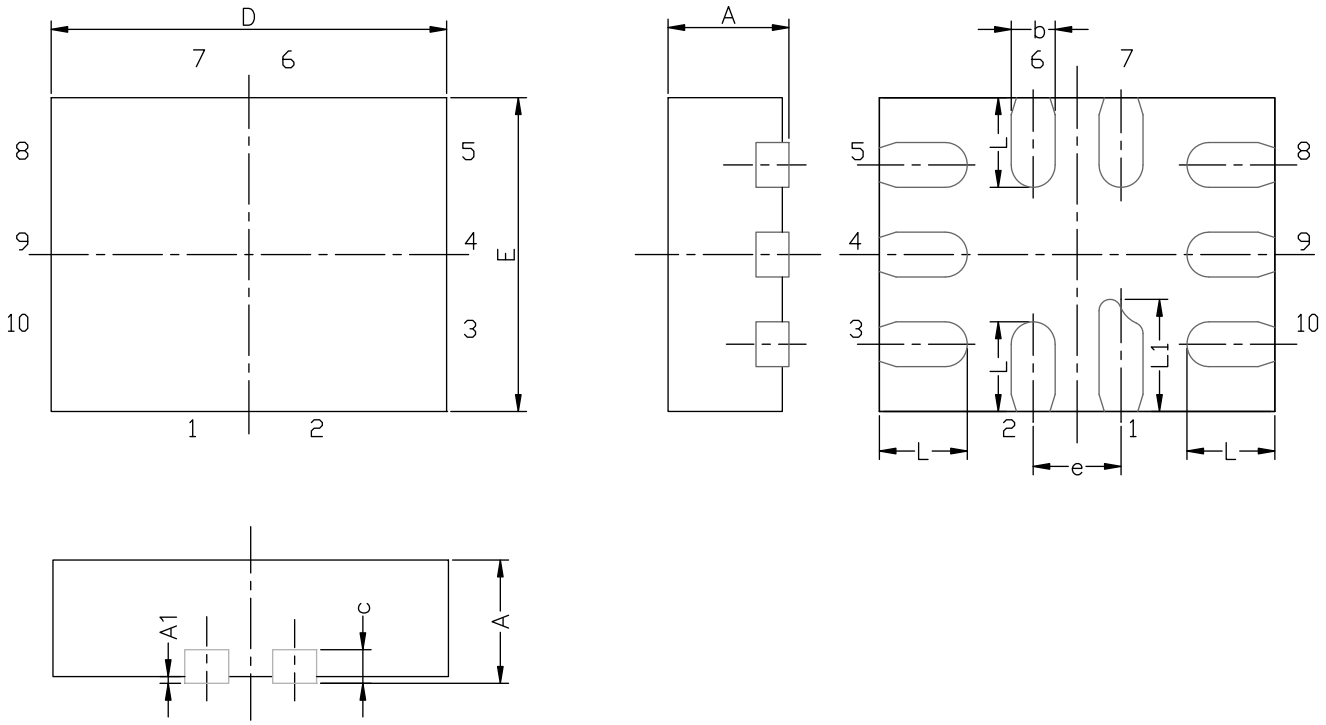



**Fig. 5 - Channel Off/On Capacitance**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64736.*

# MINI QFN-10L CASE OUTLINE



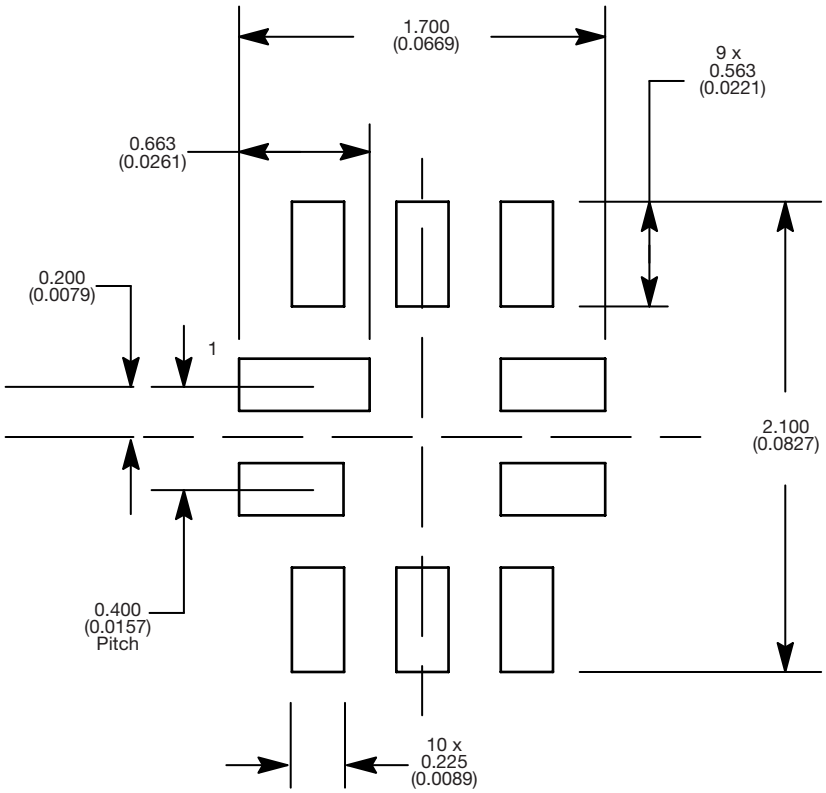

| DIM | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NAM. | MAX. | MIN. | NAM. | MAX. |
| A | 0.45 | 0.55 | 0.60 | 0.0177 | 0.0217 | 0.0236 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| c | 0.150 or 0.127 REF (1) | | | 0.006 or 0.005 REF (1) | | |
| D | 1.70 | 1.80 | 1.90 | 0.067 | 0.071 | 0.075 |
| E | 1.30 | 1.40 | 1.50 | 0.051 | 0.055 | 0.059 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L1 | 0.45 | 0.50 | 0.55 | 0.0177 | 0.0197 | 0.0217 |

**Note**

(1) The dimension depends on the leadframe that assembly house used.

ECN T16-0163-Rev. B, 16-May-16
DWG: 5957

**RECOMMENDED MINIMUM PADS FOR MINI QFN 10L**




Mounting Footprint
Dimensions in mm (inch)

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